DATA HANDBOOK

ICs for Telecom
Subscriber Sets
Cordless Telephones
Mobile/cellular
Radio Pagers
PCD4413A to 74HC/HCT7046A

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PHILIPS

ICs for Telecom
Subscriber sets
Cordless Telephones
Mobile/Cellular
Radio Pagers

Part a
Selection Guide page

Functional index 5

Numerical index 13

Comparison of the TEA1060 family 25

Comparison of microcontrollers for telephone sets 26

General

Product status definitions for type numbers with prefixes CA, MC, NE, SA and SE 29

Ordering information for type numbers with prefixes CA, MC, NE, SA and SE 30

Type designation for type numbers with prefixes FCB, FCF, OM, PCA, PCB, PCD, PCF, TDA, TDD, TEA, UAA and UMA 31

Rating systems for type numbers with prefixes FCB, FCF, OM, PCA, PCB, PCD, PCF, TDA, TDD, TEA, UAA and UMA 33

Handling MOS devices 35

Device data

CA3089 to PCD4413

Part b

Selection Guide

Functional index 901

Numerical index 909

Device data

PCD4413A to 74HC/HCT7046A

Package information

Package outlines 1687

Soldering 1727

SELECTION GUIDE

Functional index
Numerical index

FUNCTIONAL INDEX

type number	description	page
AMPLIFIERS		
NE542	dual low-noise preamplifier	69
NE/SA5204	wideband high-frequency amplifier	231
NE/SA/SE5205	wideband high-frequency amplifier	241
NE/SA5209	wideband variable gain amplifier	253
NE/SA5230	low-voltage operational amplifier	267
NE/SA5234	matched quad high-performance low-voltage operational amplifier	279
NE/SE5539	high-frequency operational amplifier	285
TDA1011	2 to 6 W audio power amplifier	1267
TDA1011A	2 to 6 W audio power amplifier	1279
TDA1015T	0.5 W audio power amplifier	1287
TDA7050	140 mW BTL or 2 x 75 mW mono/stereo audio power amplifier; low-voltage (in plastic DIL8)	1305
TDA7050T	140 mW BTL or 2 x 75 mW mono/stereo audio power amplifier; low-voltage (in SO8 plastic mini-pack)	1309
TDA7052	1 W BTL mono audio amplifier	1313
TDA7053	2 x 1 W BTL portable/mains-fed stereo power amplifier	1319
AUDIO AND DATA PROCESSORS		
NE/SA5750	audio processor - companding and amplifier section	293
NE/SA5751	audio processor - filter and control section	301
UMA1000T	data processor for AMPS/TACS cellular radio (DPROC); I²C-bus	1561
CALL PROGRESS DECODER		
NE5900	call progress decoder	311
CLOCK/CALENDAR		
PCF8573	clock/calendar with serial I/O; I²C-bus	1163
PCF8583	clock/calendar with 256 x 8-bit static RAM; I²C-bus	1233
COMPANDORS		
NE570/571/SA571	compandor	113
NE/SA572	programmable analog compandor	123
NE/SA575	low-voltage compandor	131
NE/SA575	low-voltage compandor in very small outline package (VSOP)	143
NE/SA577	unity gain level programmable low-power compandor	153
NE/SA578	unity gain level programmable low-power compandor	157
DATA CONVERSION		
PCF8591	8-bit ADC/DAC; I²C-bus	1239
DIGITAL SIGNAL PROCESSORS		
PCB5010	single-chip digital signal processor	379
PCB5011	ROM-less version of PCB5010	379

ICs for Telecom — Functional index

type number	description	page
DISPLAY DRIVERS		
PCF21XX Family	LCD duplex drivers	1025
PCF2201	LCD flat-panel row/column driver	1041
PCF8566	universal LCD driver for low multiplex rates (1:1 to 1:4) max. 96 segments; I²C-bus	1145
PCF8569	LCD column driver for dot matrix graphic displays at multiplex rates of 1:8 or 1:16; 40 outputs; I²C-bus	1151
PCF8576	universal LCD driver for low multiplex rates (1:1 to 1:4) max. 160 segments; I²C-bus	1191
PCF8577/A/C/CA	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	1201
PCF8578	LCD row/column driver for dot matrix graphic displays; 40 outputs (24 are programmable); I²C-bus	1209
PCF8579	LCD column driver for dot matrix graphic displays; 40 column outputs; I²C-bus	1219
DTMF GENERATORS/DIALLERS		
PCD3311C/12C	DTMF/modem/music tone generators with binary-coded parallel input or serial data input; I²C-bus	509
PCD4420	pulse and DTMF dialler with redial for 4 x 4 keypad	977
PCD4421	pulse and DTMF dialler with redial for 4 x 5 keypad	987
DIALLER ICs		
Pulse		
OM1036C	dialler circuit with redial	319
PCD332XC Family	pulse dialler circuits with redial	531
Pulse/DTMF		
PCD3310 Family	pulse and DTMF dialler with redial	485
PCD3347	pulse/DTMF dialler with redial	741
PCD4410	pulse and DTMF dialler with redial; manual access pause; 3 x 4 keypad plus flash; mark/space ratio 2:1; tone burst 70/140 ms; data memory	867
PCD4413	variant of PCD4410 without redial; mark/space ratio 3:2; tone burst 70/70 ms	883
PCD4413A	PCD4413 with flash time of 255 ms	923
PCD4415	PCD4410 with 3 x 4 or 3 x 5 keypad; tone burst 70/70 ms	937
PCD4415A	PCD4415 with mark/space ratio of 3:2	957
Repertory		
PCD3341	advanced 10-100-number repertory pulse/DTMF dialler; LCD control; I²C-bus	561
EXPANDERS		
PCF8574	remote 8-bit I/O expander; I²C-bus	1179
PCF8574A	remote 8-bit I/O expander; I²C-bus; different slave address	1179

ICs for Telecom — Functional index

type number	description	page
FREQUENCY SYNTHESIZERS		
TDD1742T	low-power frequency synthesizer (LOPSY)	1327
UMA1010T	low-power universal frequency synthesizer for radio communications; 400 MHz to 1150 MHz; I²C-bus	1591
UMA1012T	low-power universal frequency synthesizer for radio communications; 20 to 600 MHz; I²C-bus	1605
I²C-BUS COMPATIBLE ICs (excluding microcontrollers)		
PC.8582 Family	256 x 8-bit static EEPROMS; CMOS; for automotive applications	345
PCD3311C/12C	DTMF/modem/music tone generators with binary-coded parallel input or serial data input	509
PCD3341	advanced 10-100-number repertory pulse/DTMF dialler; LCD control	561
PCF8200	voice synthesizer (CMOS)	1053
PCF8566	universal LCD driver for low multiplex rates (1:1 to 1:4) max. 96 segments	1145
PCF8569	LCD column driver for dot matrix graphic displays at multiplex rates of 1:8 or 1:16; 40 outputs	1151
PCF8570/C	256 x 8-bit static RAM	1159
PCF8571	128 x 8-bit static RAM	1159
PCF8573	clock/calendar	1163
PCF8574/A	remote 8-bit I/O expander	1179
PCF8576	universal LCD driver for low multiplex rates (1:1 to 1:4) max. 160 segments	1191
PCF8577/A/C/CA	LCD direct driver (32 segments) or duplex driver (64 segments)	1201
PCF8578	LCD row/column driver for dot matrix graphic displays; 40 outputs (24 are programmable)	1209
PCF8579	LCD row/column driver for dot matrix graphic displays; 40 column outputs	1219
PCF8581/C	128 x 8-bit static EEPROM; low-voltage	1229
PCF8583	clock/calender with 256 x 8-bit static RAM	1233
PCF8591	8-bit ADC/DAC	1239
UMA1000T	data processor for cellular radio (DPROC)	1561
UMA1010T	low-power universal frequency synthesizer for radio communications; 400 MHz to 1150 MHz	1591
UMA1012T	low-power universal frequency synthesizer for radio communications; 20 to 600 MHz	1605
LISTENING-IN CIRCUIT		
TEA1085	listening-in circuit for line powered telephone sets; with anti-Larsen limiter	1509
MEMORIES		
FCB61C65 (L/LL)	8K x 8 high speed CMOS low-power static RAM; access time = 55 and 70 ns	45
FCF61C65 (L/LL)	8K x 8 high speed CMOS low-power static RAM for extended temperature range; access time = 85 ns	55
PC.8582 Family	256 x 8-bit static EEPROM ; CMOS; I²C-bus	345
PCD5101	256 x 4-bit static RAM	997
PCD5114	1024 x 4-bit static RAM	1003
PCF8570	256 x 8-bit static RAM; I²C-bus	1159
PCF8570C	256 x 8-bit static RAM; I²C-bus; different slave address	1159
PCF8571	128 x 8-bit static RAM; I²C-bus	1159
PCF8581/C	128 x 8-bit static EEPROM; low-voltage; I²C-bus	1229
PCF8583	clock/calendar with 256 x 8-bit static RAM; I²C-bus	1233

ICs for Telecom — Functional index

type number	description	page
MICROCONTROLLERS		
PCA80C552-4	256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; –40 to +125 °C	435
PCA80C562	256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2 pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; –40 to +125 °C	449
PCA80C652	256 x 8 RAM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; –40 to +125 °C	463
PCA83C552-4	256 x 8 RAM; 4K x 8 ROM; 80C31 CPU plus 16-bit capture/compare timer/ counter; watchdog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; –40 to +125 °C	435
PCA83C562	256 x 8 RAM; 8K x 8 ROM; 80C531 CPU plus 16-bit capture/compare timer/ counter; watchdog timer; 2 pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; –40 to +125 °C	449
PCA83C652	256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; –40 to +125 °C	463
PCB80C552-4	256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; 0 to +70 °C	435
PCB80C562	256 x 8 RAM; 80C531 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2 pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; –40 to +125 °C	449
PCB80C652	256 x 8 RAM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; 0 to +70 °C	463
PCB80C851	128 x 8 RAM; 256 x 8 EEPROM; 1.2 to 12 MHz; 0 to +70 °C; special security mode	475
PCB83C552-4	256 x 8 RAM; 8K x 8 ROM; 80C31 CPU plus 16-bit capture/compare timer/ counter; watchdog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; 0 to +70 °C	435
PCB83C562	256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/ counter; watchdog timer; 2 pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; –40 to +125 °C	449
PCB83C652	256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; 0 to +70 °C	463
PCB83C851	128 x 8 RAM; 4K x 8 ROM; 256 x 8 EEPROM; 1.2 to 12 MHz; 0 to +70 °C; special security mode	475
PCD33XX Family	single-chip 8-bit microcontroller family specification	579
PCD3315	CMOS microcontroller for telephone sets; 160 x 8 RAM; 15K x 8 ROM; –25 to +70 °C	527
PCD3343	microcontroller for telephone sets; 224 x 8 RAM; 3K x 8 ROM; 20 I/O lines; I²C-bus	615
PCD3344	CMOS microcontroller with on-chip DTMF generator; 224 x 8 RAM; 2K x 8 ROM; 20 I/O lines	655
PCD3346	microcontroller for telephone sets; 128 x 8 RAM; 4K x 8 ROM; 256 x 8 EEPROM; 20 I/O lines; I²C-bus	691
PCD3347	CMOS microcontroller with on-chip DTMF generator; 64 x 8 RAM; 1.5K x 8 ROM; 12 I/O lines	741

ICs for Telecom — Functional index

type number	description	page
PCD3348	CMOS microcontroller for telephone sets; 256 x 8 RAM; 8K x 8 ROM; 20 I/O lines; I²C-bus	777
PCD3349	CMOS microcontroller with on-chip DTMF generator; 224 x 8 RAM; 4K x 8 ROM; 20 I/O lines	817
PCF80C552-4	256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; –40 to +85 °C	435
PCF80C562	256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2 pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; –40 to +85 °C	449
PCF80C652	256 x 8 RAM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; –40 to +85 °C	463
PCF80C851	128 x 8 RAM; 256 x 8 EEPROM; 1.2 to 12 MHz; –40 to +85 °C	475
PCF83C552-4	256 x 8 RAM; 8K x 8 ROM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2 pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; –40 to +85 °C	435
PCF83C562	256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2 pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; –40 to +85 °C	449
PCF83C652	256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; –40 to +85 °C	463
PCF83C851	128 x 8 RAM; 4K x 8 ROM; 256 x 8 EEPROM; 1.2 to 12 MHz; –40 to +85 °C	475
PCF84CXXX Family	single-chip 8-bit microcontroller family specification; I²C-bus	1067
PCF84C00	256 x 8 RAM; bond-out version of PCF84CXX family; I²C-bus	1103
PCF84C12	low cost microcontroller; 64 x 8 RAM; 1K x 8 ROM	1111
PCF84C21/C	64 x 8 RAM; 2K x 8 ROM; plus 8-bit LED driver; I²C-bus; –40 to +85 °C	1103
PCF84C22	low cost microcontroller; 64 x 8 RAM; 1K x 8 ROM	1111
PCF84C41/C	128 x 8 RAM; 4K x 8 ROM; plus 8-bit LED driver; I²C-bus; –40 to +85 °C	1103
PCF84C42	low cost microcontroller; 64 x 8 RAM; 4K x 8 ROM	1111
PCF84C81/C	256 x 8 RAM; 8K x 8 ROM; plus 8-bit LED driver; I²C-bus; –40 to +85 °C	1103
PCF84C85	256 x 8 RAM; 8K x 8 ROM; 32 I/O lines; plus 8-bit LED driver; I²C-bus; –40 to +85 °C	1115
PCF84C121	microcontroller; 64 x 8 RAM; 1K x 8 ROM; 8 x 8 EEPROM; 100 kHz to 10 MHz; 13 I/O lines; 8-bit CPU; -40 to +85 °C	1121
PCF84C230	microcontroller; 64 x 8 RAM; 2K x 8 ROM; 8-bit CPU; 12 I/O lines; LCD driver; CMOS; -40 to +85 °C	1127
PCF84C633A	256 x 8 RAM; 6K x 8 ROM; 28 I/O lines; plus LCD driver; derivative port; timer/capture and timer/counter	1133
PCF84C853A	256 x 8 RAM; 8K x 8 ROM; 33 I/O lines; plus LCD driver; derivative port; timer/capture and timer/counter	1139
PCF86C410	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 32 I/O lines; 32 kHz to 16 MHz; 2 x 16-bit timer/event counter; –40 to +85°C; I²C-bus	1257
PCF86C610	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 32 I/O lines; 32 kHz to 16 MHz; 2 x 16-bit timer/event counter; –40 to +85°C; I²C-bus	1257

MIXERS AND OSCILLATORS/IF SYSTEMS

CA3089	FM IF system	39
MC3361	low-power FM IF system	65
NE/SA602	double-balanced mixer and oscillator	161
NE/SA602A	double-balanced mixer and oscillator	167
NE/SA604A	high-performance low-power FM IF system	175
NE/SA605	high-performance low-power mixer FM IF system	185
NE612	double-balanced mixer and oscillator	195
NE614	low-power FM IF system	201
NE/SA614A	low-power FM IF system	211
NE/SA615	high-performance low-power mixer FM IF system	221
TDA1576	FM/IF amplifier and detector	1293

PAGING DECODERS

PCA5000AT	decoder for POCSAG paging systems	359

PAGING RECEIVERS

UAA2033T	low-power digital VHF paging receiver	1535
UAA2050T	low-power digital UHF paging receiver	1543

PHASE-LOCKED LOOPS

NE/SE564	phase-locked loop	73
NE/SE565	0.001 Hz to 500 kHz phase-locked loop	83
NE/SE566	function generator	89
NE/SE567	tone decoder/phase-locked loop	95
NE568	150 MHz phase-locked loop	107
74HC/HCT297	digital phase-locked loop filter	1619
74HC/HCT4046A	phase-locked loop with VCO	1627
74HC/HCT7046A	phase-locked loop with VCO and lock detector	1655

POWER CONTROL ICs

PCF1251	micropower DC voltage detector	1009
PCF1252-X Family	power-fail detector and reset generator; trip voltage = 2.55 to 4.75 V	1013
TEA1081	supply circuit with power-down for telephone set peripherals	1499

SPEECH TRANSMISSION

TEA1060	speech/transmission circuit with dialler interface; low impedance input for dynamic and magnetic microphones	1349
TEA1061	speech/transmission circuit with dialler interface; high impedance input for electret and piezo-eletric microphones	1349
TEA1062	low-voltage speech/transmission circuit with dialler interface for lower performance high volume markets; suitable for parallel operation	1365
TEA1063	low-voltage speech circuit with dialler interface and speech-controlled transmit level dynamic limiting; (special markets)	1385
TEA1064A	speech/transmission circuit with dialler interface and transmit level dynamic limiting	1413
TEA1066T	speech/transmission circuit with dialler interface	1441
TEA1067	low-voltage speech/transmission circuit with dialler interface; input suitable for all microphone types	1459
TEA1068	speech/transmission circuit with dialler interface; input suitable for all microphone types	1479

TONE RINGERS

PCD3360	programmable multi-tone ringer	853

VOICE SYNTHESIZERS

OM8200	speech demonstration board (PCF8200)	333
OM8201	speech demonstration box (PCF8200)	337
OM8209	update package for OM8010	339
OM8210	speech analysis/editing system (PCF8200)	341
PCF8200	voice synthesizer (CMOS); I^2C-bus	1053

NUMERICAL INDEX

type number	description	page
CA3089N	FM IF system	39
FCB61C65 (L/LL)-XXP	8 K x 8 high speed CMOS low-power static RAM; access time = 55 and 70 ns	45
FCB61C65 (L/LL)-XXT	8 K x 8 high speed CMOS low-power static RAM; access time = 55 and 70 ns	45
FCF61C65 (L/LL)-85T	8 K x 8 high speed CMOS low-power static RAM for extended temperature range; access time = 85 ns	55
MC3361D	low-power FM IF system	65
MC3361N	low-power FM IF system	65
NE542N	dual low-noise preamplifier	69
NE564D	phase-locked loop	73
NE564N	phase-locked loop	73
NE565D	0.001 Hz to 500 kHz phase-locked loop	83
NE565F	0.001 Hz to 500 kHz phase-locked loop	83
NE565N	0.001 Hz to 500 kHz phase-locked loop	83
NE566D	function generator	89
NE566F	function generator	89
NE566N	function generator	89
NE567D	tone decoder/phase-locked loop	95
NE567F	tone decoder/phase-locked loop	95
NE567FE	tone decoder/phase-locked loop	95
NE567N	tone decoder/phase-locked loop	95
NE568D	150 MHz phase-locked loop	107
NE568N	150 MHz phase-locked loop	107
NE570F	compandor	113
NE570N	compandor	113
NE571D	compandor	113
NE571F	compandor	113
NE571N	compandor	113
NE572D	programmable analog compandor	123
NE572N	programmable analog compandor	123
NE575D	low-voltage compandor	131
NE575N	low-voltage compandor	131
NE575DJ	low-voltage compandor in very small outline package (VSOP)	143
NE577D	unity gain level programmable low-power compandor	153
NE577N	unity gain level programmable low-power compandor	153
NE578D	unity gain level programmable low-power compandor	157
NE578N	unity gain level programmable low-power compandor	157
NE602D	double-balanced mixer and oscillator	161
NE602N	double-balanced mixer and oscillator	161
NE602FE	double-balanced mixer and oscillator	161
NE602AD	double-balanced mixer and oscillator	167
NE602AN	double-balanced mixer and oscillator	167
NE602AFE	double-balanced mixer and oscillator	167
NE604AD	high-performance low-power FM IF system	175
NE604AN	high-performance low-power FM IF system	175
NE605D	high-performance low-power mixer FM IF system	185

type number	description	page
NE605N	high-performance low-power mixer FM IF system	185
NE612D	double-balanced mixer and oscillator	195
NE612N	double-balanced mixer and oscillator	195
NE614D	low-power FM IF system	201
NE614N	low-power FM IF system	201
NE614AD	low-power FM IF system	211
NE614AN	low-power FM IF system	211
NE615D	high-performance low-power mixer FM IF system	221
NE615N	high-performance low-power mixer FM IF system	221
NE5204D	wideband high-frequency amplifier	231
NE5204N	wideband high-frequency amplifier	231
NE5205D	wideband high-frequency amplifier	241
NE5205EC	wideband high-frequency amplifier	241
NE5205FE	wideband high-frequency amplifier	241
NE5205N	wideband high-frequency amplifier	241
NE5209D	wideband variable gain amplifier	253
NE5209N	wideband variable gain amplifier	253
NE5230D	low-voltage operational amplifier	267
NE5230FE	low-voltage operational amplifier	267
NE5230N	low-voltage operational amplifier	267
NE5234D	matched quad high-performance low-voltage operational amplifier	279
NE5234N	matched quad high-performance low-voltage operational amplifier	279
NE5539D	high-frequency operational amplifier	285
NE5539F	high-frequency operational amplifier	285
NE5539N	high-frequency operational amplifier	285
NE5750D	audio processor - companding and amplifier section	293
NE5750N	audio processor - companding and amplifier section	293
NE5751D	audio processor - filter and control section	301
NE5751N	audio processor - filter and control section	301
NE5900D	call progress decoder	311
NE5900N	call progress decoder	311
OM1036CP	dialler circuit with redial	319
OM8200	speech demonstration board (PCF8200)	333
OM8201	speech demonstration box (PCF8200)	337
OM8209	update package for OM8010	339
OM8210	speech analysis/editing system (PCF8200)	341
PCA5000AT	decoder for POCSAG paging systems	359
PCA80C552-4WP	256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 10-bit ADC with 8	435
PCA80C552-4H	256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I^2C-bus; −40 to +125 °C	435
PCA80C562WP	256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I^2C-bus; −40 to +125 °C	449

type number	description	page
PCA80C562H	256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; –40 to +125 °C	449
PCA80C652P	256 x 8 RAM; serial I/O; UART; 1.2 to 12 MHz; I²C-bus; –40 to +125 °C	463
PCA80C652WP	256 x 8 RAM; serial I/O; UART; 1.2 to 12 MHz; I²C-bus; –40 to +125 °C	463
PCA80C652H	256 x 8 RAM; serial I/O; UART; 1.2 to 12 MHz; I²C-bus; –40 to +125 °C	463
PCA83C552-4WP	256 x 8 RAM; 4K x 8 ROM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; –40 to +125 °C	435
PCA83C552-4H	256 x 8 RAM; 4K x 8 ROM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; –40 to +125 °C	435
PCA83C562H	256 x 8 RAM; 8K x 8 ROM; 80C531 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; –40 to +125 °C	449
PCA83C562WP	256 x 8 RAM; 8K x 8 ROM; 80C531 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; –40 to +125 °C	449
PCA83C652P	256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; 1.2 to 12 MHz; I²C-bus; –40 to +125 °C	463
PCA83C652H	256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; 1.2 to 12 MHz; I²C-bus; –40 to +125 °C	463
PCA83C652WP	256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; 1.2 to 12 MHz; I²C-bus; –40 to +125 °C	463
PCA8582BP	256 x 8-bit static EEPROM; CMOS; I²C-bus; for automotive applications	345
PCA8582BT	256 x 8-bit static EEPROM; CMOS; I²C-bus; for automotive applications	345
PCB5010WP-8	single-chip digital signal processor	379
PCB5011YC-8	ROM-less version of PCB5010	379
PCB80C552-4WP	256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; 0 to +70 °C	435
PCB80C552-4H	256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; 0 to +70 °C	435
PCB80C562WP	256 x 8 RAM; 80C531 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; –40 to +125 °C	449
PCB80C562H	256 x 8 RAM; 80C531 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; –40 to +125 °C	449
PCB80C652P	256 x 8 RAM; serial I/O; UART; 1.2 to 12 MHz; I²C-bus; 0 to +70 °C	463
PCB80C652H	256 x 8 RAM; serial I/O; UART; 1.2 to 12 MHz; I²C-bus; 0 to +70 °C	463
PCB80C652WP	256 x 8 RAM; serial I/O; UART; 1.2 to 12 MHz; I²C-bus; 0 to +70 °C	463
PCB80C851P	128 x 8 RAM; 256 x 8 EEPROM; 1.2 to 12 MHz; I²C-bus; 0 to +70 °C; special security mode	475
PCB80C851H	128 x 8 RAM; 256 x 8 EEPROM; 1.2 to 12 MHz; I²C-bus; 0 to +70 °C; special security mode	475

ICs for Telecom — Numerical index

type number	description	page
PCB80C851WP	128 x 8 RAM; 256 x 8 EEPROM; 1.2 to 12 MHz; I²C-bus; 0 to +70 °C; special security mode	475
PCB83C552-4WP	256 x 8 RAM; 8K x 8 ROM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; 0 to +70 °C	435
PCB83C552-4H	256 x 8 RAM; 8K x 8 ROM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; 0 to +70 °C	435
PCB83C562H	256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; −40 to +125 °C	449
PCB83C562WP	256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; −40 to +125 °C	449
PCB83C652P	256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; 1.2 to 12 MHz; I²C-bus; 0 to +70 °C	463
PCB83C652H	256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; 1.2 to 12 MHz; I²C-bus; 0 to +70 °C	463
PCB83C652WP	256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; 1.2 to 12 MHz; I²C-bus; 0 to +70 °C	463
PCB83C851P	128 x 8 RAM; 4K X 8 ROM; 256 x 8 EEPROM; 1.2 to 12 MHz; I²C-bus; 0 to +70 °C; special security mode	475
PCB83C851H	128 x 8 RAM; 4K X 8 ROM; 256 x 8 EEPROM; 1.2 to 12 MHz; I²C-bus; 0 to +70 °C; special security mode	475
PCB83C851WP	128 x 8 RAM; 4K X 8 ROM; 256 x 8 EEPROM; 1.2 to 12 MHz; I²C-bus; 0 to +70 °C; special security mode	475
PCD3310P	pulse and DTMF dialler with redial; pulse dialling mark/space ratio 2:1; PABX register; notepad; flash; access pause by cursor method	485
PCD3310T	pulse and DTMF dialler with redial; pulse dialling mark/space ratio 2:1; PABX register; notepad; flash; access pause by cursor method	485
PCD3310AP	variant of PCD3310 with markspace ratio 3:2	485
PCD3310AT	variant of PCD3310 with markspace ratio 3:2	485
PCD3310CP	variant of PCD3310; dialling mode indicator output	485
PCD3310CT	variant of PCD3310; dialling mode indicator output	485
PCD3310EP	PCD3310 with 20 Hz dialling frequency	485
PCD3310ET	PCD3310 with 20 Hz dialling frequency	485
PCD3310FP	PCD3310 with DTMF 60/90 ms tone burst	485
PCD3310FT	PCD3310 with DTMF 60/90 ms tone burst	485
PCD3310GP	PCD3310 with pulse/DTMF switching	485
PCD3310GT	PCD3310 with pulse/DTMF switching	485
PCD3310HP	PCD3310 with pulse/DTMF switching	485
PCD3311CP	DTMF/modem/music tone generators with binary-coded parallel input or serial data input; I²C-bus	509
PCD3311CT	DTMF/modem/music tone generators with binary-coded parallel input or serial data input; I²C-bus	509

type number	description	page
PCD3312CP	DTMF/modem/music tone generators with binary-coded parallel input or serial data input; I²C-bus	509
PCD3312CT	DTMF/modem/music tone generators with binary-coded parallel input or serial data input; I²C-bus	509
PCD3315P	CMOS microcontroller for telephone sets; 160 x 8 RAM; 15K x 8 ROM; –25 to +70 °C	527
PCD3315T	CMOS microcontroller for telephone sets; 160 x 8 RAM; 15K x 8 ROM; –25 to +70 °C	527
PCD3320CD	dialler with redial; several mute signals; no access pause; mark/space ratio 3:2	531
PCD3320CP	dialler with redial; several mute signals; no access pause; mark/space ratio 3:2	531
PCD3321CD	dialler with redial; manual and two automatic access pauses; mark/space ratios 3:2 and 2:1	531
PCD3321CP	dialler with redial; manual and two automatic access pauses; mark/space ratios 3:2 and 2:1	531
PCD3321CT	dialler with redial; manual and two automatic access pauses; mark/space ratios 3:2 and 2:1	531
PCD3322CP	variant of PCD3320C	531
PCD3322CT	variant of PCD3320C	531
PCD3324CP	dialler with one automatic access pause; variant of PCD3321C	531
PCD3325CP	dialler with manual access pause control	531
PCD3326CP	variant of PCD3321C wiht selectable access pause	531
PCD3327CP	variant of PCD3325C for ceramic resonator; automatic reset of access pause	531
PCD3327CT	variant of PCD3325C for ceramic resonator; automatic reset of access pause	531
PCD3327U	variant of PCD3325C for ceramic resonator; automatic reset of access pause	531
PCD3341P	advanced 10-100-number repertory pulse/DTMF dialler; LCD control; I²C-bus	561
PCD3341T	advanced 10-100-number repertory pulse/DTMF dialler; LCD control; I²C-bus	561
PCD33XX Family	single-chip 8-bit microcontroller family specification	579
PCD3343P	CMOS microcontroller for telephone sets; 224 x 8 RAM; 3K x 8 ROM; 20 I/O lines; I²C-bus	615
PCD3343T	CMOS microcontroller for telephone sets; 224 x 8 RAM; 3K x 8 ROM; 20 I/O lines; I²C-bus	615
PCD3344P	CMOS microcontroller with on-chip DTMF generator; 224 x 8 RAM; 2K x 8 ROM; 20 I/O lines	655
PCD3344T	CMOS microcontroller with on-chip DTMF generator; 224 x 8 RAM; 2K x 8 ROM; 20 I/O lines	655
PCD3346P	microcontroller for telephone sets; 128 x 8 RAM; 4K x 8 ROM; 256 x 8 EEPROM; 20 I/O lines; I²C-bus	691
PCD3346T	microcontroller for telephone sets; 128 x 8 RAM; 4K x 8 ROM; 256 x 8 EEPROM; 20 I/O lines; I²C-bus	691
PCD3347P	CMOS microcontroller with on-chip DTMF generator; 64 x 4 RAM; 1.5K x 8 ROM; 12 I/O lines	741
PCD3347T	CMOS microcontroller with on-chip DTMF generator; 64 x 4 RAM; 1.5K x 8 ROM; 12 I/O lines	741
PCD3348P	CMOS microcontroller for telephone sets; 256 x 8 RAM; 8K x 8 ROM; 20 I/O lines; I²C-bus	777
PCD3348T	CMOS microcontroller for telephone sets; 256 x 8 RAM; 8K x 8 ROM; 20 I/O lines; I²C-bus	777

ICs for Telecom — Numerical index

type number	description	page
PCD3349P	CMOS microcontroller with on-chip DTMF generator; 224 x 8 RAM; 4K x 8 ROM; 20 I/O lines	817
PCD3349T	CMOS microcontroller with on-chip DTMF generator; 224 x 8 RAM; 4K x 8 ROM; 20 I/O lines	817
PCD3360P	programmable multi-tone ringer	853
PCD3360T	programmable multi-tone ringer	853
PCD4410	pulse and DTMF dialler with redial; manual access pause; 3 x 4 keypad plus flash; mark/space ratio 2:1; tone burst 70/140 ms; data memory	867
PCD4413	pulse and DTMF dialler; variant of PCD4410 without redial; mark/space ratio 3:2; tone burst 70/70 ms	883
PCD4413A	PCD4413 with flash of 255 ms	923
PCD4415P	PCD4410 with 3 x 4 or 3 x 5 keypad; tone burst 70/70 ms	937
PCD4415T	PCD4410 with 3 x 4 or 3 x 5 keypad; tone burst 70/70 ms	937
PCD4415AP	PCD4415 with mark/space ratio of 3:2	957
PCD4415AT	PCD4415 with mark/space ratio of 3:2	957
PCD4420P	pulse and DTMF dialler with redial for 4 x 4 keypad	977
PCD4420T	pulse and DTMF dialler with redial for 4 x 4 keypad	977
PCD4421P	pulse and DTMF dialler with redial for 4 x 5 keypad	987
PCD4421T	pulse and DTMF dialler with redial for 4 x 5 keypad	987
PCD5101P	256 x 4-bit static RAM	997
PCD5101T	256 x 4-bit static RAM	997
PCD5114D	1024 x 4-bit static RAM	1003
PCD5114P	1024 x 4-bit static RAM	1003
PCD5114T	1024 x 4-bit static RAM	1003
PCD8582DP	256 x 8-bit static EEPROM; CMOS; I^2C-bus	345
PCD8582DT	256 x 8-bit static EEPROM; CMOS; I^2C-bus	345
PCF1251P	micropower DC voltage detector	1009
PCF1251T	micropower DC voltage detector	1009
PCF1252-0P	power fail detector and reset generator; trip voltage = 4.75 V	1013
PCF1252-0T	power fail detector and reset generator; trip voltage = 4.75 V	1013
PCF1252-1P	power fail detector and reset generator; trip voltage = 4.55 V	1013
PCF1252-1T	power fail detector and reset generator; trip voltage = 4.55 V	1013
PCF1252-2P	power fail detector and reset generator; trip voltage = 4.25 V	1013
PCF1252-2T	power fail detector and reset generator; trip voltage = 4.25 V	1013
CF1252-3P	power fail detector and reset generator; trip voltage = 4.05 V	1013
PCF1252-3T	power fail detector and reset generator; trip voltage = 4.05 V	1013
PCF1252-4P	power fail detector and reset generator; trip voltage = 3.75 V	1013
PCF1252-4T	power fail detector and reset generator; trip voltage = 3.75 V	1013
PCF1252-5P	power fail detector and reset generator; trip voltage = 3.55 V	1013
PCF1252-5T	power fail detector and reset generator; trip voltage = 3.55 V	1013
PCF1252-6P	power fail detector and reset generator; trip voltage = 3.25 V	1013
PCF1252-6T	power fail detector and reset generator; trip voltage = 3.25 V	1013
PCF1252-7P	power fail detector and reset generator; trip voltage = 3.05 V	1013
PCF1252-7T	power fail detector and reset generator; trip voltage = 3.05 V	1013

type number	description	page
PCF1252-8P	power fail detector and reset generator; trip voltage = 2.75 V	1013
PCF1252-8T	power fail detector and reset generator; trip voltage = 2.75 V	1013
PCF1252-9P	power fail detector and reset generator; trip voltage = 2.55 V	1013
PCF1252-9T	power fail detector and reset generator; trip voltage = 2.55 V	1013
PCF2100P	LCD duplex driver; 40 segments	1025
PCF2100T	LCD duplex driver; 40 segments	1025
PCF2110P	LCD duplex driver; 60 segments and 2 LEDs	1025
PCF2110T	LCD duplex driver; 60 segments and 2 LEDs	1025
PCF2111P	LCD duplex driver; 64 segments	1025
PCF2111T	LCD duplex driver; 64 segments	1025
PCF2112P	LCD driver; 32 segments	1025
PCF2112T	LCD driver; 32 segments	1025
PCF2201V	LCD flat-panel row/column driver	1041
PCF5010WP-8	single-chip digital signal processor	379
PCF5011YC-8	ROM-less version of PCB5010	379
PCF80C552-4H	256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; −40 to +85 °C	435
PCF80C552-4WP	256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; −40 to +85 °C	435
PCF80C562H	256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; −40 to +85 °C	449
PCF80C562WP	256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; −40 to +85 °C	449
PCF80C652H	256 x 8 RAM; serial I/O; UART; 1.2 to 12 MHz; I²C-bus; −40 to +85 °C	463
PCF80C652P	256 x 8 RAM; serial I/O; UART; 1.2 to 12 MHz; I²C-bus; −40 to +85 °C	463
PCF80C652WP	256 x 8 RAM; serial I/O; UART; 1.2 to 12 MHz; I²C-bus; −40 to +85 °C	463
PCF80C851H	128 x 8 RAM; 256 x 8 EEPROM; 1.2 to 12 MHz; −40 to +85 °C	475
PCF80C851P	128 x 8 RAM; 256 x 8 EEPROM; 1.2 to 12 MHz; −40 to +85 °C	475
PCF80C851WP	128 x 8 RAM; 256 x 8 EEPROM; 1.2 to 12 MHz; −40 to +85 °C	475
PCF8200	voice synthesizer (CMOS); I²C-bus	1053
PCF83C552-4H	256 x 8 RAM; 8K x 8 ROM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; −40 to +85 °C	435
PCF83C552-4WP	256 x 8 RAM; 8K x 8 ROM; 80C31 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; −40 to +85 °C	435
PCF83C562H	256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; −40 to +85 °C	449
PCF83C562WP	256 x 8 RAM; 8K x 8 ROM; 80C51 CPU plus 16-bit capture/compare timer/counter; watchdog timer; 2-pulse-width modulated signals; 8-bit ADC with 8 multiplexed input lines; 1.2 to 12 MHz; I²C-bus; −40 to +85 °C	449

ICs for Telecom — Numerical index

type number	description	page
PCF83C652H	256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; 1.2 to 12 MHz; I²C-bus; –40 to +85 °C	463
PCF83C652P	256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; 1.2 to 12 MHz; I²C-bus; –40 to +85 °C	463
PCF83C652WP	256 x 8 RAM; 8K x 8 ROM; serial I/O; UART; 1.2 to 12 MHz; I²C-bus; –40 to +85 °C	463
PCF83C851H	128 x 8 RAM; 4K x 8 ROM; 256 x 8 EEPROM; 1.2 to 12 MHz; -40 to +85 °C	475
PCF83C851P	128 x 8 RAM; 4K x 8 ROM; 256 x 8 EEPROM; 1.2 to 12 MHz; -40 to +85 °C	475
PCF83C851WP	128 x 8 RAM; 4K x 8 ROM; 256 x 8 EEPROM; 1.2 to 12 MHz; -40 to +85 °C	475
PCF84CXXX Family	single-chip 8-bit microcontroller family specification	1067
PCF84C00B	256 x 8 RAM; bond-out version of PCF84CXX family; I²C-bus	1103
PCF84C00T	256 x 8 RAM; bond-out version of PCF84CXX family; I²C-bus	1103
PCF84C12P	low cost microcontroller; 64 x 8 RAM; 1K x 8 ROM	1111
PCF84C12T	low cost microcontroller; 64 x 8 RAM; 1K x 8 ROM	1111
PCF84C21CP	64 x 8 RAM; 2K x 8 ROM; plus 8-bit LED driver; I²C-bus; –40 to +85 °C	1103
PCF84C21CT	64 x 8 RAM; 2K x 8 ROM; plus 8-bit LED driver; I²C-bus; –40 to +85 °C	1103
PCF84C22P	low cost microcontroller; 64 x 8 RAM; 1K x 8 ROM	1111
PCF84C22T	low cost microcontroller; 64 x 8 RAM; 1K x 8 ROM	1111
PCF84C41CP	128 x 8 RAM; 4K x 8 ROM; plus 8-bit LED driver; I²C-bus; –40 to +85 °C	1103
PCF84C41CT	128 x 8 RAM; 4K x 8 ROM; plus 8-bit LED driver; I²C-bus; –40 to +85 °C	1103
PCF84C42P	low cost microcontroller; 64 x 8 RAM; 4K x 8 ROM	1111
PCF84C42T	low cost microcontroller; 64 x 8 RAM; 4K x 8 ROM	1111
PCF84C81CP	256 x 8 RAM; 8K x 8 ROM; plus 8-bit LED driver; I²C-bus; –40 to +85 °C	1103
PCF84C81CT	256 x 8 RAM; 8K x 8 ROM; plus 8-bit LED driver; I²C-bus; –40 to +85 °C	1103
PCF84C85P	256 x 8 RAM; 8K x 8 ROM; 32 I/O lines; plus 8-bit LED driver; I²C-bus; –40 to +85 °C	1115
PCF84C85T	256 x 8 RAM; 8K x 8 ROM; 32 I/O lines; plus 8-bit LED driver; I²C-bus; –40 to +85 °C	1115
PCF84C121P	microcontroller; 64 x 8 RAM; 1K x 8 ROM; 8 x 8 EEPROM; 100 kHz to 10 MHz; 13 I/O lines; 8-bit CPU; –40 to +85 °C	1121
PCF84C121T	microcontroller; 64 x 8 RAM; 1K x 8 ROM; 8 x 8 EEPROM; 100 kHz to 10 MHz; 13 I/O lines; 8-bit CPU; –40 to +85 °C	1121
PCF84C230P	microcontroller; 64 x 8 RAM; 2K x 8 ROM; 8-bit CPU; 12 I/O lines; LCD driver; (CMOS); –40 to +85 °C	1127
PCF84C230T	microcontroller; 64 x 8 RAM; 2K x 8 ROM; 8-bit CPU; 12 I/O lines; LCD driver; (CMOS); –40 to +85 °C	1127
PCF84C633AT	256 x 8 RAM; 6K x 8 ROM; 28 I/O lines; plus LCD driver; derivative port; timer/capture and timer/ counter	1133
PCF84C853AP	256 x 8 RAM; 8K x 8 ROM; 33 I/O lines; plus LCD driver; derivative port; timer/capture and timer/ counter	1139
PCF84C853AT	256 x 8 RAM; 8K x 8 ROM; 33 I/O lines; plus LCD driver; derivative port; timer/capture and timer/ counter	1139
PCF8566P	univeral LCD driver for low multiplex rates (1:1 to 1:4) max. 96 segments; I²C-bus	1145
PCF8566T	univeral LCD driver for low multiplex rates (1:1 to 1:4) max. 96 segments; I²C-bus	1145
PCF8569T	LCD column driver for dot matrix graphic displays at multiplex rates of 1:8 or 1:16; 40 outputs; I²C-bus	1151
PCF8569V	LCD column driver for dot matrix graphic displays at multiplex rates of 1:8 or 1:16; 40 outputs; I²C-bus	1151
PCF8570P	256 x 8-bit static RAM; I²C-bus	1159

ICs for Telecom — Numerical index

type number	description	page
PCF8570T	256 x 8-bit static RAM; I²C-bus	1159
PCF8570CP	256 x 8-bit static RAM; I²C-bus; different slave address	1159
PCF8570CT	256 x 8-bit static RAM; I²C-bus; different slave address	1159
PCF8571P	128 x 8-bit static RAM; I²C-bus	1159
PCF8571T	128 x 8-bit static RAM; I²C-bus	1159
PCF8573P	clock/calender with serial I/O; I²C-bus	1163
PCF8573T	clock/calender with serial I/O; I²C-bus	1163
PCF8574P	remote 8-bit I/O expander; I²C-bus	1179
PCF8574T	remote 8-bit I/O expander; I²C-bus	1179
PCF8574AP	remote 8-bit I/O expander; I²C-bus; different slave address	1179
PCF8574AT	remote 8-bit I/O expander; I²C-bus; different slave address	1179
PCF8576T	univeral LCD driver for low multiplex rates (1:1 to 1:4) max. 160 segments; I²C-bus	1191
PCF8576U	univeral LCD driver for low multiplex rates (1:1 to 1:4) max. 160 segments; I²C-bus	1191
PCF8576U/10	univeral LCD driver for low multiplex rates (1:1 to 1:4) max. 160 segments; I²C-bus	1191
PCF8576V	univeral LCD driver for low multiplex rates (1:1 to 1:4) max. 160 segments; I²C-bus	1191
PCF8577P	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	1201
PCF8577T	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	1201
PCF8577AP	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	1201
PCF8577AT	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	1201
PCF8577CP	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	1201
PCF8577CT	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	1201
PCF8577CAP	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	1201
PCF8577CAT	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	1201
PCF8577U/5	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	1201
PCF8577CU/5	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	1201
PCF8577U/10	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	1201
PCF8577CU/10	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	1201
PCF8578T	LCD row/column driver for dot matrix graphic displays; 40 outputs (24 are programmable); I²C-bus	1209
PCF8578U	LCD row/column driver for dot matrix graphic displays; 40 outputs (24 are programmable); I²C-bus	1209
PCF8578V	LCD row/column driver for dot matrix graphic displays; 40 outputs (24 are programmable); I²C-bus	1209
PCF8579T	LCD column driver for dot matrix graphic displays; 40 column outputs; I²C-bus	1219
PCF8579U	LCD column driver for dot matrix graphic displays; 40 column outputs; I²C-bus	1219
PCF8579V	LCD column driver for dot matrix graphic displays; 40 column outputs; I²C-bus	1219
PCF8581P	128 x 8-bit static EEPROM; low-voltage; I²C-bus	1229
PCF8581T	128 x 8-bit static EEPROM; low-voltage; I²C-bus	1229

PCF8581CP	128 x 8-bit static EEPROM; low-voltage; I²C-bus	1229
PCF8581CT	128 x 8-bit static EEPROM; low-voltage; I²C-bus	1229
PCF8582AP	256 x 8-bit static EEPROM; CMOS; I²C-bus	345
PCF8582AT	256 x 8-bit static EEPROM; CMOS; I²C-bus	345
PCF8582CP	256 x 8-bit static EEPROM; CMOS; I²C-bus ; for automotive applications	345
PCF8582CT	256 x 8-bit static EEPROM; CMOS; I²C-bus ; for automotive applications	345
PCF8582EP	256 x 8-bit static EEPROM; CMOS; I²C-bus ; for automotive applications	345
PCF8582ET	256 x 8-bit static EEPROM; CMOS; I²C-bus ; for automotive applications	345
PCF8583P	clock/calender with 256 x 8-bit static RAM; I²C-bus	1233
PCF8583T	clock/calender with 256 x 8-bit static RAM; I²C-bus	1233
PCF8591P	8-bit ADC/DAC; I²C-bus	1239
PCF8591T	8-bit ADC/DAC; I²C-bus	1239
PCF86C410P	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 32 I/O lines; 32 kHz to 16 MHz; 2 x 16-bit timer/event counter; –40 to +85 °C; I²C-bus	1257
PCF86C410T	microcontroller; 128 x 8 RAM; 4K x 8 ROM; 32 I/O lines; 32 kHz to 16 MHz; 2 x 16-bit timer/event counter; –40 to +85 °C; I²C-bus	1257
PCF68C610P	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 32 I/O lines; 32 kHz to 16 MHz; 2 x 16-bit timer/event counter; –40 to +85 °C; I²C-bus	1257
PCF68C610T	microcontroller; 256 x 8 RAM; 8K x 8 ROM; 32 I/O lines; 32 kHz to 16 MHz; 2 x 16-bit timer/event counter; –40 to +85 °C; I²C-bus	1257
SA571F	compandor	113
SA571N	compandor	113
SA572D	programmable analog compandor	123
SA572F	programmable analog compandor	123
SA572N	programmable analog compandor	123
SA575D	low-voltage compandor	131
SA575N	low-voltage compandor	131
SA575DJ	low-voltage compandor in very small outline package (VSOP)	143
SA577D	unity gain level programmable low-power compandor	153
SA577N	unity gain level programmable low-power compandor	153
SA578D	unity gain level programmable low-power compandor	157
SA578N	unity gain level programmable low-power compandor	157
SA602D	double-balanced mixer and oscillator	161
SA602FE	double-balanced mixer and oscillator	161
SA602N	double-balanced mixer and oscillator	161
SA602AD	double-balanced mixer and oscillator	167
SA602AFE	double-balanced mixer and oscillator	167
SA602AN	double-balanced mixer and oscillator	167
SA604AD	high-performance low-power FM IF system	175
SA604AN	high-performance low-power FM IF system	175
SA605D	high-performance low-power mixer FM IF system	185
SA605N	high-performance low-power mixer FM IF system	185
SA614AD	low-power FM IF system	211
SA614AN	low-power FM IF system	211
SA615D	high-performance low-power mixer FM IF system	221
SA615N	high-performance low-power mixer FM IF system	221
SA5204D	wideband high-frequency amplifier	231
SA5204N	wideband high-frequency amplifier	231
SA5205D	wideband high-frequency amplifier	241

SA5205FE	wideband high-frequency amplifier	241
SA5205N	wideband high-frequency amplifier	241
SA5209D	wideband variable gain amplifier	253
SA5209N	wideband variable gain amplifier	253
SA5230D	low-voltage operational amplifier	259
SA5230FE	low-voltage operational amplifier	259
SA5230N	low-voltage operational amplifier	259
SA5234D	matched quad high-performance low-voltage operational amplifier	279
SA5234N	matched quad high-performance low-voltage operational amplifier	279
SA5750D	audio processor - companding and amplifier section	293
SA5750N	audio processor - companding and amplifier section	293
SA5751D	audio processor - filter and control section	301
SA5751N	audio processor - filter and control section	301
SE564F	phase-locked loop	73
SE564N	phase-locked loop	73
SE565F	0.001 Hz to 500 kHz phase-locked loop	83
SE565N	0.001 Hz to 500 kHz phase-locked loop	83
SE566F	function generator	89
SE566N	function generator	89
SE567F	tone decoder/phase-locked loop	95
SE567FE	tone decoder/phase-locked loop	95
SE567N	tone decoder/phase-locked loop	95
SE5205FE	wideband high-frequency amplifier	241
SE5205N	wideband high-frequency amplifier	241
SE5539F	high-frequency operational amplifier	285
SE5539N	high-frequency operational amplifier	285
TDA1011	2 to 6 W audio power amplifier	1267
TDA1011A	2 to 6 W audio power amplifier	1279
TDA1015T	0.5 W audio power amplifier	1287
TDA1576	FM/IF amplifier and detector	1293
TDA7050	140 mW BTL or 2 x 75 mW mono/stereo audio power amplifier; low-voltage (in plastic DIL8)	1305
TDA7050T	140 mW BTL or 2 x 75 mW mono/stereo audio power amplifier; low-voltage (in SO8 plastic mini-pack)	1309
TDA7052	1 W BTL mono audio amplifier	1313
TDA7053	2 x 1 W BTL portable/mains-fed stereo power amplifier	1319
TDD1742T	low-power frequency synthesizer (LOPSY)	1327
TEA1060	speech/transmission circuit with dialler interface; low impedance input for dynamic and magnetic microphones	1349
TEA1061	speech/transmission circuit with dialler interface; high impedance input for electret and piezo-electric microphones	1349
TEA1062P	low-voltage speech/transmission circuit with dialler interface for lower performance high volume markets; suitable for parallel operation	1365
TEA1062T	low-voltage speech/transmission circuit with dialler interface for lower performance high volume markets; suitable for parallel operation	1365
TEA1063P	low-voltage speech circuit with dialler interface and speech-controlled transmit level dynamic limiting; (special markets)	1385

TEA1063T	low-voltage speech circuit with dialler interface and speech-controlled transmit level dynamic limiting; (special markets)	1385
TEA1064AP	speech/transmission circuit with dialler interface and transmit level dynamic limiting	1413
TEA1064AT	speech/transmission circuit with dialler interface and transmit level dynamic limiting	1413
TEA1066T	speech/transmission circuit with dialler interface	1441
TEA1067P	low-voltage speech/transmission circuit with dialler interface; input suitable for all microphone types	1459
TEA1067T	low-voltage speech/transmission circuit with dialler interface; input suitable for all microphone types	1459
TEA1068P	speech/transmission circuit with dialler interface; input suitable for all microphone types	1479
TEA1068T	speech/transmission circuit with dialler interface; input suitable for all microphone types	1479
TEA1081P	supply circuit with power-down for telephone set peripherals	1499
TEA1081T	supply circuit with power-down for telephone set peripherals	1499
TEA1085P	listening-in circuit for line-powered telephone sets; with anti-Larson limiter	1509
TEA1085T	listening-in circuit for line-powered telephone sets; with anti-Larson limiter	1509
UAA2033T	low-power digital VHF paging receiver	1535
UAA2050T	low-power digital UHF paging receiver	1543
UMA1000T	data processor for AMPS/TACS cellular radio (DPROC); I^2C-bus	1561
UMA1010T	low-power universal frequency synthesizer for radio communiations; 400 MHz to 1150 MHz; I^2C-bus	1591
UMA1012T	low-power universal synthesizer for radio communiations; 20 to 600 MHz; I^2C-bus	1605
74HC/HCT297P	digital phase-locked loop filter	1619
74HC/HCT297T	digital phase-locked loop filter	1619
74HC/HCT4046AP	phase-locked loop with VCO	1627
74HC/HCT4046AT	phase-locked loop with VCO	1627
74HC/HCT7046AP	phase-locked loop with VCO and lock detector	1655
74HC/HCT7046AT	phase-locked loop with VCO and lock detector	1655

DEVICE DATA

PULSE AND DTMF DIALLER

GENERAL DESCRIPTION

The PCD4413A is a single-chip silicon gate CMOS integrated circuit with an on-chip oscillator for a 3,58 MHz crystal. It is a dual-standard dialling circuit for either pulse dialling (PD) or dual tone multi-frequency (DTMF) dialling.

Input data is derived from any standard matrix keyboard for dialling in either PD or DTMF mode.

In DTMF mode bursts as well as pauses are timed to a minimum, in manual dialling the maximum depends on the key depression time.

Features

- Pulse and DTMF dialling
- 23-digit memory capacity
- Three dialling modes; pulse, DTMF and data transmission (DTMF)
- Two function keys; * and FL (flash)
- DTMF timing:
  manual dialling — minimum duration for bursts and pauses
- On-chip voltage reference for supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT CS 203 compatible)
- On-chip oscillator uses low-cost 3,58 MHz (tv colour burst) crystal
- Uses standard single-contact or double-contact (common left open) keyboard
- Keyboard entries fully debounced
- Flash (register recall) output

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}	2,5 to 6,0	V
Standby supply voltage	V_{DDO}	1,8 to 6,0	V
Low standby current (on hook) at V_{DDO} = 1,8 V	I_{DDO}	max. 5	μA
Operating currents			
conversation mode	I_{DDC}	max. 150	μA
pulse dialling mode	I_{DDP}	max. 200	μA
DTMF dialling mode	I_{DDF}	max. 0,9	mA
DTMF output voltage level (r.m.s. values)			
HIGH group	$V_{HG(rms)}$	typ. 192	mV
LOW group	$V_{LG(rms)}$	typ. 150	mV
Pre-emphasis of group	ΔV_G	typ. 2,1	dB
Total harmonic distortion	THD	−25	dB
Operating ambient temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102G,N,PE).

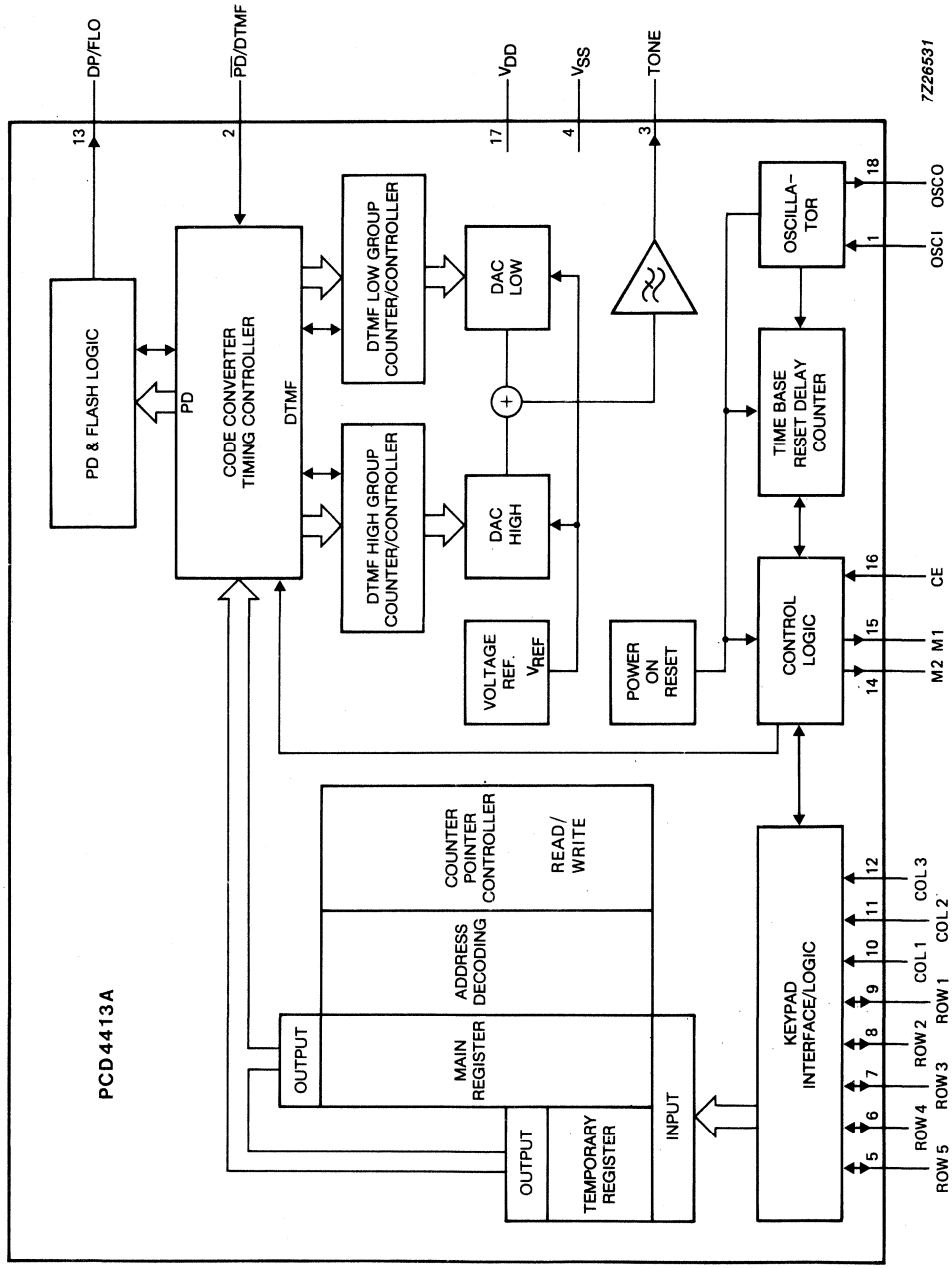


Fig. 1 Block diagram.

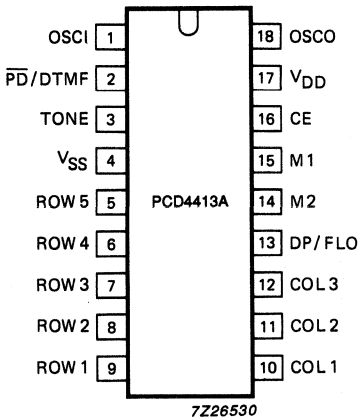


Fig. 2 Pinning diagram.

PINNING

1	OSCI	oscillator input
2	$\overline{PD}$/DTMF	select pin; pulse or DTMF dialling
3	TONE	single or dual tone frequency output
4	V_{SS}	negative supply
5	ROW 5	scanning row keyboard input/outputs
6	ROW 4	
7	ROW 3	
8	ROW 2	
9	ROW 1	
10	COL 1	sense column keyboard inputs with internal pull-ups
11	COL 2	
12	COL 3	
13	DP/FLO	dialling pulse and flash output
14	M2	strobe; active HIGH during transmission
15	M1	muting output
16	CE	chip enable input
17	V_{DD}	positive supply
18	OSCO	oscillator output

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The positive supply of the circuit (V_{DD}) must meet the voltage requirements as indicated in the characteristics.
To avoid undefined states of the device when powered-on, an internal reset circuit clears the control logic and counters.

The power-on-reset signal has the highest priority. It blocks and resets the complete circuit without delay regardless of the state of chip enable input (CE).

Clock oscillator (OSCI, OSCO)

The time base for the PCD4413A for both PD and DTMF modes is a crystal controlled on-chip oscillator which is completed by connecting a 3,58 MHz crystal between the OSCI and OSCO pins.

Chip Enable (CE)

The CE input enables the circuit and is used to initialize the IC.

CE = LOW provides the static standby condition. In this state the clock oscillator is disabled, the keyboard input is inhibited and all registers and logic are reset with the exception of the Write Address Counter (WAC) which points to the last entered digit (see Fig. 4).
The current drawn is I_{DDO} (standby current) during hook-on.

CE = HIGH activates the clock oscillator and the circuit changes from static standby condition to the conversation mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard. Then a dialling or redialling operation starts. The operating current is I_{DDP} if in the pulse dialling mode, or I_{DDF} if the DTMF dialling mode is selected.

If the CE input is taken to a LOW level for more than time t_{rd} (see Fig. 7, Fig. 8 and timing data) the system changes to the static standby state and the oscillator stops running. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses are not produced.

Mode selection ($\overline{PD}$/DTMF)

DTMF mode

If $\overline{PD}$/DTMF = V_{DD} the dual tone multi-frequency dialling mode is selected. Each pushbutton activated corresponds to a combination of two tones, each one out of four possible LOW and HIGH group frequencies. The frequencies are transmitted with a constant amplitude, regardless of power supply variations, and filtered off harmonic content to fulfil the CEPT CS 203 recommendations.

The duration of bursts and pauses is the actual pushbutton depress time, but not less than the minimum transmission time (t_t) or minimum pause time (t_p).

PD/Data transmission mode

If PD/DTMF = V_{SS} the pulse-data mode is selected. Starting with numeric keys digits will be dialled out in pulse dialling mode, until key * is depressed which selects the data transmission mode (the * tone is not transmitted). All keys (including * and #) will now be transmitted in DTMF tones.

There are two ways to leave the data transmission mode:

- Reactivate chip enable (CE); HIGH to LOW then HIGH again
- Pressing the flash (FL) key

Keyboard inputs/outputs

The sense column inputs COL 1 to COL 3 and the scanning row outputs ROW 1 to ROW 5 of the PCD4413A are directly connected to the keyboard as shown in Fig. 3.
All keyboard entries are debounced on both the leading and trailing edges for approximately time t_e as shown in Fig. 7, 8 and 9. Each entry is tested for validity.

When a pushbutton is pressed, keyboard scanning starts and only returns to the sense mode after release of the pushbutton.

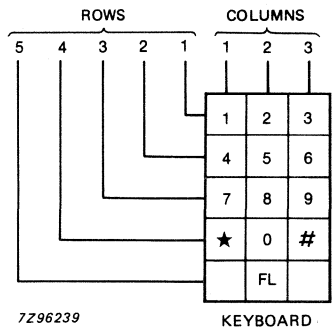


Fig. 3 Keyboard organization.

Row 5 of the keyboard contains the special function key FL — flash or register recall.

Flash

Flash (or register recall) is activated by the FL key and can be used in DTMF, pulse and data transmission modes. Pressing the FL pushbutton will produce a timed line-break of t_{FL} at the DP/FLO output. During the conversation mode this flash pulse entry will act as a chip enable.

The flash pulse resets the read address counter (RAC).

TONE output (DTMF mode)

The single and dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an on-chip active RC low-pass filter.

Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 1 shows the frequency tolerance of the output tones for DTMF signalling.

FUNCTIONAL DESCRIPTION (continued)

Table 1 Frequency tolerance of the output tones for DTMF signalling

row/ column	standard frequency Hz	tone output frequency Hz (1)	frequency deviation	
			%	Hz
row 1	697	697,90	+0,13	+0,90
row 2	770	770,46	+0,06	+0,46
row 3	852	850,45	−0,18	−1,55
row 4	941	943,23	+0,24	+2,23
col 1	1209	1206,45	−0,21	−2,55
col 2	1336	1341,66	+0,42	+5,66
col 3	1477	1482,21	+0,35	+5,21

(1) Tone output frequency when using a 3,579 545 MHz crystal.

When the DTMF mode is selected output tones are timed in manual dialling with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS}. Low group frequencies are generated by forcing the row to V_{DD}. The single tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

Dial pulse and flash output (DP/FLO)

This is a combined output which provides control signals for proper timing in pulse dialling or for a calibrated break in both dialling modes (flash or register recall).

Mute output (M1)

During pulse dialling the mute output becomes active HIGH for the period of the inter-digit pause, break time and make time. It remains at this level until the last digit is pulsed out.

During DTMF dialling the mute output stays HIGH for the period of the transmit and pause time. During Flash the mute output is active HIGH and remains at this level for the period of flash and flash hold-over time.

Mute output ($\overline{M1}$)

Inverted output of M1. In the PCD4413A it is only available as a bonding option of M1.

Strobe output (M2)

Active HIGH output during actual dialling; i.e. during break and make time in pulse dialling, or during tone transmission in DTMF dialling.

Data transmission mode

Timing in the data transmission mode is the same as the manual dialling mode.

DEVELOPMENT DATA

DIALLING PROCEDURES (see also Figs 5 and 6)

Dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address (see Fig. 4). By entering first a numeric digit, the Write Address Counter (WAC) will be set to the first address, the decoded digit will be stored in the register and the WAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the main register after validation. All entries are debounced on both the leading and trailing edges for at least time t_e as shown in Figs 7, 8 and 9. Each entry is tested for validity before being deposited in the main register.

In pulse dialling mode only the 0 to 9 keys result in dialling operations.

* is a special function key:

* *key*

- Used to switch from dialling mode to data transmission mode. The * tones will not be transmitted.

In DTMF and data transmission mode keys 0 to 9, * and # result in associated DTMF tones (see Table 1).

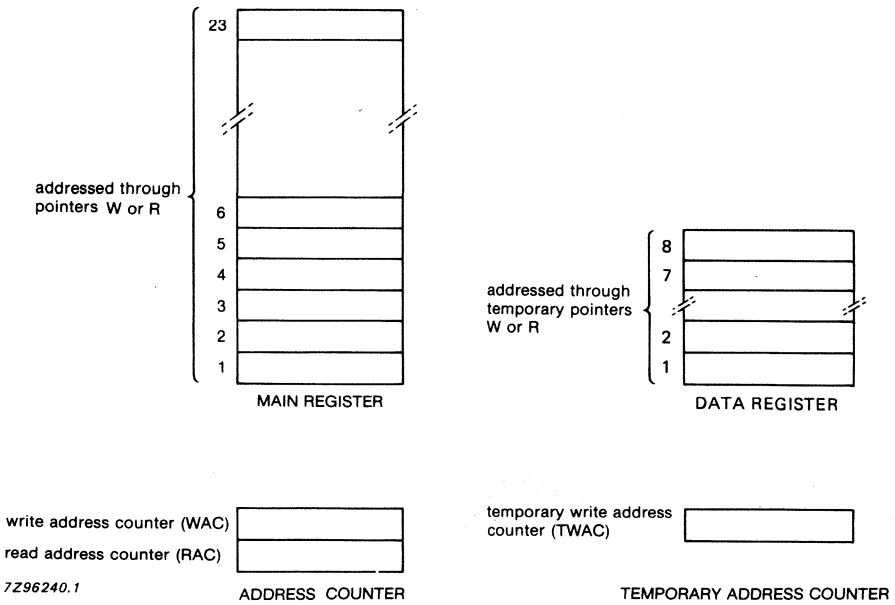


Fig. 4 Memory organization.

DIALLING PROCEDURES (continued)

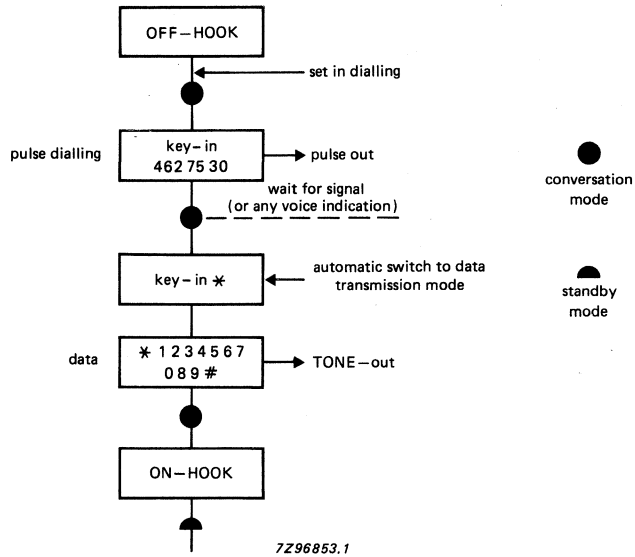


Fig. 5 Pulse and data transmission mode.

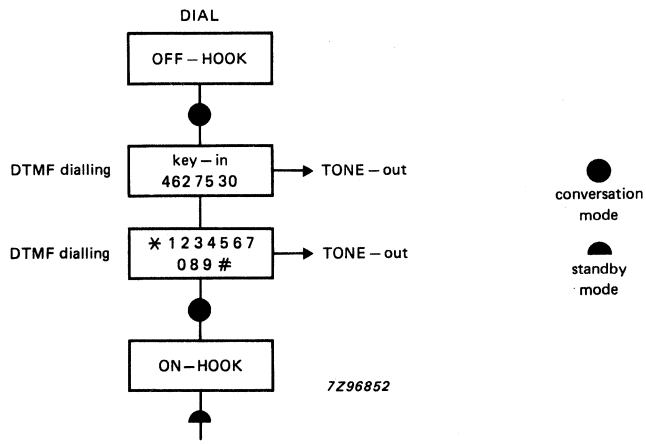


Fig. 6 DTMF mode.

DEVELOPMENT DATA

TIMING

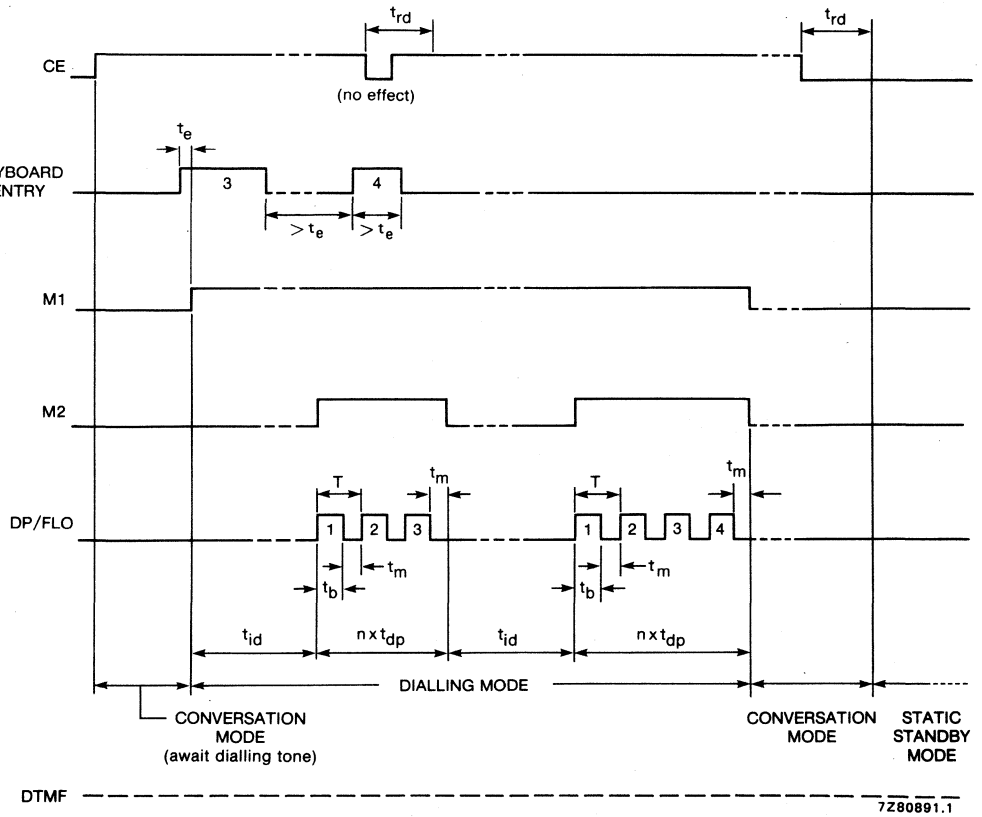


Fig. 7 Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling ($\overline{PD}$/DTMF = V_{SS}).

TIMING (continued)

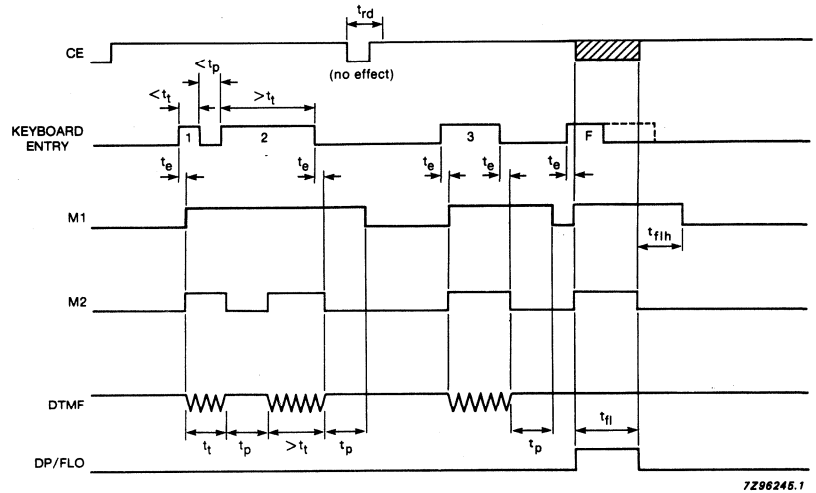


Fig. 8 Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; DTMF dialling ($\overline{PD}$/DTMF = V_{DD}).

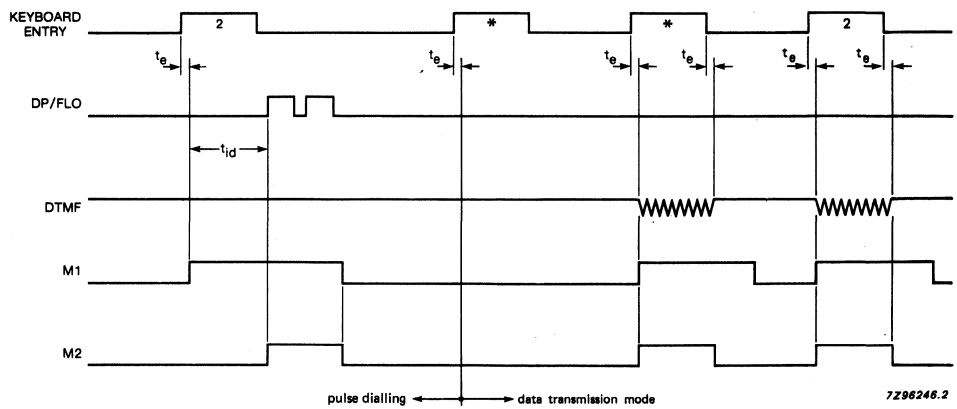


Fig. 9 Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling and data transmission mode.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to 8	V
Supply current	I_{DD}	max.	50	mA
DC current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8	V
Total power dissipation	P_{tot}	max.	300	mW
Power dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579545 MHz; R_S = 100 Ω max.; T_{amb} = −25 to + 70 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Standby supply voltage	V_{DDO}	1,8	–	6,0	V
Operating supply current					
conversation mode (oscillator ON)	I_{DDC}	–	–	150	μA
pulse dialling or flash	I_{DDP}	–	–	200	μA
DTMF dialling (tone ON)	I_{DDF}	–	–	0,9	mA
DTMF dialling (tone OFF)	I_{DDF}	–	–	200	μA
Standby supply current (oscillator OFF; note 1) at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DDO}	–	–	5	μA
INPUTS					
Input voltage LOW (any pin)	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH (any pin)	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current; CE	$\lvert I_{IL}\rvert$	–	–	1	μA
Keyboard inputs					
Keyboard ON resistance	R_{KON}	–	–	2	kΩ
Keyboard OFF resistance	R_{KOFF}	1	–	–	MΩ
OUTPUTS					
Output sink current at $V_{OL} = V_{SS} + 0{,}5$ V					
M1, M2, DP/FLO	I_{OL}	0,7	–	–	mA
Output source current at $V_{OH} = V_{DD} - 0{,}5$ V					
M1, M2, DP/FLO	$-I_{OH}$	0,6	–	–	mA
TIMING AND FREQUENCY					
Clock start-up time	t_{on}	–	4	–	ms
Debounce time	t_e	–	12	–	ms
Reset delay time	t_{rd}	152	160	168	ms

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 10) at V_{DD} = 2,5 to 6 V					
DTMF output voltage levels (r.m.s. value)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Frequency deviation	$\Delta f/f$	−0,6	−	+ 0,6	%
DC voltage level	V_{DC}	−	½V_{DD}	−	V
Output impedance	$\|Z_O\|$	−	0,1	0,5	kΩ
Load resistance	R_L	10	−	−	kΩ
Pre-emphasis of group	ΔV_G	1,85	2,1	2,35	dB
Total harmonic distortion at T_{amb} = 25 °C (note 2)	THD	−	−25	−	dB
Transmission and pause time					
Manual and data transmission dialling mode	t_t	65	−	−	ms
	t_p	65	−	−	ms
Flash pulse duration	t_{FL}	252	254	256	ms
Flash hold-over time	t_{flh}	30	32	34	ms
Pulse dialling (PD)					
Dialling pulse frequency	f_{dp}	9,8	10	10,4	Hz
Inter-digit pause	t_{id}	800	840	880	ms
Break time (note 3)	t_b	58	60	62	ms
Make time (note 3)	t_m	38	40	42	ms

Notes to the characteristics

1. Crystal connected between OSCI and OSCO; CE at V_{SS} and all other pins open-circuit.
2. Related to the level of the LOW group frequency component (CEPT CS 203).
3. Mark-to-space ratio 3 : 2.

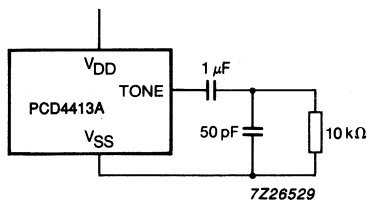
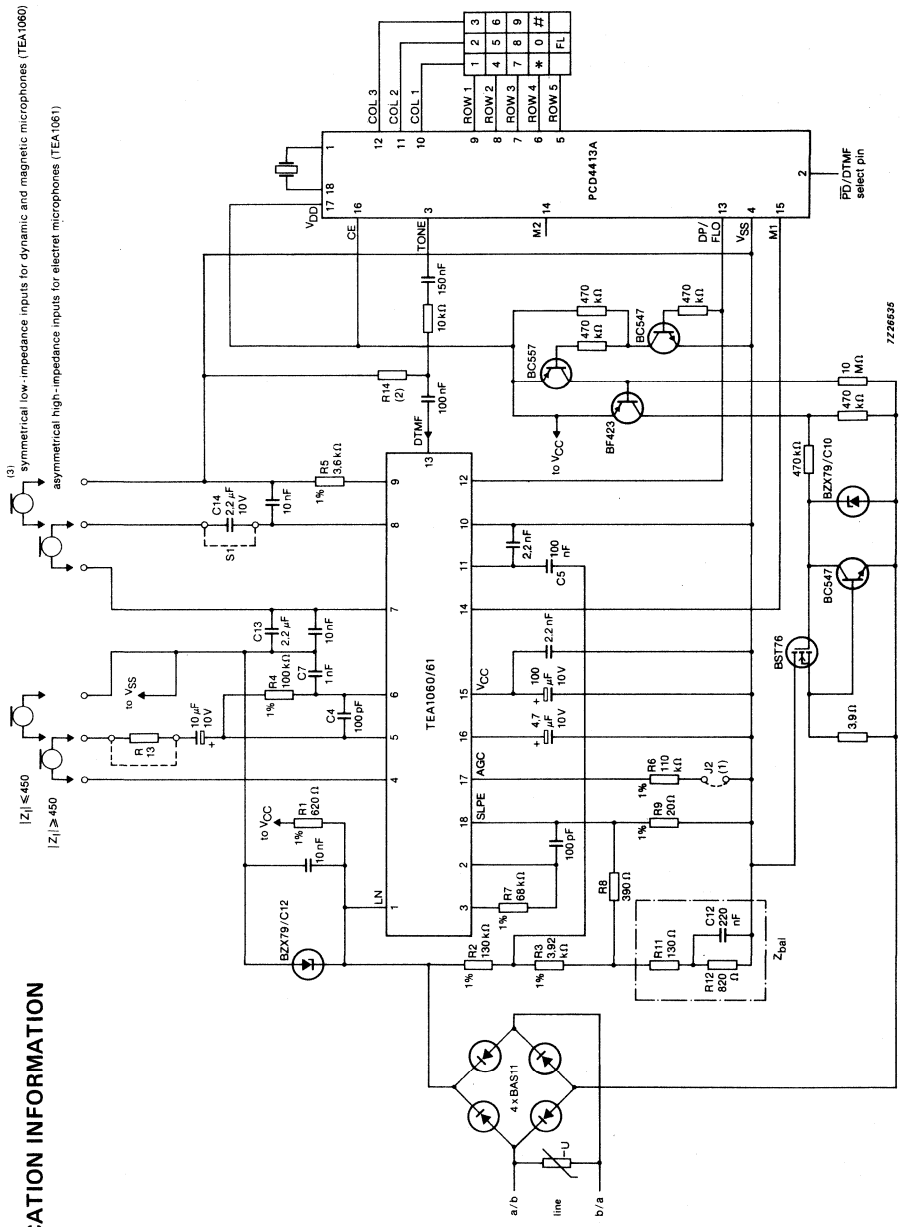


Fig. 10 Tone output test circuit.

APPLICATION INFORMATION



(1) Automatic line compensation obtained by connecting R6 to V_{SS}.
(2) The value of resistor R14 is determined by the required level at LN and the DTMF gain of the TEA1060/61.
(3) Omit C13 and C14; insert S1.

Fig. 11 Application diagram of the full electronic basic telephone set.

PULSE AND DTMF DIALLER WITH REDIAL

GENERAL DESCRIPTION

The PCD4415 is a single-chip silicon gate CMOS integrated circuit with an on-chip oscillator for a 3,58 MHz crystal. It is a dual-standard dialling circuit for either pulse dialling (PD) or dual tone multi-frequency (DTMF) dialling.

Input data is derived from any standard matrix keyboard for dialling in either PD or DTMF mode. Numbers of up to 23 digits can be retained in RAM for redial.

In DTMF mode bursts as well as pauses are timed to a minimum, in manual dialling the maximum depends on the key depression time.

Features

- Pulse and DTMF dialling
- 23-digit capacity for redial operation
- Three dialling modes; pulse, DTMF and data transmission (DTMF)
- Redial buffer for PABX and public calls
- Three function keys; * or >, # or R/AP and FL (flash)
- DTMF timing:
  - manual dialling — minimum duration for bursts and pauses
  - redialling — calibrated timing
- On-chip voltage reference for supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT CS 203 compatible)
- On-chip oscillator uses low-cost 3,58 MHz (tv colour burst) crystal
- Uses standard single-contact or double-contact (common left open) keyboard
- Keyboard entries fully debounced
- Flash (register recall) output

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}	2,5 to 6,0	V
Standby supply voltage	V_{DDO}	1,8 to 6,0	V
Low standby current (on hook) at V_{DDO} = 1,8 V	I_{DDO}	max. 5	μA
Operating currents			
conversation mode	I_{DDC}	max. 150	μA
pulse dialling mode	I_{DDP}	max. 200	μA
DTMF dialling mode	I_{DDF}	max. 0,9	mA
DTMF output voltage level (r.m.s. values)			
HIGH group	$V_{HG(rms)}$	typ. 192	mV
LOW group	$V_{LG(rms)}$	typ. 150	mV
Pre-emphasis of group	ΔV_G	typ. 2,1	dB
Total harmonic distortion	THD	−25	dB
Operating ambient temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINES

PCD4415P: 18-lead DIL; plastic (SOT102).
PCD4415T: 20-lead mini-pack; plastic (SO20; SOT163A).

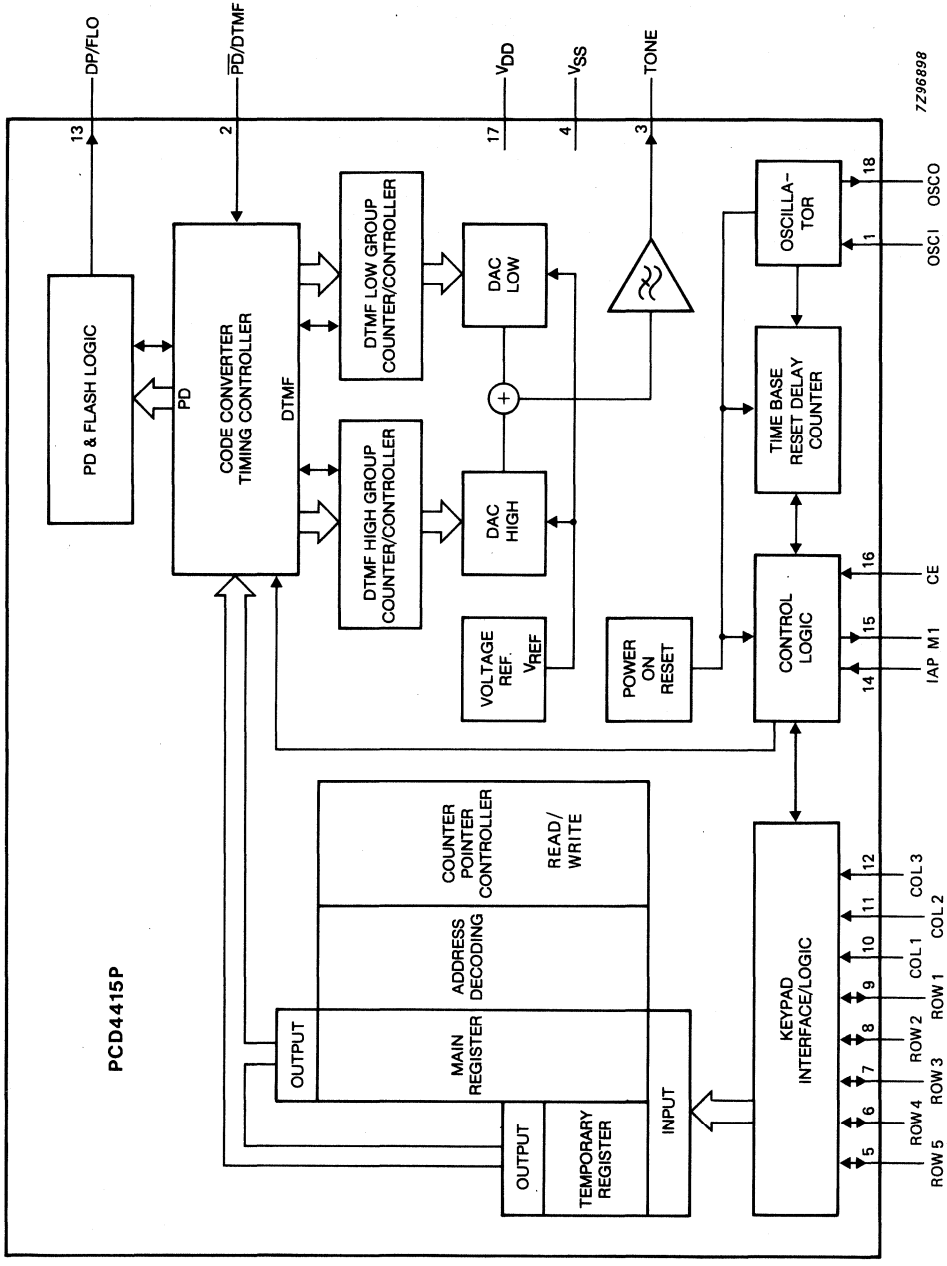


Fig. 1 Block diagram; PCD4415P.

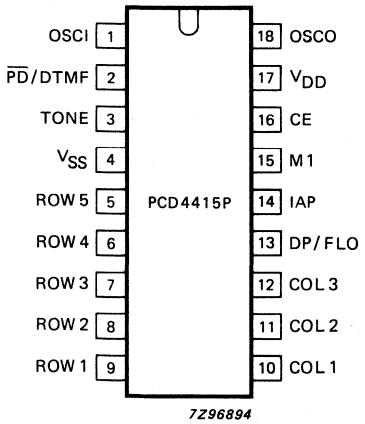


Fig. 2 Pinning diagram; PCD4415P.

PINNING

1	OSCI	oscillator input
2	$\overline{PD}$/DTMF	select pin; pulse or DTMF dialling
3	TONE	single or dual tone frequency output
4	V_{SS}	negative supply
5	ROW 5	scanning row keyboard input/outputs
6	ROW 4	
7	ROW 3	
8	ROW 2	
9	ROW 1	
10	COL 1	sense column keyboard inputs with internal pull-ups
11	COL 2	
12	COL 3	
13	DP/FLO	dialling pulse and flash output
14	IAP	input access pause
15	M1	muting output
16	CE	chip enable input
17	V_{DD}	positive supply
18	OSCO	oscillator output

DEVELOPMENT DATA

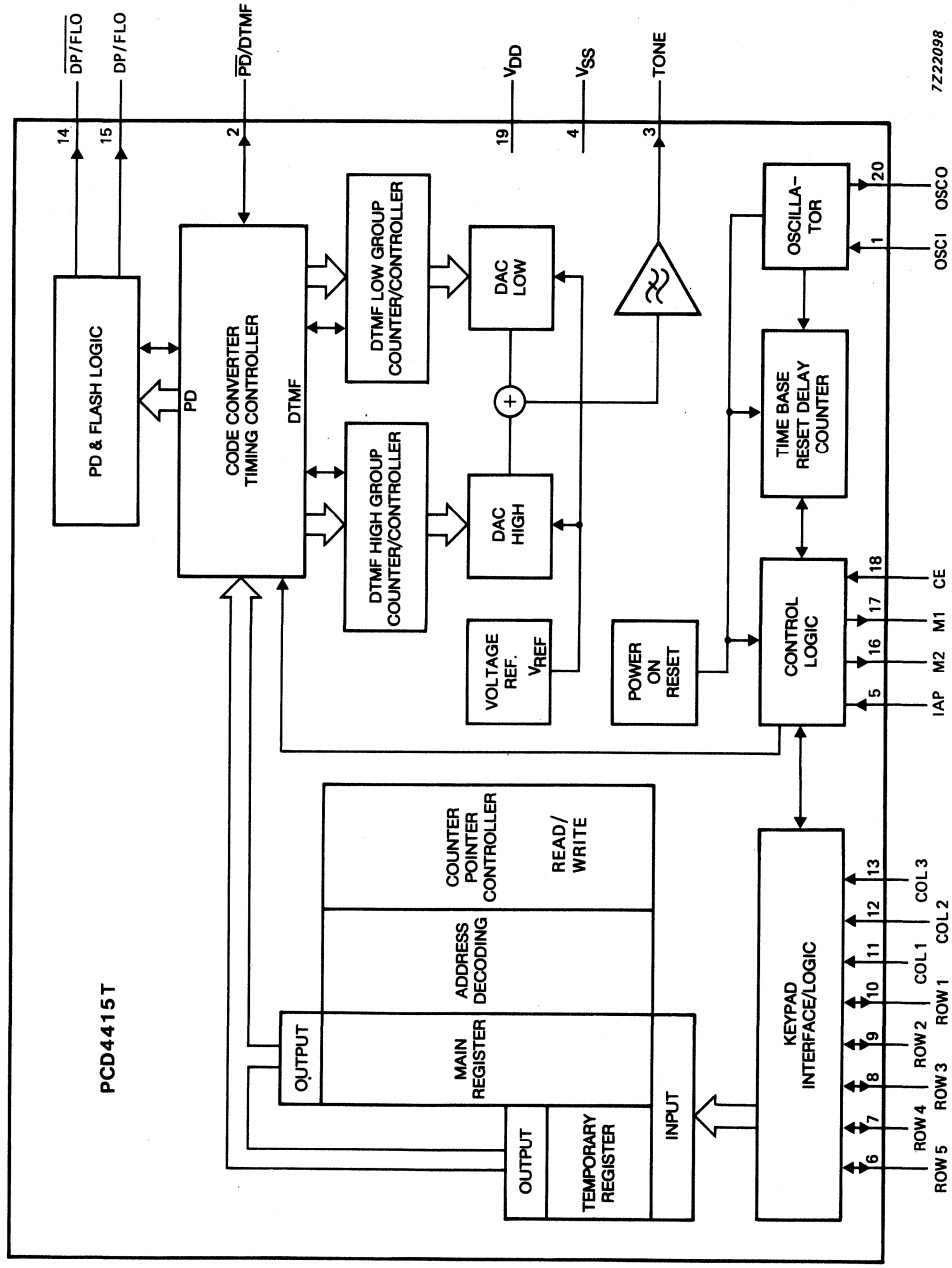


Fig. 3 Block diagram; PCD4415T.

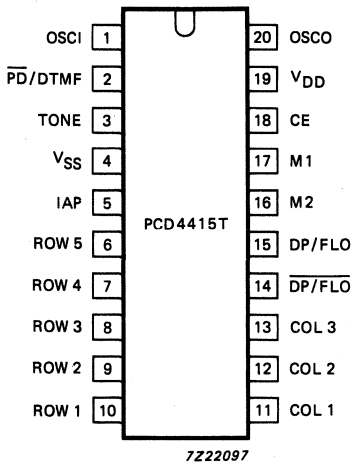


Fig. 4 Pinning diagram; PCD4415T.

PINNING

1	OSCI	oscillator input
2	$\overline{PD}$/DTMF	select pin; pulse or DTMF dialling
3	TONE	single or dual tone frequency output
4	V_{SS}	negative supply
5	IAP	input access pause
6	ROW 5	scanning row keyboard input/outputs
7	ROW 4	
8	ROW 3	
9	ROW 2	
10	ROW 1	
11	COL 1	sense column keyboard inputs with internal pull-ups
12	COL 2	
13	COL 3	
14	$\overline{DP}$/FLO	inverted dialling pulse and flash output
15	DP/FLO	dialling pulse and flash output
16	M2	strobe; active HIGH during transmission
17	M1	muting output
18	CE	chip enable input
19	V_{DD}	positive supply
20	OSCO	oscillator output

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The positive supply of the circuit (V_{DD}) must meet the voltage requirements as indicated in the characteristics.
To avoid undefined states of the device when powered-on, an internal reset circuit clears the control logic and counters.
If V_{DD} drops below the minimum standby supply voltage of 1,8 V the power-on reset circuit inhibits redialling after hook-off.
The power-on-reset signal has the highest priority. It blocks and resets the complete circuit without delay regardless of the state of chip enable input (CE).

Clock oscillator (OSCI, OSCO)

The time base for the PCD4415 for both PD and DTMF modes is a crystal controlled on-chip oscillator which is completed by connecting a 3,58 MHz crystal between the OSCI and OSCO pins.

Chip Enable (CE)

The CE input enables the circuit and is used to initialize the IC.

CE = LOW provides the static standby condition. In this state the clock oscillator is disabled, all registers and logic are reset with the exception of the Write Address Counter (WAC) which points to the last entered digit (see Fig. 6). The keyboard input is inhibited, but data previously entered is saved in the redial register as long as V_{DD} is higher than $V_{DDO(min)}$.
The current drawn is I_{DDO} (standby current) and serves to retain data in the redial register during hook-on.

CE = HIGH activates the clock oscillator and the circuit changes from static standby condition to the conversation mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard. Then a dialling or redialling operation starts. The operating current is I_{DDP} if in the pulse dialling mode, or I_{DDF} if the DTMF dialling mode is selected.

If the CE input is taken to a LOW level for more than time t_{rd} (see Fig. 10a, Fig. 10b and timing data) the system changes to the static standby state and the oscillator stops running. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses are not produced.

Mode selection ($\overline{PD}$/DTMF)

PD mode

If $\overline{PD}$/DTMF = V_{SS} the pulse dialling mode is selected.

DTMF mode

If $\overline{PD}$/DTMF = V_{DD} the dual tone multi-frequency dialling mode is selected. Each numeric push-button activated corresponds to a combination of two tones, each one out of four possible LOW and HIGH group frequencies. The frequencies are transmitted with a constant amplitude, regardless of power supply variations, and filtered off harmonic content to fulfil the CEPT CS 203 recommendations.

The transmission time is calibrated for redial. In manual operation the duration of bursts and pauses is the actual pushbutton depress time, but not less than the minimum transmission time (t_t) or minimum pause time (t_p).

Data transmission mode

Data transmission mode is entered from the dialling mode (PD or DTMF) on first depression of key*, or key >. The "*" tones are not transmitted.
In the data transmission mode no digits are stored for later redial, "*" and "#" are purely DTMF keys, so are no longer special functions. The digits are temporarily stored in a special register, which has a maximum capacity of eight digits.

There are two ways to leave the data transmission mode:

- Reactivate chip enable (CE); HIGH to LOW then HIGH again
- Pressing the flash (FL) key

Keyboard inputs/outputs

The sense column inputs COL 1 to COL 3 and the scanning row outputs ROW 1 to ROW 5 of the PCD4415 are directly connected to the keyboard as shown in Fig. 5.
All keyboard entries are debounced on both the leading and trailing edges for approximately time t_e as shown in Fig. 10. Each entry is tested for validity.

When a pushbutton is pressed, keyboard scanning starts and only returns to the sense mode after release of the pushbutton.

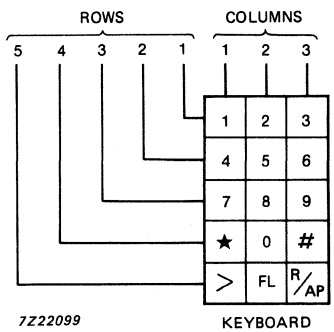


Fig. 5 Keyboard organization.

Keys* and # represent the DTMF tones and also special dialling functions. In ROW 5 the keys > and R/AP only are function keys, while key FL offers flash or register recall.

Flash

Flash (or register recall) is activated by the FL key and can be used in DTMF, pulse and data transmission modes. Pressing the FL pushbutton will produce a timed line-break of 100 ms at the DP/FLO output. During the conversation mode this flash pulse entry will act as a chip enable. This flash pulse duration (t_{FL}) is calibrated at 100 ms.

The flash pulse resets the read address counter (RAC). Later redial is possible (see redial procedure with the "Flash" inserted telephone number).

TONE output (DTMF mode)

The single and dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an on-chip active RC low-pass filter.

Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 1 shows the frequency tolerance of the output tones for DTMF signalling.

FUNCTIONAL DESCRIPTION (continued)

Table 1 Frequency tolerance of the output tones for DTMF signalling

row/ column	standard frequency Hz	tone output frequency Hz (1)	frequency deviation	
			%	Hz
row 1	697	697,90	+0,13	+0,90
row 2	770	770,46	+0,06	+0,46
row 3	852	850,45	−0,18	−1,55
row 4	941	943,23	+0,24	+2,23
col 1	1209	1206,45	−0,21	−2,55
col 2	1336	1341,66	+0,42	+5,66
col 3	1477	1482,21	+0,35	+5,21

(1) Tone output frequency when using a 3,579 545 MHz crystal.

When the DTMF mode is selected output tones are timed in manual dialling with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS}. Low group frequencies are generated by forcing the row to V_{DD}. The single tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

Dial pulse and flash output (DP/FLO)

This is a combined output which provides control signals for proper timing in pulse dialling or for a calibrated break in both dialling modes (flash or register recall).

Dial pulse and flash output ($\overline{DP/FLO}$)

Inverted output of DP/FLO. In the PCD4415 it is only available as a bonding option of DP/FLO.

Mute output (M1)

During pulse dialling the mute output becomes active HIGH for the period of the inter-digit pause, break time and make time. It remains at this level until the last digit is pulsed out.

During DTMF dialling the mute output becomes HIGH for the period of the tone transmission and pause times. During Flash the mute output is active HIGH and remains at this level for the period of flash and flash hold-over time.

Mute output ($\overline{M1}$)

Inverted output of M1. In the PCD4415 it is only available as a bonding option of M1.

Strobe output (M2)

Active HIGH output during actual dialling; i.e. during break and make time in pulse dialling, or during tone transmission in DTMF dialling. Only available as a bonding option of IAP.

Input access pause (IAP)

This input can be used instead of the # (R/AP) key for programming access pause(s) in RAM when dialling and terminating access pause(s) during redial.

Data transmission mode

Timing in the data transmission mode is the same as the manual dialling mode.

DIALLING PROCEDURES (see also Figs 7, 8 and 9)

Dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address (see Fig. 6). By entering first a numeric digit, the Write Address Counter (WAC) will be set to the first address, the decoded digit will be stored in the register and the WAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the redial register after validation. If more than 23 digits are entered redial will be inhibited. All entries are debounced on both the leading and trailing edges for at least time t_e as shown in Fig. 10. Each entry is tested for validity before being deposited in the redial register.

In manual dialling mode (pulses and DTMF) only the 0 to 9 keys result in dialling operations.

"#" and "*" are special function keys:

 # key or R/AP key

- If the first key after CE or Flash means: Redial (see redial procedure)
- If not the first key, then it is used to program access pause(s) in the RAM for later redial. If it is the last key it will be omitted before going "on-hook".

** key or > key*

- Used to switch from dialling mode (pulse or DTMF) to data transmission mode. The * tones will not be transmitted even if the previous mode was DTMF dialling.

In data transmission mode keys 0 to 9, * and # result in associated DTMF tones (see Table 1), keys > and R/AP will be ignored.

DEVELOPMENT DATA

Redialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address to be sent. The PCD4415 is in conversation mode.
If "#"or "R/AP" is the first keyboard entry the circuit starts redialling the contents of the register, Timing in the DTMF mode is calibrated for both tone bursts and pauses.
Only the first part entered (the pulse or DTMF dialled part of the stored number) can be redialled.
During redial keyboard entries (function or non-function) are not accepted until the circuit returns to the conversation mode after completion of redialling. The # and R/AP keys are active only during access pauses.

No redial activity takes place if one of the following events occur:

- Power-on reset
- Memory overflow (more than 23 valid data entries)

If an access pause is detected during redial, the circuit is switched back to the conversation mode and stays there until the # or R/AP key is depressed. Therefore when the # or R/AP key is depressed the access pause is ended. After termination of the access pause the circuit continues dialling the rest of the telephone number.

In addition to the manual use of the # or R/AP key for programming and terminating access pause(s), the input input IAP can be used. If during manual dialling and conversation mode IAP becomes HIGH, an access pause will be stored in the memory.
If after "on-hook" or "flash" the last stored digit is an access pause then it will be deleted out of the memory.
When during redialling an access pause occurs and IAP becomes HIGH, then the access pause will be automatically terminated and redialling continues.

As soon as the conversation mode is entered depressing the * or > key will again switch the circuit to the data transmission mode.

Redial takes place in the main register (max. 23 digits). After redial when a numeric key is pressed (first digit of an extension number) the redial number will be cleared. Thus the total capacity of the main register is available for extension number dialling. This extension number is stored in the main register

DIALLING PROCEDURES (continued)

(max. 23 digits) and is available later after "on-hook", "off-hook".

The main register will also store digits that have been keyed-in at a rate faster than dialled out.

Access pause

- The number of access pauses is unlimited.
- Consecutive pauses will be stored as a single pause.

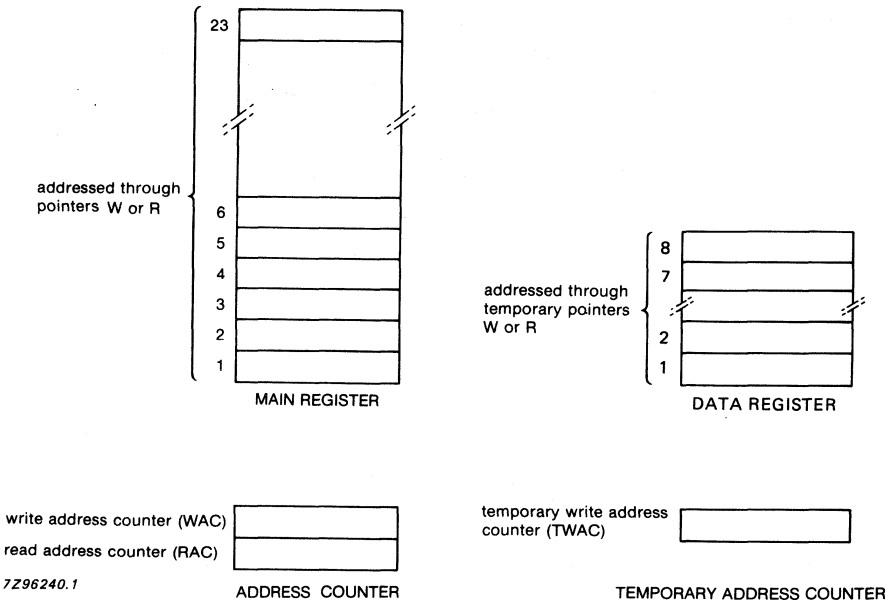


Fig. 6 Memory organization.

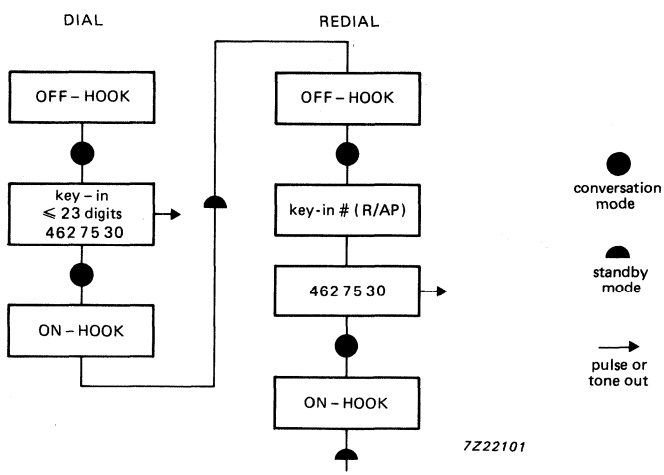


Fig. 7 Pulse/DTMF dialling mode.

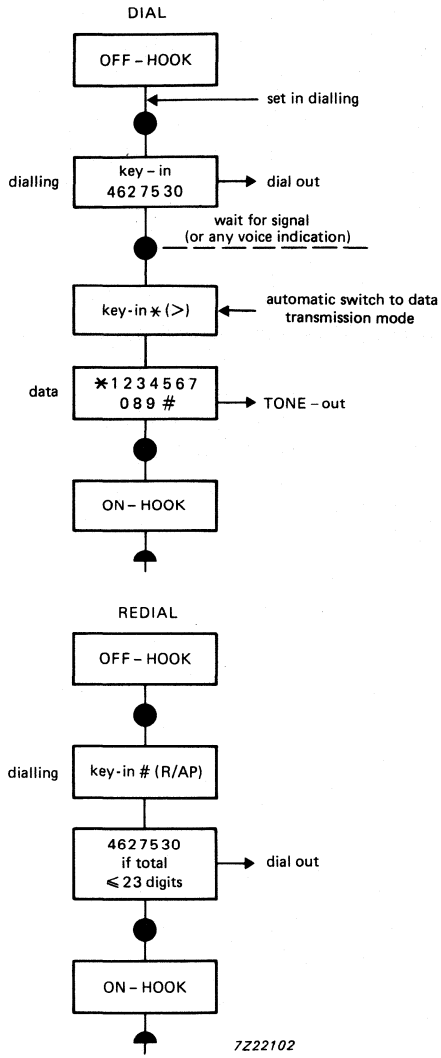


Fig. 8 Pulse/DTMF dialling and data transmission mode.

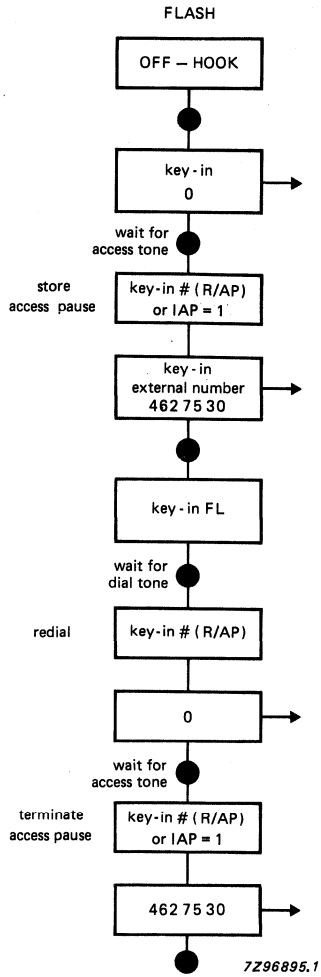


Fig. 9 Flash; independent of dialling mode.

DEVELOPMENT DATA

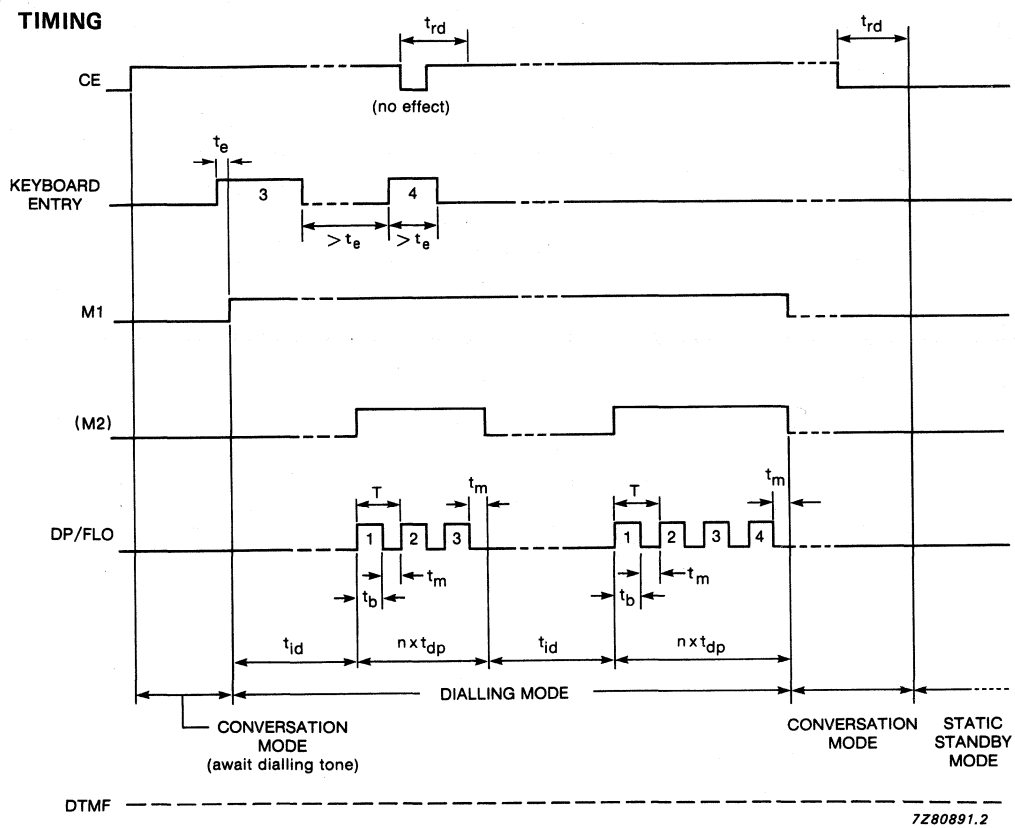


Fig. 10a Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling ($\overline{PD}$/DTMF = V_{SS}).

TIMING (continued)

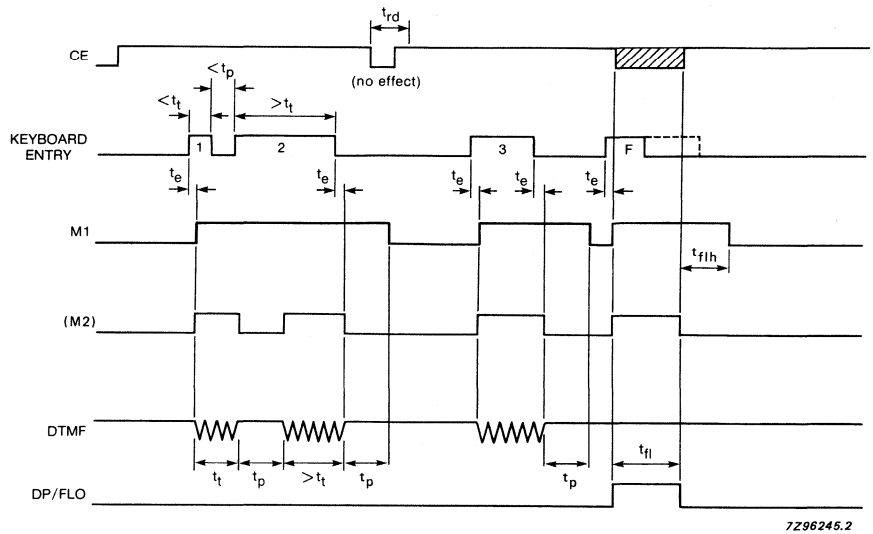


Fig. 10b Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; DTMF dialling ($\overline{PD}$/DTMF = V_{DD}).

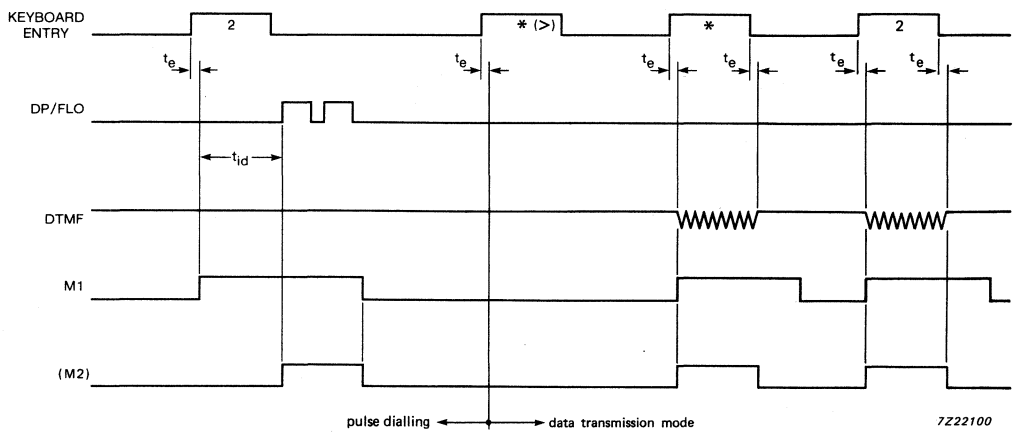


Fig. 10c Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling and data transmission mode.

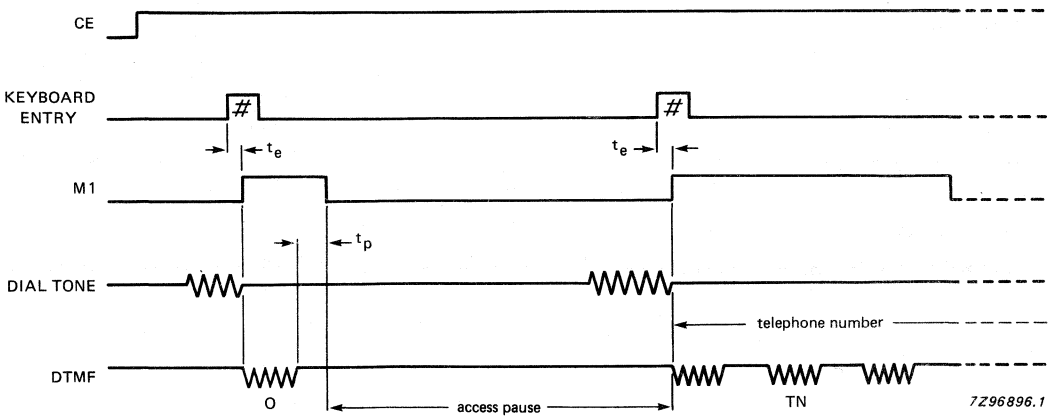


Fig. 11a Timing diagram showing REDIAL where PABX access digit(s) are the first keyboard entries and access pause is terminated by the # or R/AP key; DTMF dialling with $\overline{PD}$/DTMF = V_{DD}.

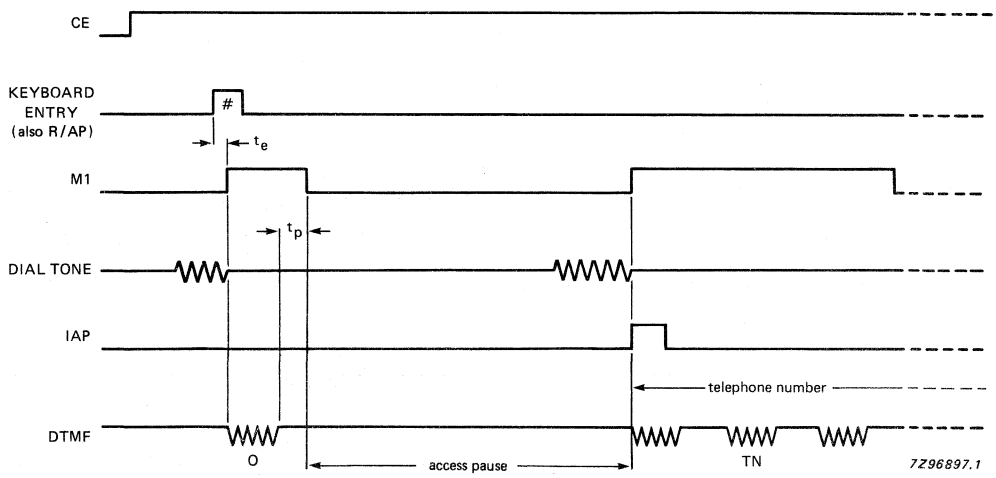


Fig. 11b Timing diagram showing REDIAL where PABX access digit(s) occur and are terminated by IAP; DTMF dialling with $\overline{PD}$/DTMF = V_{DD}.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to 8	V
Supply current	I_{DD}	max.	50	mA
DC current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8	V
Total power dissipation	P_{tot}	max.	300	mW
Power dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579545 MHz; R_S = 100 Ω max.; T_{amb} = −25 to + 70 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Standby supply voltage	V_{DDO}	1,8	–	6,0	V
Operating supply current					
conversation mode (oscillator ON)	I_{DDC}	–	–	150	μA
pulse dialling or flash	I_{DDP}	–	–	200	μA
DTMF dialling (tone ON)	I_{DDF}	–	–	0,9	mA
DTMF dialling (tone OFF)	I_{DDF}	–	–	200	μA
Standby supply current (oscillator OFF; note 1) at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DDO}	–	–	5	μA
INPUTS					
Input voltage LOW (any pin)	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH (any pin)	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current; CE	$\lvert I_{IL}\rvert$	–	–	1	μA
Keyboard inputs					
Keyboard ON resistance	R_{KON}	–	–	2	kΩ
Keyboard OFF resistance	R_{KOFF}	1	–	–	MΩ
OUTPUTS					
Output sink current at $V_{OL} = V_{SS} + 0{,}5$ V					
M1, M2, DP/FLO, $\overline{DP/FLO}$	I_{OL}	0,7	–	–	mA
Output source current at $V_{OH} = V_{DD} - 0{,}5$ V					
M1, M2, DP/FLO	$-I_{OH}$	0,6	–	–	mA
TIMING AND FREQUENCY					
Clock start-up time	t_{on}	–	4	–	ms
Debounce time	t_e	–	12	–	ms
Reset delay time	t_{rd}	152	160	168	ms

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 12) at V_{DD} = 2,5 to 6 V					
DTMF output voltage levels (r.m.s. value)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Frequency deviation	$\Delta f/f$	−0,6	−	+ 0,6	%
DC voltage level	V_{DC}	−	½V_{DD}	−	V
Output impedance	$\|Z_O\|$	−	0,1	0,5	kΩ
Load resistance	R_L	10	−	−	kΩ
Pre-emphasis of group	ΔV_G	1,85	2,1	2,35	dB
Total harmonic distortion at T_{amb} = 25 °C (note 2)	THD	−	−25	−	dB
Transmission and pause time (note 3)					
Manual and data transmission dialling mode	t_t	65	−	−	ms
	t_p	65	−	−	ms
Redialling	t_t	65	70	75	ms
	t_p	65	70	75	ms
Flash pulse duration	t_{FL}	95	100	105	ms
Flash hold-over time	t_{flh}	32	34	36	ms
Pulse dialling (PD) (note 3)					
Dialling pulse frequency	f_{dp}	9,8	10	10,4	Hz
Inter-digit pause	t_{id}	800	840	880	ms
Break time (note 4)	t_b	64	66	68	ms
Make time (note 4)	t_m	32	34	36	ms

Notes to the characteristics

1. Crystal connected between OSCI and OSCO; CE at V_{SS} and all other pins open-circuit.
2. Related to the level of the LOW group frequency component (CEPT CS 203).
3. Other timing is possible on request.
4. Mark-to-space ratio 2:1.

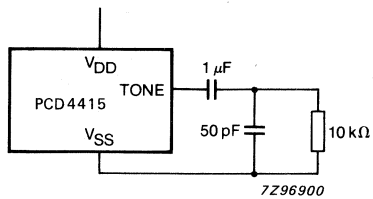
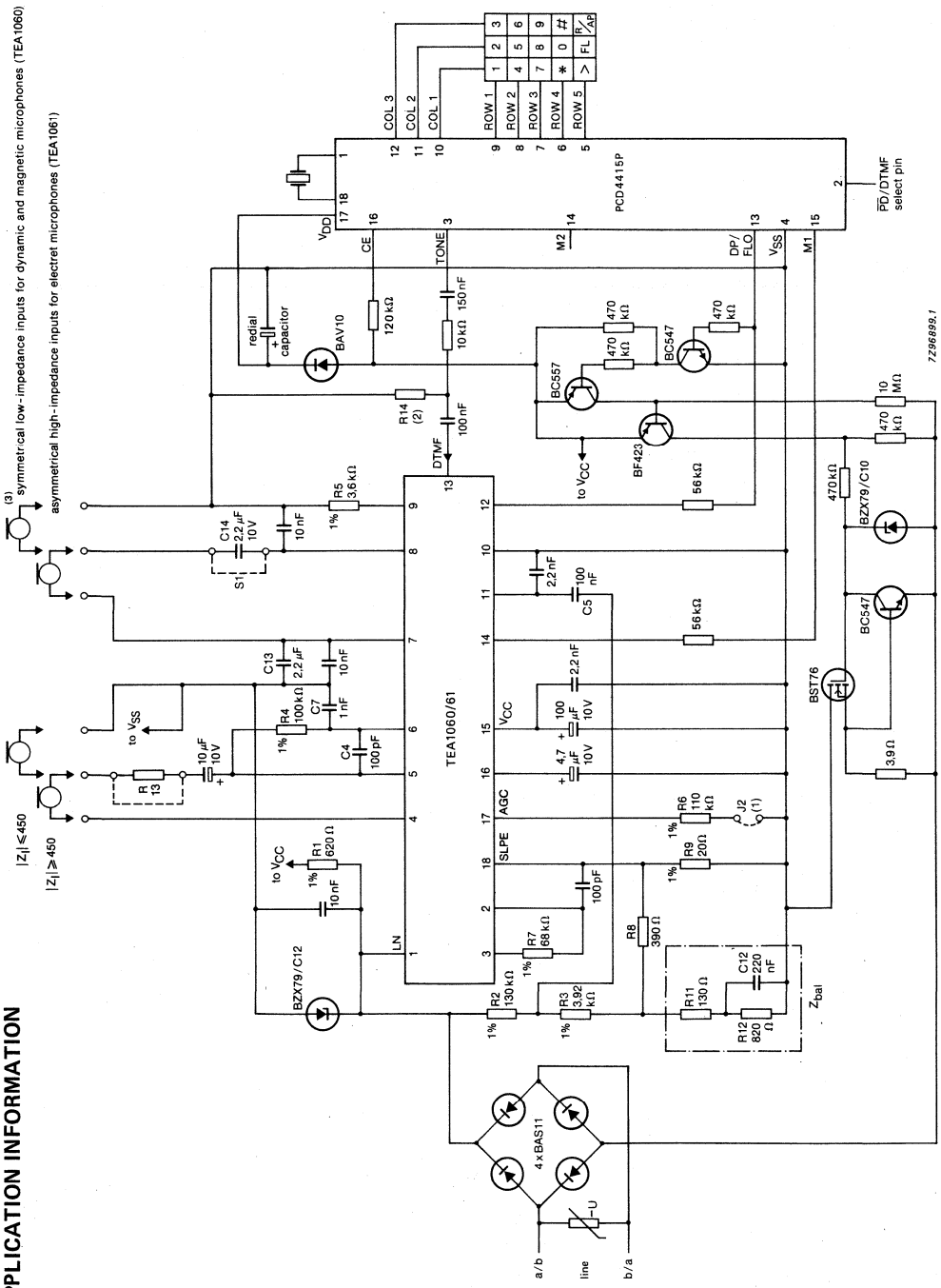


Fig. 12 Tone output test circuit.

DEVELOPMENT DATA

APPLICATION INFORMATION



(1) Automatic line compensation obtained by connecting R6 to V_{SS}.
(2) The value of resistor R14 is determined by the required level at LN and the DTMF gain of the TEA1060/61.
(3) Omit C13 and C14; insert S1.

Fig. 13 Application diagra f the full electronic basic telephone set.

PULSE AND DTMF DIALLER WITH REDIAL

GENERAL DESCRIPTION

The PCD4415A is a single-chip silicon gate CMOS integrated circuit with an on-chip oscillator for a 3,58 MHz crystal. It is a dual-standard dialling circuit for either pulse dialling (PD) or dual tone multi-frequency (DTMF) dialling.

Input data is derived from any standard matrix keyboard for dialling in either PD or DTMF mode. Numbers of up to 23 digits can be retained in RAM for redial.

In DTMF mode bursts as well as pauses are timed to a minimum, in manual dialling the maximum depends on the key depression time.

Features

- Pulse and DTMF dialling
- 23-digit capacity for redial operation
- Three dialling modes; pulse, DTMF and data transmission (DTMF)
- Redial buffer for PABX and public calls
- Three function keys; * or >, # or R/AP and FL (flash)
- DTMF timing:
  manual dialling – minimum duration for bursts and pauses
  redialling – calibrated timing
- On-chip voltage reference for supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT CS 203 compatible)
- On-chip oscillator uses low-cost 3,58 MHz (tv colour burst) crystal
- Uses standard single-contact or double-contact (common left open) keyboard
- Keyboard entries fully debounced
- Flash (register recall) output

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}	2,5 to 6,0	V
Standby supply voltage	V_{DDO}	1,8 to 6,0	V
Low standby current (on hook) at V_{DDO} = 1,8 V	I_{DDO}	max. 5	μA
Operating currents			
conversation mode	I_{DDC}	max. 150	μA
pulse dialling mode	I_{DDP}	max. 200	μA
DTMF dialling mode	I_{DDF}	max. 0,9	mA
DTMF output voltage level (r.m.s. values)			
HIGH group	$V_{HG(rms)}$	typ. 192	mV
LOW group	$V_{LG(rms)}$	typ. 150	mV
Pre-emphasis of group	ΔV_G	typ. 2,1	dB
Total harmonic distortion	THD	−25	dB
Operating ambient temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINES

PCD4415AP: 18-lead DIL; plastic (SOT102G,N,PE).
PCD4415AT: 20-lead mini-pack; plastic (SO20; SOT163A).

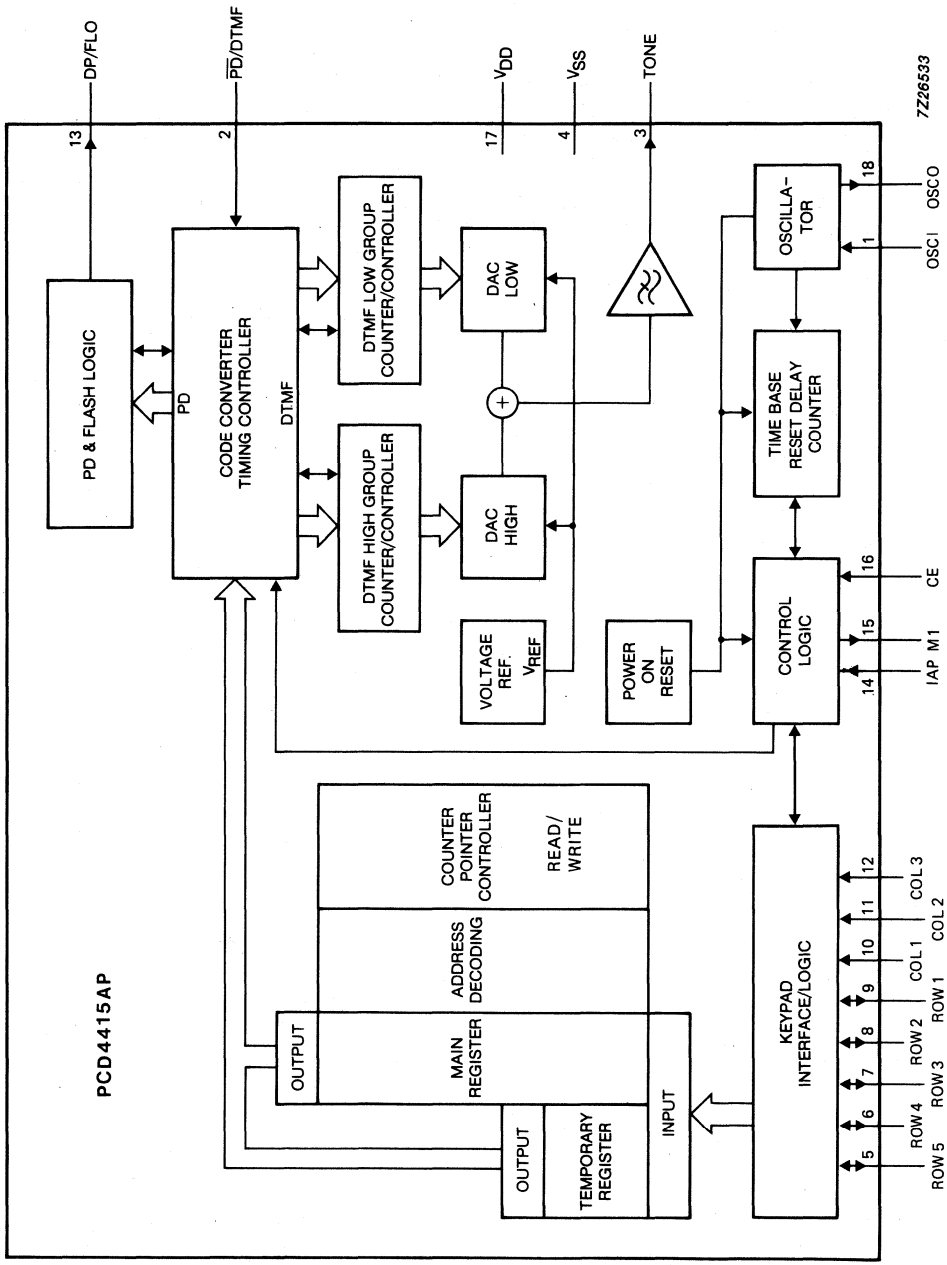


Fig.1 Block diagram; PCD4415AP.

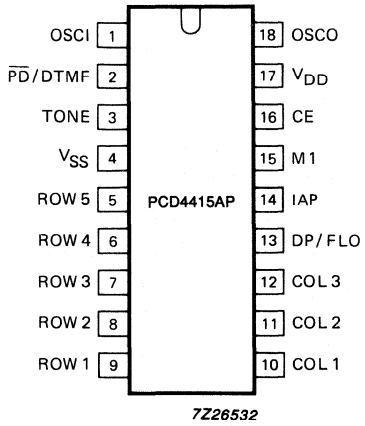


Fig.2 Pinning diagram; PCD4415AP.

PINNING

1	OSCI	oscillator input
2	$\overline{PD}$/DTMF	select pin; pulse or DTMF dialling
3	TONE	single or dual tone frequency output
4	V_{SS}	negative supply
5	ROW 5	scanning row keyboard input/outputs
6	ROW 4	
7	ROW 3	
8	ROW 2	
9	ROW 1	
10	COL 1	sense column keyboard inputs with internal pull-ups
11	COL 2	
12	COL 3	
13	DP/FLO	dialling pulse and flash output
14	IAP	input access pause
15	M1	muting output
16	CE	chip enable input
17	V_{DD}	positive supply
18	OSCO	oscillator output

DEVELOPMENT DATA

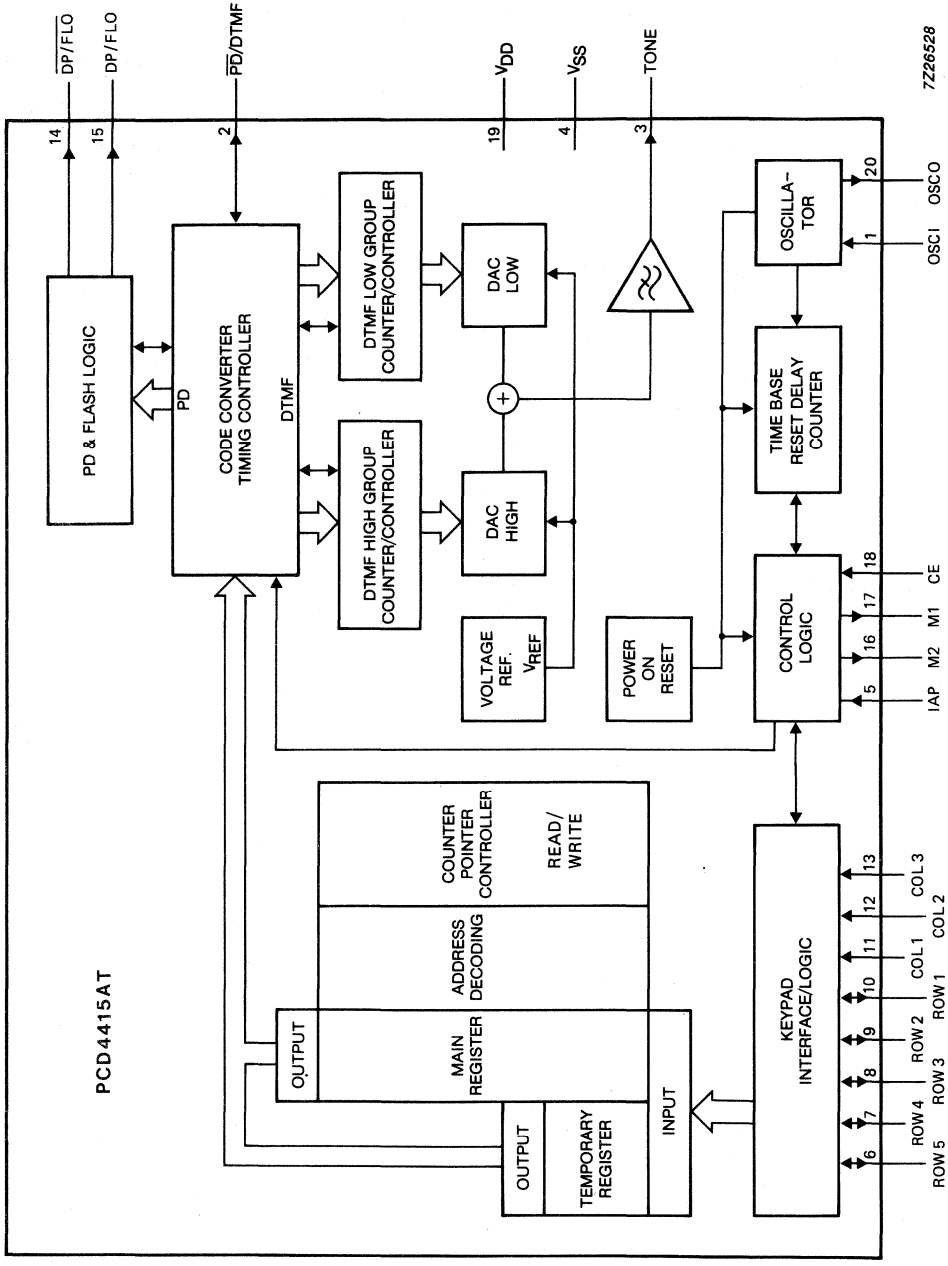


Fig.3 Block diagram; PCD4415AT.

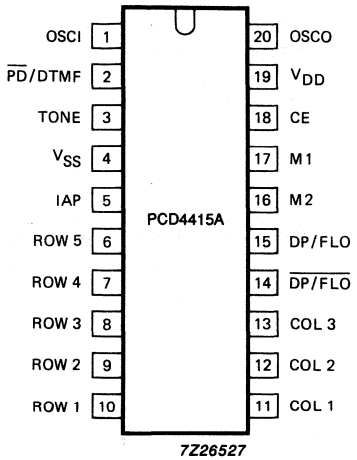


Fig.4 Pinning diagram; PCD4415AT.

PINNING

1	OSCI	oscillator input
2	$\overline{PD}$/DTMF	select pin; pulse or DTMF dialling
3	TONE	single or dual tone frequency output
4	V_{SS}	negative supply
5	IAP	input access pause
6	ROW 5	scanning row keyboard input/outputs
7	ROW 4	
8	ROW 3	
9	ROW 2	
10	ROW 1	
11	COL 1	sense column keyboard inputs with internal pull-ups
12	COL 2	
13	COL 3	
14	$\overline{DP}$/FLO	inverted dialling pulse and flash output
15	DP/FLO	dialling pulse and flash output
16	M2	strobe; active HIGH during transmission
17	M1	muting output
18	CE	chip enable input
19	V_{DD}	positive supply
20	OSCO	oscillator output

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The positive supply of the circuit (V_{DD}) must meet the voltage requirements as indicated in the characteristics.
To avoid undefined states of the device when powered-on, an internal reset circuit clears the control logic and counters.
If V_{DD} drops below the minimum standby supply voltage of 1,8 V the power-on reset circuit inhibits redialling after hook-off.
The power-on-reset signal has the highest priority. It blocks and resets the complete circuit without delay regardless of the state of chip enable input (CE).

Clock oscillator (OSCI, OSCO)

The time base for the PCD4415A for both PD and DTMF modes is a crystal controlled on-chip oscillator which is completed by connecting a 3,58 MHz crystal between the OSCI and OSCO pins.

Chip Enable (CE)

The CE input enables the circuit and is used to initialize the IC.

CE = LOW provides the static standby condition. In this state the clock oscillator is disabled, all registers and logic are reset with the exception of the Write Address Counter (WAC) which points to the last entered digit (see Fig. 6). The keyboard input is inhibited, but data previously entered is saved in the redial register as long as V_{DD} is higher than $V_{DDO(min)}$.
The current drawn is I_{DDO} (standby current) and serves to retain data in the redial register during hook-on.

CE = HIGH activates the clock oscillator and the circuit changes from static standby condition to the conversation mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard. Then a dialling or redialling operation starts. The operating current is I_{DDP} if in the pulse dialling mode, or I_{DDF} if the DTMF dialling mode is selected.

If the CE input is taken to a LOW level for more than time t_{rd} (see Fig. 10a, Fig. 10b and timing data) the system changes to the static standby state and the oscillator stops running. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses are not produced.

Mode selection ($\overline{PD}$/DTMF)

PD mode

If $\overline{PD}$/DTMF = V_{SS} the pulse dialling mode is selected.

DTMF mode

If $\overline{PD}$/DTMF = V_{DD} the dual tone multi-frequency dialling mode is selected. Each numeric push-button activated corresponds to a combination of two tones, each one out of four possible LOW and HIGH group frequencies. The frequencies are transmitted with a constant amplitude, regardless of power supply variations, and filtered off harmonic content to fulfil the CEPT CS 203 recommendations.

The transmission time is calibrated for redial. In manual operation the duration of bursts and pauses is the actual pushbutton depress time, but not less than the minimum transmission time (t_t) or minimum pause time (t_p).

Data transmission mode

Data transmission mode is entered from the dialling mode (PD or DTMF) on first depression of key*, or key >. The "*" tones are not transmitted.
In the data transmission mode no digits are stored for later redial, "*" and "#" are purely DTMF keys, so are no longer special functions. The digits are temporarily stored in a special register, which has a maximum capacity of eight digits.

There are two ways to leave the data transmission mode:

- Reactivate chip enable (CE); HIGH to LOW then HIGH again
- Pressing the flash (FL) key

Keyboard inputs/outputs

The sense column inputs COL 1 to COL 3 and the scanning row outputs ROW 1 to ROW 5 of the PCD4415A are directly connected to the keyboard as shown in Fig. 5.
All keyboard entries are debounced on both the leading and trailing edges for approximately time t_e as shown in Fig. 10. Each entry is tested for validity.

When a pushbutton is pressed, keyboard scanning starts and only returns to the sense mode after release of the pushbutton.

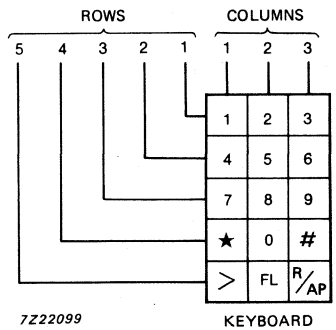


Fig. 5 Keyboard organization.

Keys* and # represent the DTMF tones and also special dialling functions. In ROW 5 the keys > and R/AP only are function keys, while key FL offers flash or register recall.

Flash

Flash (or register recall) is activated by the FL key and can be used in DTMF, pulse and data transmission modes. Pressing the FL pushbutton will produce a timed line-break of t_{FL} at the DP/FLO output. During the conversation mode this flash pulse entry will act as a chip enable.
The flash pulse resets the read address counter (RAC). Later redial is possible (see redial procedure with the "Flash" inserted telephone number).

TONE output (DTMF mode)

The single and dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an on-chip active RC low-pass filter.

Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 1 shows the frequency tolerance of the output tones for DTMF signalling.

FUNCTIONAL DESCRIPTION (continued)

Table 1 Frequency tolerance of the output tones for DTMF signalling

row/ column	standard frequency Hz	tone output frequency Hz (1)	frequency deviation	
			%	Hz
row 1	697	697,90	+0,13	+0,90
row 2	770	770,46	+0,06	+0,46
row 3	852	850,45	−0,18	−1,55
row 4	941	943,23	+0,24	+2,23
col 1	1209	1206,45	−0,21	−2,55
col 2	1336	1341,66	+0,42	+5,66
col 3	1477	1482,21	+0,35	+5,21

(1) Tone output frequency when using a 3,579 545 MHz crystal.

When the DTMF mode is selected output tones are timed in manual dialling with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS}. Low group frequencies are generated by forcing the row to V_{DD}. The single tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

Dial pulse and flash output (DP/FLO)

This is a combined output which provides control signals for proper timing in pulse dialling or for a calibrated break in both dialling modes (flash or register recall).

Dial pulse and flash output ($\overline{DP/FLO}$)

Inverted output of DP/FLO. In the PCD4415A it is only available as a bonding option of DP/FLO.

Mute output (M1)

During pulse dialling the mute output becomes active HIGH for the period of the inter-digit pause, break time and make time. It remains at this level until the last digit is pulsed out.

During DTMF dialling the mute output becomes HIGH for the period of the tone transmission and pause times. During Flash the mute output is active HIGH and remains at this level for the period of flash and flash hold-over time.

Mute output ($\overline{M1}$)

Inverted output of M1. In the PCD4415A it is only available as a bonding option of M1.

Strobe output (M2)

Active HIGH output during actual dialling; i.e. during break and make time in pulse dialling, or during tone transmission in DTMF dialling. Only available as a bonding option of IAP.

Input access pause (IAP)

This input can be used instead of the # (R/AP) key for programming access pause(s) in RAM when dialling and terminating access pause(s) during redial.

Data transmission mode

Timing in the data transmission mode is the same as the manual dialling mode.

DIALLING PROCEDURES (see also Figs 7, 8 and 9)

Dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address (see Fig. 6). By entering first a numeric digit, the Write Address Counter (WAC) will be set to the first address, the decoded digit will be stored in the register and the WAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the redial register after validation. If more than 23 digits are entered redial will be inhibited. All entries are debounced on both the leading and trailing edges for at least time t_e as shown in Fig. 10. Each entry is tested for validity before being deposited in the redial register.

In manual dialling mode (pulses and DTMF) only the 0 to 9 keys result in dialling operations.

"#" and "*" are special function keys:

 # key or R/AP key

- If the first key after CE or Flash means: Redial (see redial procedure)
- If not the first key, then it is used to program access pause(s) in the RAM for later redial. If it is the last key it will be omitted before going "on-hook".

** key or > key*

- Used to switch from dialling mode (pulse or DTMF) to data transmission mode. The * tones will not be transmitted even if the previous mode was DTMF dialling.

In data transmission mode keys 0 to 9, * and # result in associated DTMF tones (see Table 1), keys > and R/AP will be ignored.

DEVELOPMENT DATA

Redialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address to be sent. The PCD4415 is in conversation mode.
If "#" or "R/AP" is the first keyboard entry the circuit starts redialling the contents of the register, Timing in the DTMF mode is calibrated for both tone bursts and pauses.
Only the first part entered (the pulse or DTMF dialled part of the stored number) can be redialled.
During redial keyboard entries (function or non-function) are not accepted until the circuit returns to the conversation mode after completion of redialling. The # and R/AP keys are active only during access pauses.

No redial activity takes place if one of the following events occur:

- Power-on reset
- Memory overflow (more than 23 valid data entries)

If an access pause is detected during redial, the circuit is switched back to the conversation mode and stays there until the # or R/AP key is depressed. Therefore when the # or R/AP key is depressed the access pause is ended. After termination of the access pause the circuit continues dialling the rest of the telephone number.

In addition to the manual use of the # or R/AP key for programming and terminating access pause(s), the input input IAP can be used. If during manual dialling and conversation mode IAP becomes HIGH, an access pause will be stored in the memory.
If after "on-hook" or "flash" the last stored digit is an access pause then it will be deleted out of the memory.
When during redialling an access pause occurs and IAP becomes HIGH, then the access pause will be automatically terminated and redialling continues.

As soon as the conversation mode is entered depressing the * or > key will again switch the circuit to the data transmission mode.

Redial takes place in the main register (max. 23 digits). After redial when a numeric key is pressed (first digit of an extension number) the redial number will be cleared. Thus the total capacity of the main register is available for extension number dialling. This extension number is stored in the main register

DIALLING PROCEDURES (continued)

(max. 23 digits) and is available later after "on-hook", "off-hook".

The main register will also store digits that have been keyed-in at a rate faster than dialled out.

Access pause

- The number of access pauses is unlimited.
- Consecutive pauses will be stored as a single pause.

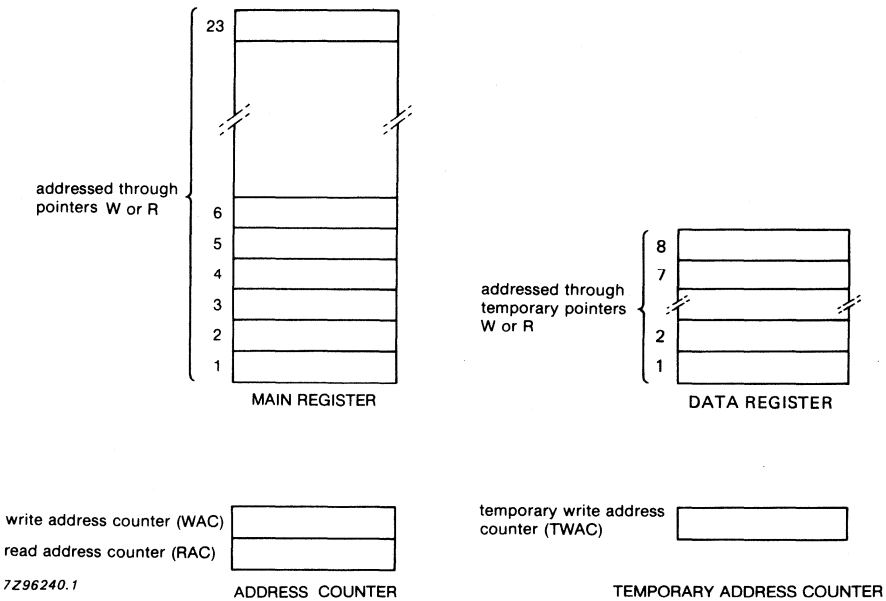


Fig. 6 Memory organization.

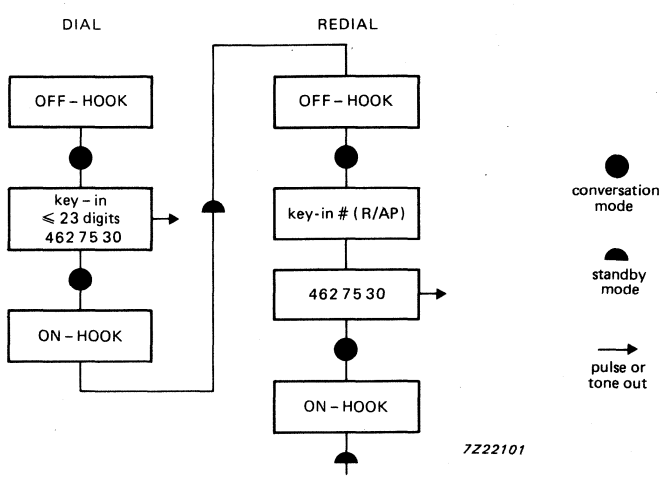


Fig. 7 Pulse/DTMF dialling mode.

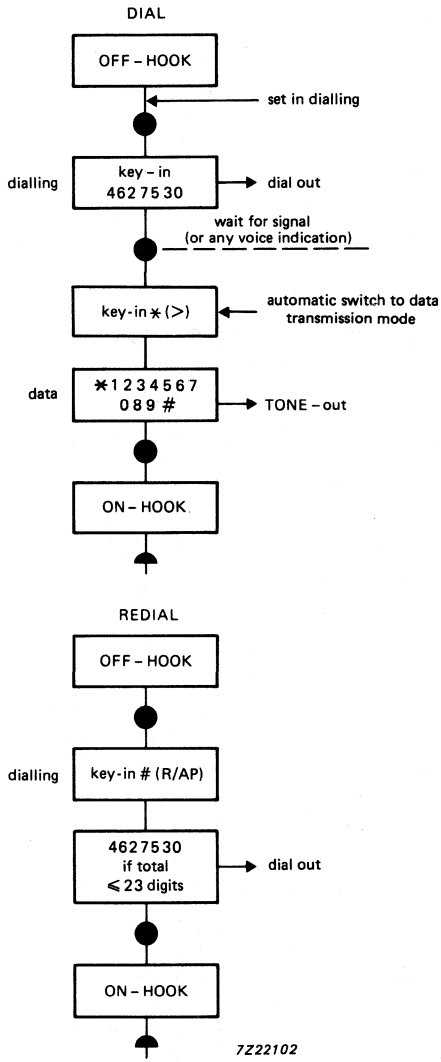


Fig. 8 Pulse/DTMF dialling and data transmission mode.

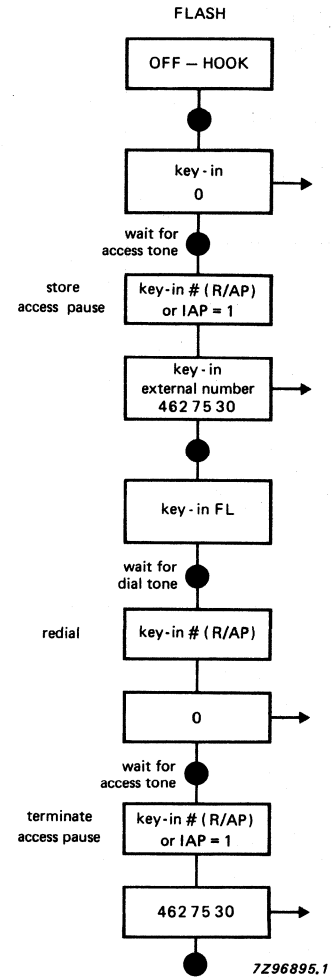


Fig. 9 Flash; independent of dialling mode.

DEVELOPMENT DATA

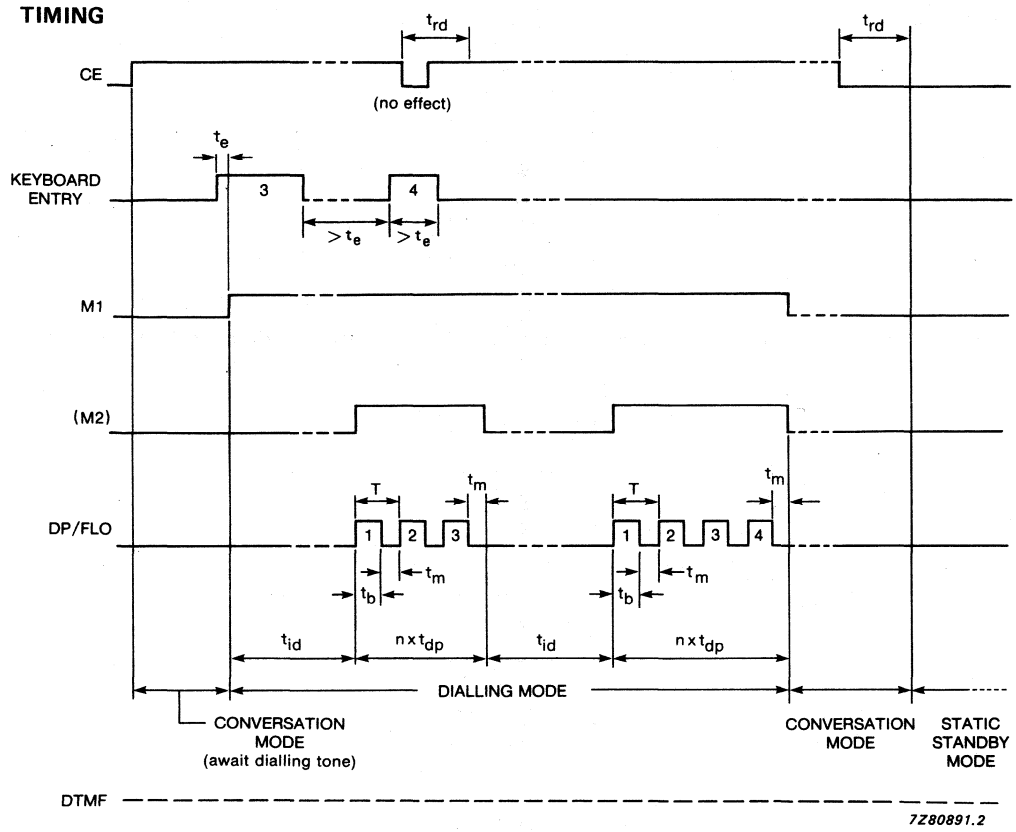


Fig. 10a Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling ($\overline{PD}$/DTMF = V_{SS}).

TIMING (continued)

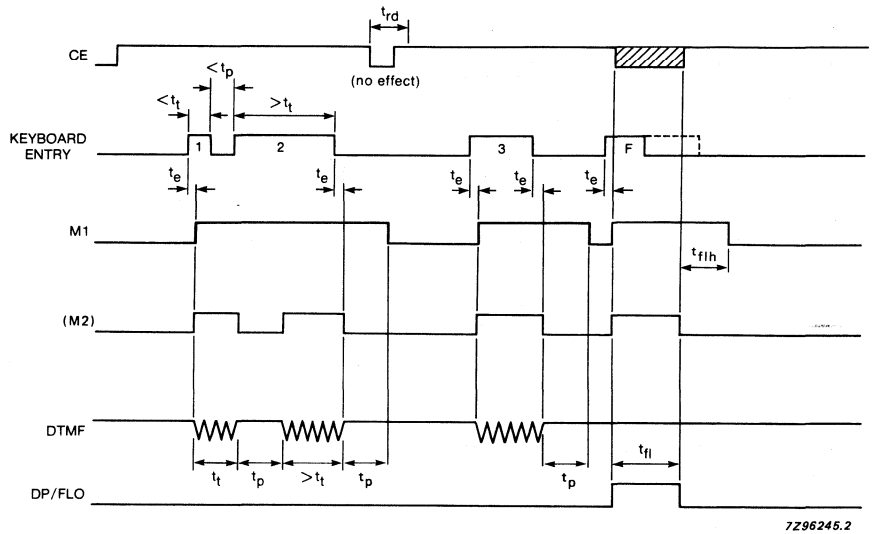


Fig. 10b Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; DTMF dialling ($\overline{PD}$/DTMF = V_{DD}).

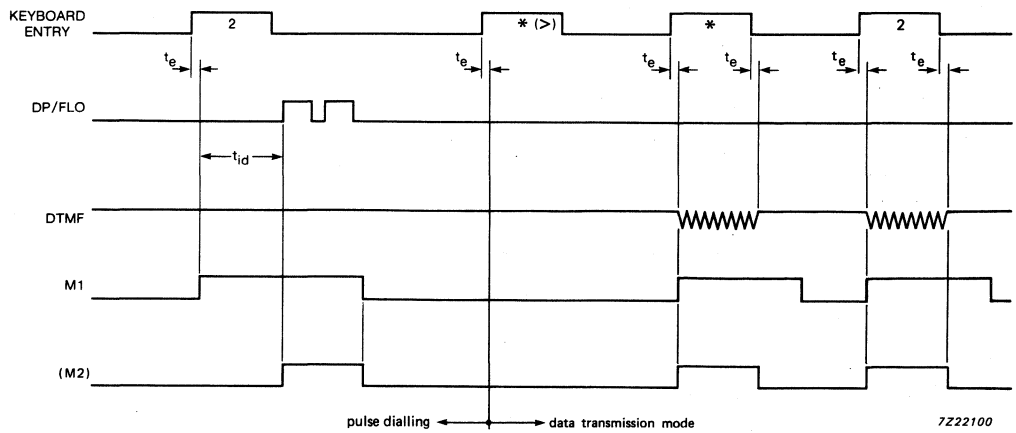


Fig. 10c Timing diagram for dialling mode defined by $\overline{PD}$/DTMF selection pin; pulse dialling and data transmission mode.

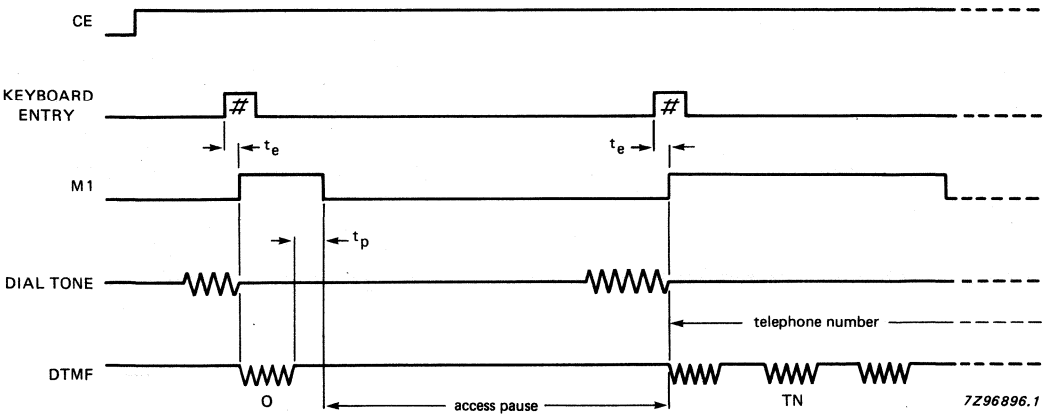


Fig. 11a Timing diagram showing REDIAL where PABX access digit(s) are the first keyboard entries and access pause is terminated by the # or R/AP key; DTMF dialling with $\overline{PD}$/DTMF = V_{DD}.

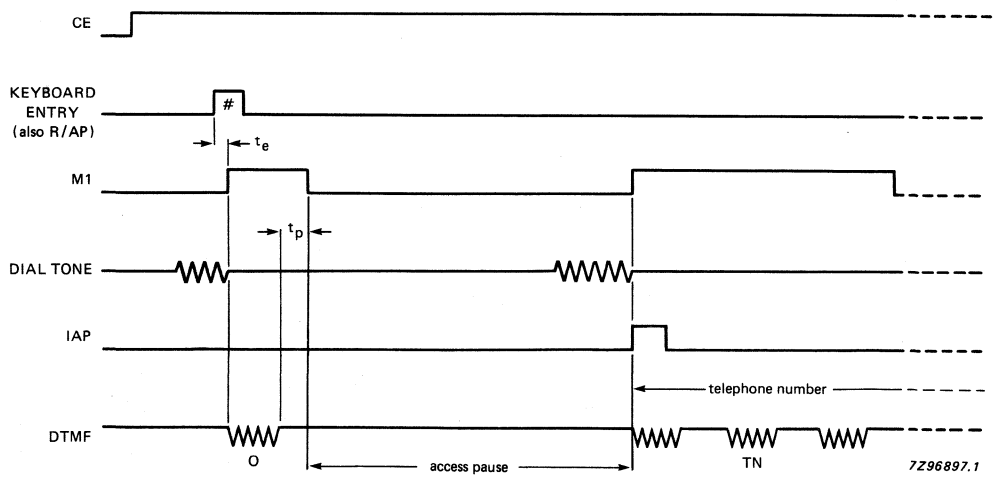


Fig. 11b Timing diagram showing REDIAL where PABX access digit(s) occur and are terminated by IAP; DTMF dialling with $\overline{PD}$/DTMF = V_{DD}.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to 8	V
Supply current	I_{DD}	max.	50	mA
DC current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8	V
Total power dissipation	P_{tot}	max.	300	mW
Power dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579545 MHz; R_S = 100 Ω max.; T_{amb} = −25 to + 70 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Standby supply voltage	V_{DDO}	1,8	–	6,0	V
Operating supply current					
conversation mode (oscillator ON)	I_{DDC}	–	–	150	μA
pulse dialling or flash	I_{DDP}	–	–	200	μA
DTMF dialling (tone ON)	I_{DDF}	–	–	0,9	mA
DTMF dialling (tone OFF)	I_{DDF}	–	–	200	μA
Standby supply current (oscillator OFF; note 1) at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DDO}	–	–	5	μA
INPUTS					
Input voltage LOW (any pin)	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH (any pin)	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current; CE	$\lvert I_{IL}\rvert$	–	–	1	μA
Keyboard inputs					
Keyboard ON resistance	R_{KON}	–	–	2	kΩ
Keyboard OFF resistance	R_{KOFF}	1	–	–	MΩ
OUTPUTS					
Output sink current at $V_{OL} = V_{SS} + 0{,}5$ V M1, M2, DP/FLO, $\overline{DP/FLO}$	I_{OL}	0,7	–	–	mA
Output source current at $V_{OH} = V_{DD} - 0{,}5$ V M1, M2, DP/FLO	$-I_{OH}$	0,6	–	–	mA
TIMING AND FREQUENCY					
Clock start-up time	t_{on}	–	4	–	ms
Debounce time	t_e	–	12	–	ms
Reset delay time	t_{rd}	152	160	168	ms

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 12) at V_{DD} = 2,5 to 6 V					
DTMF output voltage levels (r.m.s. value)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Frequency deviation	$\Delta f/f$	−0,6	−	+ 0,6	%
DC voltage level	V_{DC}	−	$\frac{1}{2}V_{DD}$	−	V
Output impedance	$\|Z_O\|$	−	0,1	0,5	kΩ
Load resistance	R_L	10	−	−	kΩ
Pre-emphasis of group	ΔV_G	1,85	2,1	2,35	dB
Total harmonic distortion at T_{amb} = 25 °C (note 2)	THD	−	−25	−	dB
Transmission and pause time (note 3)					
Manual and data transmission dialling mode	t_t	65	−	−	ms
	t_p	65	−	−	ms
Redialling	t_t	65	70	75	ms
	t_p	65	70	75	ms
Flash pulse duration	t_{FL}	252	254	256	ms
Flash hold-over time	t_{flh}	32	34	36	ms
Pulse dialling (PD) (note 3)					
Dialling pulse frequency	f_{dp}	9,8	10	10,4	Hz
Inter-digit pause	t_{id}	800	840	880	ms
Break time (note 4)	t_b	58	60	62	ms
Make time (note 4)	t_m	38	40	42	ms

Notes to the characteristics

1. Crystal connected between OSCI and OSCO; CE at V_{SS} and all other pins open-circuit.
2. Related to the level of the LOW group frequency component (CEPT CS 203).
3. Other timing is possible on request.
4. Mark-to-space ratio 2:1.

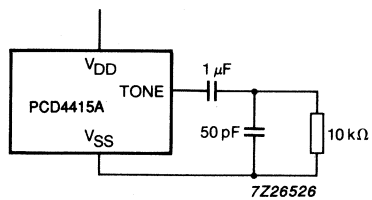
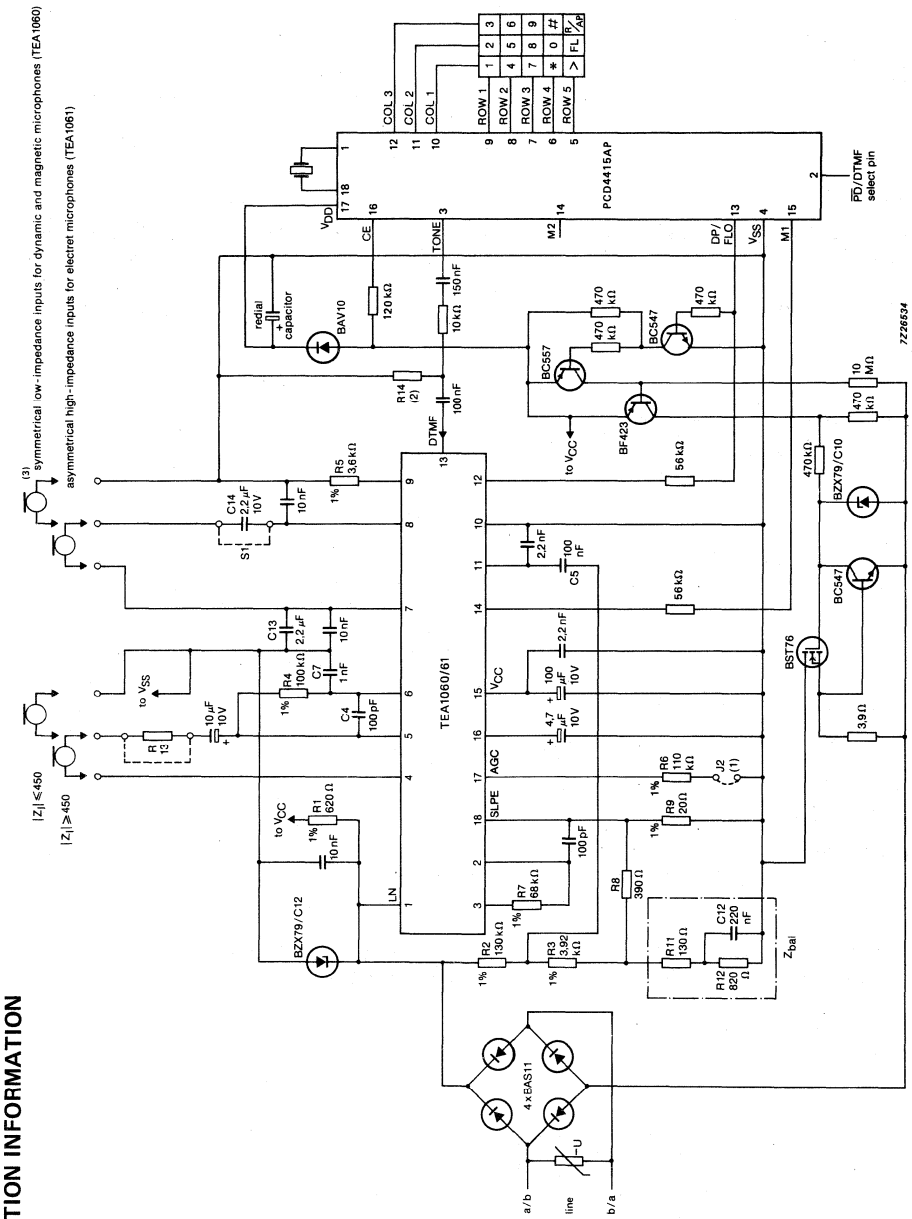


Fig. 12 Tone output test circuit.

DEVELOPMENT DATA

APPLICATION INFORMATION



(1) Automatic line compensation obtained by connecting R6 to V_{SS}.
(2) The value of resistor R14 is determined by the required level at LN and the DTMF gain of the TEA1060/61.
(3) Omit C13 and C14; insert S1.

Fig.13 Application diagram of the full electronic basic telephone set.

Philips Components

Data sheet	
status	Product specification
date of issue	September 1990

PCD4420
DTMF dialler with redial

FEATURES

- DTMF dialling
- Redial 23-digit
- Redial selected using the '#' key
- At redial after the 1st digit an access pause can be inserted
- Timing:
  - manual dialling
  - minimum duration for tone bursts and pauses
  - redial
  - calibrated timing
- On-chip voltage reference for supply and temperature independent tone-level output
- On-chip filtering for low harmonic distortion (CEPT CS 203 compatible)
- Pin selectable on-chip oscillator uses 3.58 MHz quartz or 447 kHz ceramic resonator
- Single-contact or double-contact (common left open) keyboard
- Keyboard entries fully debounced.

GENERAL DESCRIPTION

The PCD4420 is a single-chip silicon gate CMOS integrated circuit with a dual on-chip oscillator for use with a 3.58 MHz or a 447 kHz quartz or ceramic resonator. It is a standard dialling circuit for dual tone multi frequency (DTMF). Input data is derived from a standard matrix 4 x 4 keyboard for dialling. Numbers of up to 23 digits can be stored in RAM for redial facilities. The last number can be redialled using the '#' key. DTMF bursts as well as pauses are timed to a minimum, in manual dialling the maximum depends on the key depression time.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage dialling		2.5	-	6	V
V_{DDC}	supply voltage conversation		2.0	-	6	V
V_{DDO}	standby supply voltage		1.6	-	6	V
I_{DDO}	low standby current (on-hook)	V_{DDO} = 1.6 V	-	0.8	1.5	µA
Operating currents		V_{DD} = 3 V				
I_{DDC}	conversation mode	f_{osc} = 3.58 MHz	-	120	200	µA
I_{DDC}	conversation mode	f_{osc} = 447 kHz	-	120	200	µA
I_{DDF}	dialling mode	f_{osc} = 3.58 MHz	-	0.3	0.7	mA
I_{DDF}	dialling mode	f_{osc} = 447 kHz	-	0.3	0.7	mA
DTMF output voltage level						
$V_{HG(rms)}$	HIGH group		158	182	205	mV
$V_{LG(rms)}$	LOW group		125	143	160	mV
ΔV_G	pre-emphasis of group		1.75	2.0	2.25	dB
THD	total harmonic distortion		-	–25	-	dB
T_{amb}	operating ambient temperature range		–25	-	+ 70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD4420P	16	DIL	plastic	SOT38
PCD4420T	16	mini-pack	plastic	SO16L; SOT162A

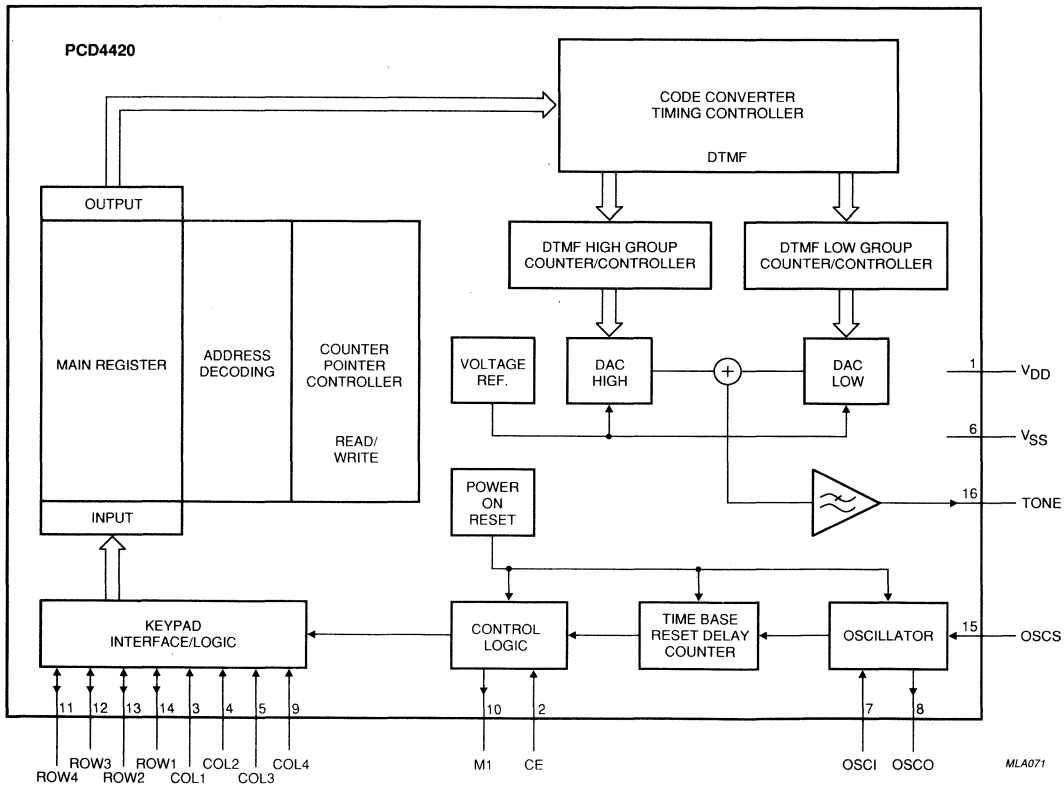


Fig.1 Block diagram.

DTMF dialler with redial PCD4420

PIN CONFIGURATION

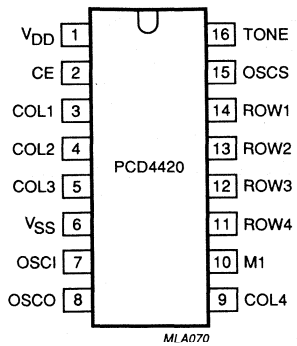


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DD}	1	positive supply
CE	2	chip enable input
COL1	3	column 1 keyboard input
COL2	4	column 2 keyboard input
COL3	5	column 3 keyboard input
VSS	6	negative supply
OSCI	7	oscillator input
OCSO	8	oscillator output
COL4	9	column 4 keyboard input
M1	10	mute
ROW4	11	row 4 keyboard output
ROW3	12	row 3 keyboard output
ROW2	13	row 2 keyboard output
ROW1	14	row 1 keyboard output
OSCS	15	select pin for 3.58 MHz or 447 kHz oscillator
TONE	16	DTMF output

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The positive supply of the circuit (V_{DD}) meets the voltage requirements as shown in the DC Characteristics. To avoid undefined states of the device when powered-up, an internal reset circuit clears the control logic and counters. If V_{DD} drops below the minimum standby supply voltage of 1.6 V the Power-on reset circuit inhibits redialling after hook-off. The Power-on reset signal has the highest priority. It blocks and resets the complete circuit without delay, regardless of the state of Chip Enable input (CE).

During the conversation mode the supply voltage may drop to a minimum of 2.0 V.

Clock oscillator (OSCI, OSCO, OSCS)

The PCD4420 has a dual on-chip oscillator. If pin 15 (OSCS) is not connected then a 3.58 MHz crystal (quartz or PXE) should be connected between pin 7 (OSCI) and pin 8 (OSCO). If pin 15 (OSCS) is connected to V_{SS} then a 447 kHz ceramic resonator should be connected between pin 7 (OSCI) and pin 8 (OSCO).

A special low cost quartz resonator, ideal for telephony applications, is available from Philips (code number 4322 143 04401).

Chip Enable (CE)

The CE input enables the circuit and is used to initialize the IC.

CE = LOW provides the static standby condition. In this state the clock oscillator is disabled, all registers and logic are reset with the exception of the Write Address Counter (WAC) which points to the last entered digit. The keyboard input is inhibited, but data previously entered is saved in the redial register providing V_{DD} is higher than $V_{DDO(min)}$. The current drawn is I_{DDO} (standby current) and serves to retain data in the redial register during hook-on.

CE = HIGH activates the clock oscillator and the circuit changes from the static standby condition to the conversation mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard; then a dialling or redialling operation starts. The operating current is I_{DDF}.

If the CE input is held LOW longer than the time period t_{rd} (see Fig.5) an internal reset pulse will be generated at the end of the t_{rd} period and the system changes to the static standby state. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses will not be generated.

Dialling mode

Each key activated corresponds to a combination of two tones, one tone from the HIGH group frequencies the other from the LOW group frequencies. These frequencies are transmitted with a constant amplitude, regardless of power supply variations. Harmonic content is filtered out thus meeting the CEPT CS 203 recommendations.

The transmission time is calibrated for redial. In manual dialling the duration of burst and pauses is the actual key depression time, but not less than the minimum transmission time (t_t) or minimum pause time (t_p).

Keyboard inputs/outputs

The sense column inputs (COL1 to COL4) and the scanning row outputs (ROW1 to ROW4) of the PCD4420 are connected to the keyboard as shown in Fig.3. All keyboard entries are debounced on both the leading and trailing edges for approximately time t_e, as shown in Fig.5. Each entry is tested for validity. When a key is depressed, keyboard scanning starts and only returns to the sense mode after release of the key.

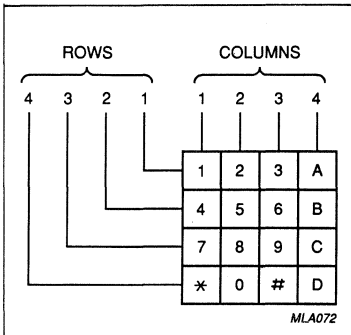


Fig.3 Keyboard.

Tone output

The single and dual tones which are provided at the Tone output are filtered by an on-chip switched-capacitor filter, followed by an on-chip active RC low-pass filter. Hence, the total harmonic distortion of the DTMF tones meets the CEPT CS 203 recommendations.

An on-chip reference voltage provides output-tone levels independent of the supply voltage and ambient temperature. Tables 1 and 2 show the frequency tolerance of the output tones for DTMF signalling.

Table 1 Frequency tolerance of the output tones for DTMF signalling; f_{OSC} = 3.579545 MHz.

ROW/COLUMN	STANDARD FREQUENCY(Hz)	TONE OUTPUT FREQUENCY (Hz)	FREQUENCY DEVIATION (%)
Row1	697	697.0	0.01
Row2	770	768.8	−0.16
Row3	852	850.7	−0.16
Row4	941	944.0	0.32
Col1	1209	1209.3	0.03
Col2	1336	1339.7	0.27
Col3	1477	1481.6	0.31
Col4	1633	1633.0	0.00

Table 2 Frequency tolerance of the output tones for DTMF signalling; f_{OSC} = 477 kHz.

ROW/COLUMN	STANDARD FREQUENCY(Hz)	TONE OUTPUT FREQUENCY (Hz)	FREQUENCY DEVIATION (%)
Row1	697	696.3	−0.11
Row2	770	768.0	−0.25
Row3	852	849.8	−0.26
Row4	941	943.0	0.22
Col1	1209	1208.1	−0.07
Col2	1336	1338.3	0.17
Col3	1477	1480.1	0.21
Col4	1633	1631.4	−0.10

DTMF tones are timed in manual dialling with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS} and Low group frequencies are generated by forcing the row to V_{DD}. The single tone frequencies will be transmitted during activation time, but are neither calibrated nor stored.

Mute output (M1)

During dialling the mute output becomes active HIGH for the period of tone transmission and remains at this level until the end of hold-over time. During redial if the '#' key is kept depressed the 1st digit is sent out. Mute will become LOW after the hold-over time until the '#' key is released.

DIALLING PROCEDURES (see Fig.4)

Dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address. By entering the first valid digit, the Write Address Counter (WAC) will be set to the first address, the decoded digit will be stored in the register and the WAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the redial register after validation. All following digits will be stored in the register (a total of not more than 23). If more than 23 digits are entered redial will be inhibited. All entries are debounced on both the leading and trailing edges for at least time t_e as shown in Fig 5. Each entry is tested for validity before being deposited in the redial register.

Redialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address to be sent. The PCD4420 is in the conversation mode. If '#' is the first keyboard entry the circuit starts redialling the contents of the register. If the overflow flag of the WAC was set in the previous dialling, the redial will be inhibited. If the '#' key is the first key pressed and is held down, dialling will stop after the first digit until the '#' key is released. Dialling will then continue. Timing is calibrated for both tone bursts and pauses.

During redial, keyboard entries are not accepted until the circuit returns to the conversation mode after completion of redialling. No redial activity takes place if one of the following events occur:

- Power-on reset.
- Memory overflow (more than 23 valid data entries).

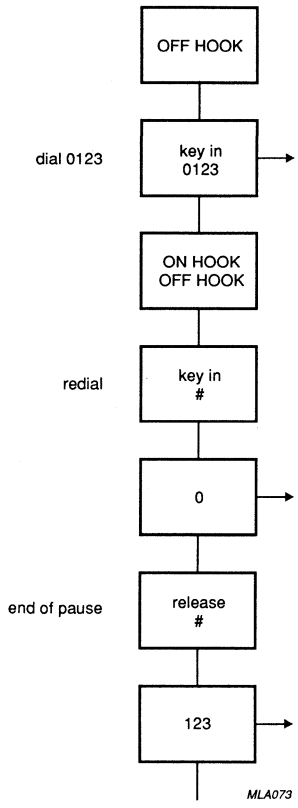


Fig.4 Redial and access pause.

TIMING

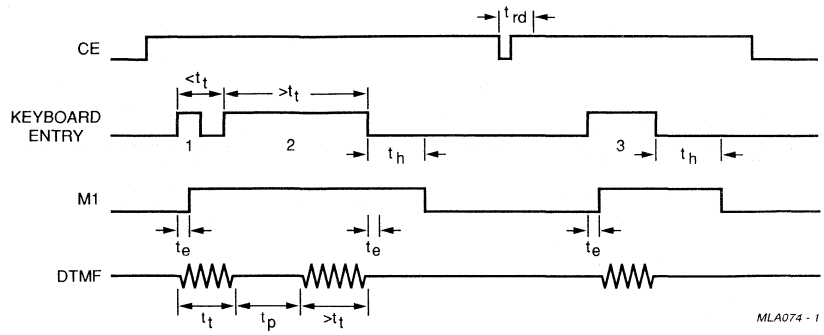


Fig.5 Timing diagram for manual dialling.

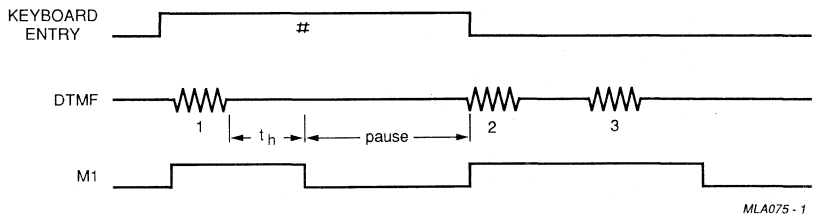


Fig.6 Timing diagram for redialling (e.g. 123 and access pause between 1 and 2)

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range	−0.8	+ 8	V
I_{DD}	supply current	-	50	mA
I_{DC}	DC current into any input or output	-	±10	mA
V_I	all input voltages	−0.8	V_{DD} + 0.8	V
P_{tot}	total power dissipation	-	300	mW
P_O	power dissipation per output	-	50	mW
T_{stg}	storage temperature range	−65	+ 150	°C
T_{amb}	operating ambient temperature range	−25	+ 70	°C

DC CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters; f_{osc} = 3.579545 MHz or 447 kHz (note 1); T_{amb} = −25 to + 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage @ dialling		2.5	-	6	V
V_{DDC}	supply voltage @ conversation		2.0	-	6	V
V_{DDO}	standby supply voltage		1.6	-	6	V
	operating supply current	f = 3.58 MHz				
I_{DDC}	conversation mode	oscillator ON	-	120	200	µA
I_{DDF}	DTMF dialling	tone ON	-	0.3	0.7	mA
I_{DDF}	DTMF dialling	tone OFF	-	150	250	µA
	operating supply current	f 447 kHz				
I_{DDC}	conversation mode	oscillator ON	-	120	200	µA
I_{DDF}	DTMF dialling	tone ON	-	0.3	0.7	mA
I_{DDF}	DTMF dialling	tone OFF	-	150	250	µA
I_{DDO}	standby supply current	V_{DD} = 1.6 V; T_{amb} = 25 °C; oscillator OFF, note 2	-	0.8	1.5	µA
Inputs						
V_{IL}	input voltage LOW (any pin)		0.0	-	0.3 V_{DD}	V
V_{IH}	input voltage HIGH (any pin)		0.7 V_{DD}	-	V_{DD}	V
$\lvert I_{IL} \rvert$	input leakage current; CE		-	-	1.0	µA
Keyboard inputs						
R_{KON}	keyboard ON resistance		-	-	2.0	kΩ
R_{KOFF}	keyboard OFF resistance		1.0	-	-	MΩ
Keyboard outputs						
I_{OL}	output sink current	V_{OL} = V_{SS} + 0.5 V	-	2.5	-	mA
$-I_{OH}$	output source current	V_{OH} = V_{DD} - 0.5 V	-	200	-	µA
Output M1						
I_{OL}	output sink current	V_{OL} = V_{SS} + 0.5 V	0.7	-	-	mA
$-I_{OH}$	output source current	V_{OH} = V_{DD} - 0.5 V	0.6	-	-	mA
Oscillator transconductance						
gm	oscillator transconductance		60	160	-	µA/V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Tone output (see Fig.7)		VDD = 2.5 to 6V				
	DTMF output voltage levels					
VHG(rms)	HIGH group		158	182	205	mV
$V_{LG(rms)}$	LOW group		125	143	160	mV
$\Delta f/f$	frequency deviation		−0.26	-	0.31	%
V_{DC}	DC voltage level		-	$0.67V_{DD}$	-	V
$\|Z_O\|$	output impedance		-	0.1	0.5	kΩ
ΔV_G	pre-emphasis of group		1.75	2	2.25	dB
THD	total harmonic distortion	T_{amb} = 25 °C; note 3	-	−25	-	dB
Timing						
t_{on}	clock start-up time		-	4	-	ms
t_e	debounce time		-	12	-	ms
t_{rd}	reset delay time		160	-	176	ms
Transmission and pause time						
t_t, t_p	manual dialling	note 4	68	-	-	ms
t_t, t_p	redialling	note 4	68	70	72	ms
t_h	holdover time (muting on M1)		-	80	-	ms

Notes to the DC characteristics

1. Recommended resonator types:
   - 3.58 MHz quartz : Philips 4322 143 04401
   - 3.58 MHz PXE : Murata CSA 3.58MG310VA
   - 447 kHz PXE : tbf
2. Resonator connected between OSCI and OSCO; CE at V_{SS} and all other pins open-circuit.
3. Related to the level of the LOW group frequency component (CEPT CS 203).
4. On request a 100 ms tone burst; $t_t = t_p = t_h$ = 100 ms.

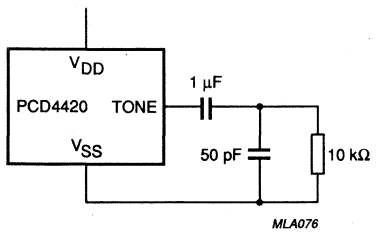


Fig.7 Tone output test circuit.

Philips Components

Data sheet	
status	Product specification
date of issue	October 1990

PCD4421

DTMF dialler with redial

FEATURES

- DTMF dialling
- Redial 23-digit
- Redial is selected using the 'R' key
- Four extra function keys: access pause, flash, redial and disconnect
- Manual access pause inserted using the 'AP' key
- Flash (register recall) using the 'FL' key
- Disconnected selected with the 'DI' key
- DTMF timing: - manual dialling
  - minimum duration for tone bursts and pauses
  - redial
  - calibrated timing
- On-chip voltage reference for supply and temperature independent tone-level output
- On-chip filtering for low harmonic distortion (CEPT CS 203 compatible)
- Dual on-chip oscillator uses 3.58 MHz quartz or 447 kHz ceramic resonator
- Single-contact or double-contact (common left open) keyboard
- Keyboard entries fully debounced.

GENERAL DESCRIPTION

The PCD4421 is a single-chip silicon gate CMOS integrated circuit with a dual on-chip oscillator for use with a 3.58 MHz or a 447 kHz quartz or ceramic resonator. It is a standard dialling circuit for dual tone multi frequency (DTMF). Input data is derived from a standard matrix 4 x 5 keyboard for dialling. Numbers of up to 23 digits can be stored in RAM for redial facilities. The last number can be redialled using the 'R' key. DTMF bursts as well as pauses are timed to a minimum, in manual dialling the maximum depends on the key depression time.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage dialling		2.5	-	6	V
V_{DDC}	supply voltage conversation		2	-	6	V
V_{DDO}	standby supply voltage		1.6	-	6	V
I_{DDO}	low standby current (on-hook)	V_{DDO} = 1.6 V	-	0.8	1.5	µA
Operating currents		V_{DDO} = 1.6 V				
I_{DDC}	conversation mode	f_{osc} = 3.58 MHz	-	120	200	µA
I_{DDC}	conversation mode	f_{osc} = 447 kHz	-	120	200	µA
I_{DDF}	dialling mode	f_{osc} = 3.58 MHz	-	300	700	µA
I_{DDF}	dialling mode	f_{osc} = 447 kHz	-	300	700	µA
DTMF output voltage level						
$V_{HG(rms)}$	HIGH group		158	182	205	mV
$V_{LG(rms)}$	LOW group		125	143	16	mV
ΔV_G	pre-emphasis of group		1.75	2	2.25	dB
THD	total harmonic distortion		-	–25	-	dB
T_{amb}	operating ambient temperature range		–25	-	+ 70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD4421P	18	DIL	plastic	SOT102
PCD4421T	20	mini-pack	plastic	SO20; SOT163A

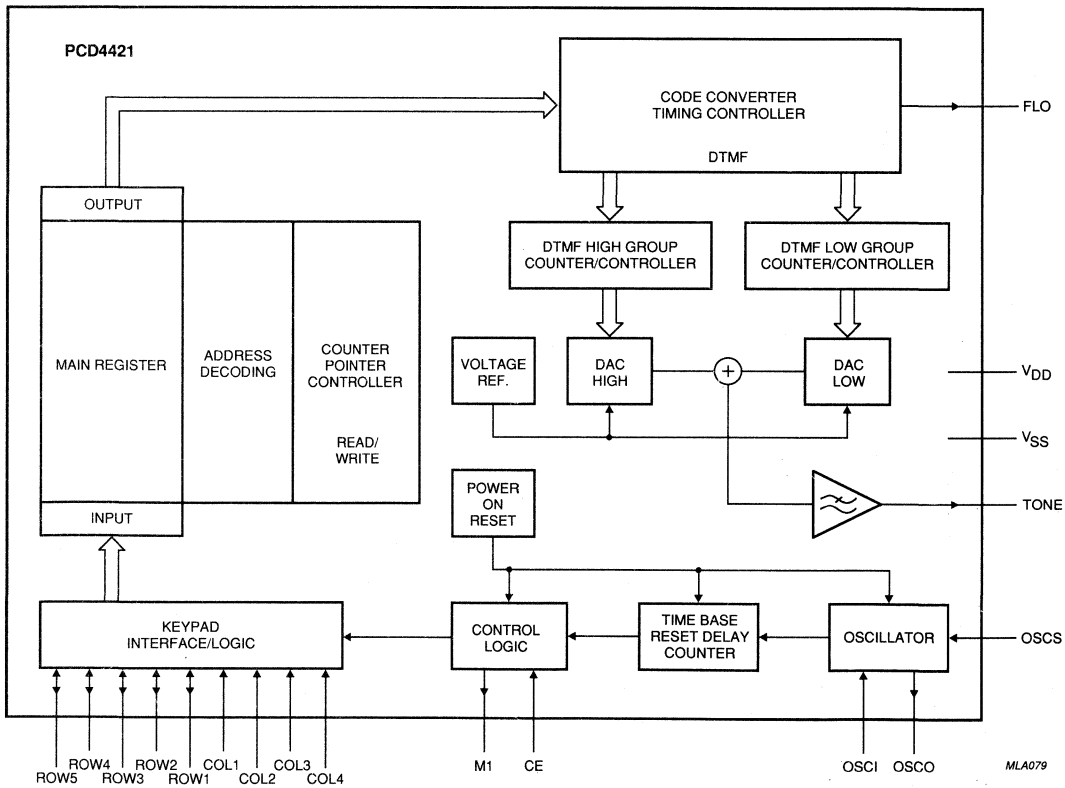


Fig.1 Block diagram PCD4421 DTMF generator.

DTMF dialler with redial PCD4421

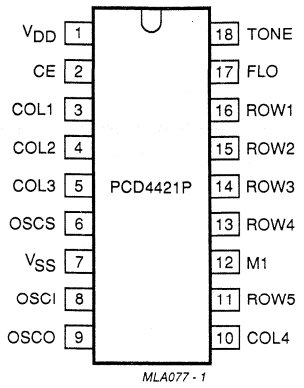


Fig.2 Pinning diagram of the PCD4421P.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DD}	1	positive supply
CE	2	chip Enable input
COL1	3	column 1 keyboard input
COL2	4	column 2 keyboard input
COL3	5	column 3 keyboard input
OSCS	6	select pin for 3.58 MHz or 447 kHz oscillator
VSS	7	negative supply
OSCI	8	oscillator input
OSCO	9	oscillator output
COL4	10	column 4 keyboard input
ROW5	11	row 5 keyboard output
M1	12	muting output
ROW4	13	row 4 keyboard output
ROW3	14	row 3 keyboard output
ROW2	15	row 2 keyboard output
ROW1	16	row 1 keyboard output
FLO	17	flash/disconnect output
TONE	18	single or dual tone frequency output

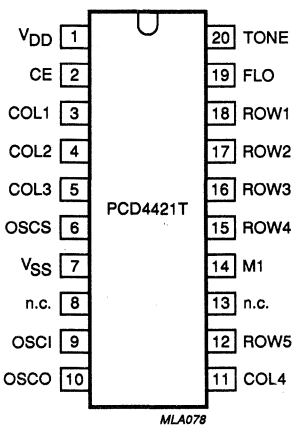


Fig.3 Pinning diagram of the PCD4421T.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DD}	1	positive supply
CE	2	chip Enable input
COL1	3	column 1 keyboard input
COL2	4	column 2 keyboard input
COL3	5	column 3 keyboard input
OSCS	6	select pin for 3.58 MHz or 447 kHz oscillator
VSS	7	negative supply
n.c.	8	not connected
OSCI	9	oscillator input
OSCO	10	oscillator output
COL4	11	column 4 keyboard input
ROW5	12	row 5 keyboard output
n.c.	13	not connected
M1	14	muting output
ROW4	15	row 4 keyboard output
ROW3	16	row 3 keyboard output
ROW2	17	row 2 keyboard output
ROW1	18	row 1 keyboard output
FLO	19	flash/disconnect output
TONE	20	single or dual tone frequency output

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The positive supply of the circuit (V_{DD}) meets the voltage requirements as indicated in the DC Characteristics. To avoid undefined states of the device when powered-up, an internal reset circuit clears the control logic and counters. If V_{DD} drops below the minimum standby supply voltage of 1.6 V the Power-on-reset circuit inhibits redialling after hook-off. The Power-on-reset signal has the highest priority. It blocks and resets the complete circuit without delay regardless of the state of chip enable input (CE).

During conversation mode the supply voltage may drop to a minimum of 2.0 V.

Clock oscillator (OSCI, OSCO, OSCS)

The PCD4421 has a dual on-chip oscillator. If pin-OSCS is left open then a 3.58 MHz crystal (quartz or PXE) resonator should be connected between the OSCI and OSCO pins. If pin-OSCS is wired to V_{SS} then a 447 kHz ceramic resonator should be connected between pins OSCI and OSCO.

A special low cost quartz resonator, ideal for telephony applications, is available from Philips (code number 4322 143 04401).

Chip Enable (CE)

The CE input enables the circuit and is used to initialize the IC.

CE = LOW provides the static standby condition. In this state the clock oscillator is disabled and all registers and logic are reset with the exception of the Write Address Counter (WAC) which points to the last entered digit. The keyboard input is inhibited, but data previously entered is saved in the redial register providing V_{DD} is higher than $V_{DDO(min)}$. The current drawn is I_{DDO} (standby current) and serves to retain data in the redial register during hook-on.

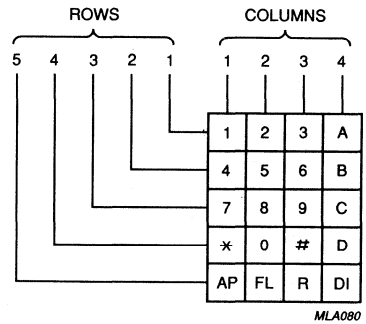
CE = HIGH activates the clock oscillator and the circuit changes from the static standby condition to the conversation mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard; then a dialling or redialling operation starts. The operating current is I_{DDF}.

If the CE input is held LOW longer than the time period t_{rd} (see Fig.6) an internal reset pulse will be generated at the end of the t_{rd} period and the system changes to the static standby state. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses will not be generated. During Flash the delayed reset procedure is not affected.

Dialling mode

Each key activated corresponds to a combination of two tones, one tone from the HIGH group frequencies, the other from the LOW group frequencies. These frequencies are transmitted with a constant amplitude, regardless of power supply variations. Harmonic content is filtered out thus meeting CEPT CS 203 recommendations.

The transmission time is calibrated for redial. In manual dialling the duration of burst and pauses is the actual key depression time, but not less than the minimum transmission time (t_t) or minimum pause time(t_p).



AP = Access pause
FL = Flash or register recall
R = Redial
DI = Disconect

Fig.4 Keyboard.

Keyboard inputs/outputs

The sense column inputs (COL1 to COL4) and the scanning row outputs (ROW1 to ROW5) of the PCD4421 are connected to the keyboard as shown in Fig.4. All keyboard entries are debounced on both the leading and trailing edges for approximately time t_e as shown in Fig.6. Each entry is tested for validity. When a key is pressed, keyboard scanning starts and only returns to the sense mode after release of that key.

In dialling mode the valid keys are the 10 numeric keys (0-9) and the non-numeric keys *, #, A, B, C and D. They are transmitted as dual tone combinations and at the same time stored in the redial register. The function keys are AP, FL, R and DI.

Flash

Flash or register recall is activated by the 'FL' key. Pressing the 'FL' key will produce a timed line-break of 100 ms at the FLO output. The 'FL' entry is not stored in the redial memory but will reset the Read Address Counter thus acting as a chip enable (CE). Later redial is possible with the after "Flash" inserted telephone number. The counter of the reset delay timer is stopped during the period t_{fl}.

Disconnect

Disconnect is activated by the 'DI' key. Pressing this key will produce a line-break at the FLO output until the key is released. The 'DI' entry is not stored in the redial memory but will reset the Read Address Counter thus acting as a chip enable (CE). Later redial is possible with the after "Disconnect" inserted telephone number. The counter of the reset delay timer is stopped during the disconnect operation.

Mute input function (optional)

Instead of the 'AP' key, the 'FL' key or 'DI' key may be chosen for a 'MU' key. The initial depression of the 'MU' key will cause the Mute output M1 to go high, pressing again will return M1 to its LOW state. The 'MU' key operates as a toggle switch for the Mute output M1.

Tone output

The single and dual tones provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an on-chip active RC low-pass filter. Hence, the low total harmonic distortion of the DTMF tones meets the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage and ambient temperature. Tables 1 and 2 show the frequency tolerance of the output tones for DTMF signalling.

DTMF tones are timed in manual dialling with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS} and Low group frequencies are generated by forcing the row to V_{DD}. The single tone frequencies will be transmitted during activation time but are neither calibrated nor stored.

Mute output (M1)

During dialling the mute output becomes active HIGH for the period of tone transmission and remains at this level until the end of hold-over time. The Mute output is also active HIGH during Flash and Flash hold-over time. During redial if the 'R' key is kept depressed, the 1st digit is sent out and the Mute output becomes LOW after hold-over time and will remain LOW until the 'R' key is released. At redial during access pauses the Mute output is LOW.

Table 1 Frequency tolerance of the output tones for DTMF signalling; f_{OSC} = 3.579545 MHz.

ROW/COLUMN	STANDARD FREQUENCY (Hz)	TONE OUTPUT FREQUENCY (Hz)	FREQUENCY DEVIATION (%)
Row1	697	697.0	0.01
Row2	770	768.8	−0.16
Row3	852	850.7	−0.16
Row4	941	944.0	0.32
Col1	1209	1209.3	0.03
Col2	1336	1339.7	0.27
Col3	1477	1481.6	0.31
Col4	1633	1633.0	0.00

Table 2 Frequency tolerance of the output tones for DTMF signalling; f_{OSC} = 477 kHz.

ROW/COLUMN	STANDARD FREQUENCY (Hz)	TONE OUTPUT FREQUENCY (Hz)	FREQUENCY DEVIATION (%)
Row1	697	696.3	−0.11
Row2	770	768.0	−0.25
Row3	852	849.8	−0.26
Row4	941	943.0	0.22
Col1	1209	1208.1	−0.07
Col2	1336	1338.3	0.17
Col3	1477	1480.1	0.21
Col4	1633	1631.4	−0.10

DIALLING PROCEDURES

Dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address. By entering the first valid digit (not the 'R' key), the Write Address Counter (WAC) will be set to the first address, the decoded digit will be stored in the register and the WAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the redial register aftervalidation. All following digits (0-9, *, #, AP) will be stored in the register (a total of not more than 23). The manual inserted access pauses are considered as digits. If more than 23 digits are entered redial will be inhibited. All entries are debounced on both the leading and trailing edges for at least the time period t_e as shown in Fig.6. Each entry is tested for validity before being deposited in the redial register.

Redialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address to be sent. The PCD4421 is in the conversation mode. If 'R' is the first keyboard entry the circuit starts redialling the contents of the register. If the overflow flag of the WAC was set in the previous dialling, the redial will be inhibited. If the 'R' key is the first key pressed and is held down, dialling will stop after the first digit but will continue when the key is released. Timing is calibrated for both tone bursts and pauses.

During redial, keyboard entries are not accepted until the circuit returns to the conversation mode after completion of redialling. No redial activity takes place if one of the following events occur:

- Power-on reset.
- Memory overflow (more than 23 valid data entries).

ACCESS PAUSE

During manual dialling access pauses can be programmed by the 'AP' key for later redial:

- the number of access pauses is unlimited, the total is 23 digits plus access pauses
- consecutive pauses will be stored as a single pause.

During redial the transmission of digits is stopped if:

- an access pause is detected (maximum 2 seconds)
- the 'R' key is kept depressed then only the first digit will be transmitted; transmission continues when the 'R' key is released.

During redial the termination of access pauses occurs:

- after 2 seconds.
- if during the pause the 'R' key is depressed
- an automatic inserted access pause (see redial procedures) is terminated after release of the 'R' key.

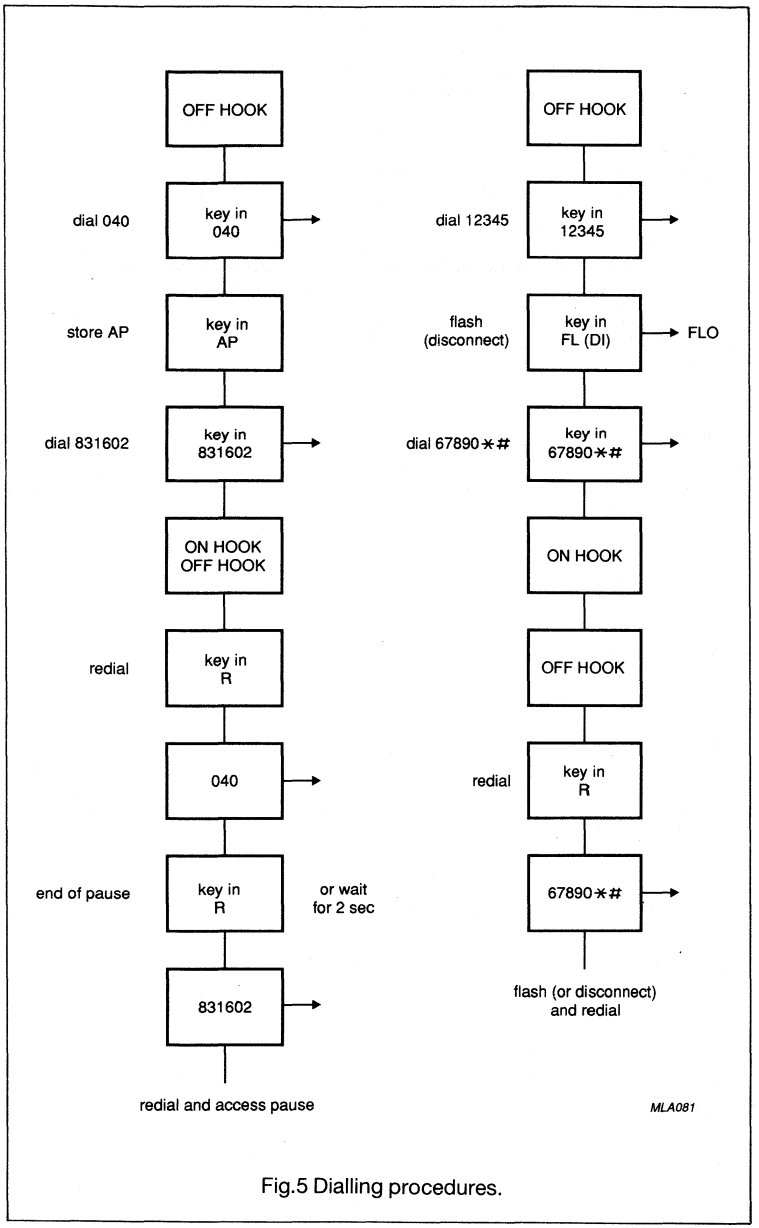


Fig.5 Dialling procedures.

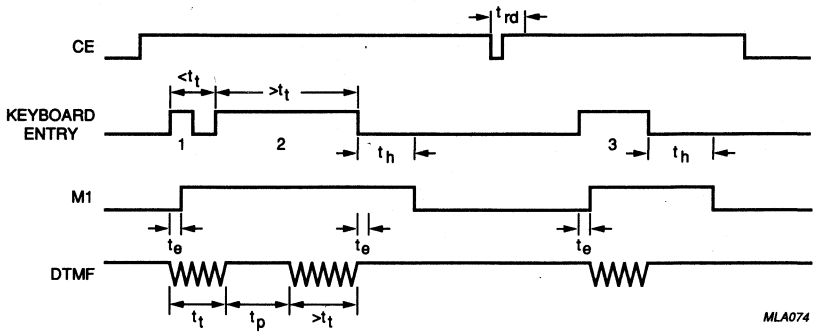


Fig.6 Timing diagram for manual dialling.

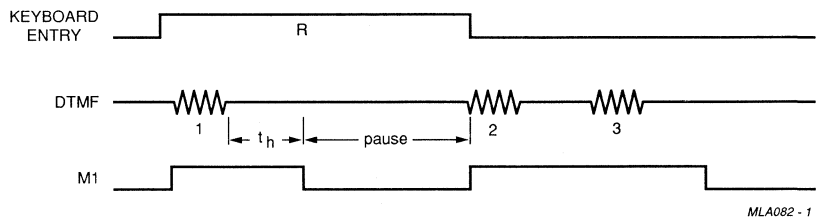


Fig.7 Timing diagram for redialling (e.g. 123 and access pause between 1 and 2).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range	−0.8	+ 8	V
I_{DD}	supply current	-	50	mA
I_{DC}	DC current into any input or output	-	±10	mA
V_I	all input voltages	−0.8	V_{DD} + 0.8	V
P_{tot}	total power dissipation	-	300	mW
P_O	power dissipation per output	-	50	mW
T_{stg}	storage temperature range	−65	+ 150	°C
T_{amb}	operating ambient temperature range	−25	+ 70	°C

DC CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters; f_{osc} = 3.579545 MHz or 447 kHz (note 1); T_{amb} = −25 to + 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage @ dialling		2.5	-	6	V
V_{DDC}	supply voltage @ conversation		2.0	-	6	V
V_{DDO}	standby supply voltage		1.6	-	6	V
	operating supply current	f = 3.58 MHz				
I_{DDC}	conversation mode	oscillator ON	-	120	200	µA
I_{DDF}	DTMF dialling	tone ON	-	300	700	µA
I_{DDF}	DTMF dialling	tone OFF	-	150	250	µA
	operating supply current	f = 447 kHz				
I_{DDC}	conversation mode	oscillator ON	-	120	200	µA
I_{DDF}	DTMF dialling	tone ON	-	300	700	µA
I_{DDF}	DTMF dialling	tone OFF, note 2	-	150	250	µA
I_{DDO}	standby supply current	V_{DD} = 1.6 V; T_{amb} = 25 °C; oscillator OFF, note 3	-	0.8	1.5	µA
Inputs						
V_{IL}	input voltage LOW (any pin)		0.0	-	0.3 V_{DD}	V
V_{IH}	input voltage HIGH (any pin)		0.7 V_{DD}	-	V_{DD}	V
$\|I_{IL}\|$	input leakage current; CE		-	-	1	µA
Keyboard inputs						
R_{KON}	keyboard ON resistance		-	-	2	kΩ
R_{KOFF}	keyboard OFF resistance		1	-	-	MΩ
Keyboard outputs						
I_{OL}	output sink current	$V_{OL} = V_{SS}$ + 0.5 V	-	2.5	-	mA
$-I_{OH}$	output source current	$V_{OH} = V_{DD}$ - 0.5 V	-	200	-	µA
Output M1, FLO						
I_{OL}	output sink current	$V_{OL} = V_{SS}$ + 0.5 V	0.7	-	-	mA
$-I_{OH}$	output source current	$V_{OH} = V_{DD}$ - 0.5 V	0.6	-	-	mA
Oscillator transconductance						
gm	oscillator transconductance		60	160	-	µA/V
Tone output		V_{DD} = 2.5 V to 6 V				
	DTMF output voltage levels					
VHG(rms)	HIGH group		158	182	205	mV
$V_{LG(rms)}$	LOW group		125	143	160	mV
Δf/f	frequency deviation		−0.26	-	0.31	%
V_{DC}	DC voltage level		-	0.67V_{DD}	-	V
$\|Z_O\|$	output impedance		-	0.1	0.5	kΩ
ΔV_G	pre-emphasis of group		1.75	2	2.25	dB
THD	total harmonic distortion	T_{amb} = 25 °C; note 4	-	−25	-	dB
Timing						
t_{on}	clock start-up time		-	4	-	ms
t_e	debounce time		-	12	-	ms
t_{rd}	reset delay time		160	-	176	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Transmission and pause time						
t_t, t_p	manual dialling	note 4	68	-	-	ms
t_t, t_p	redialling	note 4	68	70	72	ms
t_h	holdover time (muting on M1)		-	80	-	ms
t_{FL}	flash pulse duration	note 5	-	100	-	ms
t_{FLh}	flash holdover		-	34	-	ms
t_{ap}	access pause duration		-	-	2	s

Notes to the DC characteristics

1. Recommended resonator types:
   - 3.58 MHz quartz : Philips 4322 143 04401
   - 3.58 MHz PXE : Murata CSA 3.58MG310VA
   - 447 kHz PXE : tbf
2. No key depressed.
3. Resonator connected between OSCI and OSCO; CE at V_{SS} and all other pins open-circuit.
4. Related to the level of the LOW group frequency component (CEPT CS 203).
5. On-request also 100 ms tone burst; $t_t = t_p = t_h = 100$ ms.
6. On-request also 256 ms flash duration.

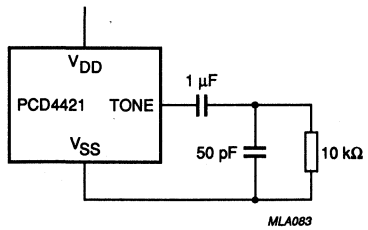


Fig.8 Tone output test circuit: V_{DD} = 2.5 to 6 V.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

256 × 4-BIT STATIC RAM

GENERAL DESCRIPTION

The PCD5101 is a very low-power 1024-bit static CMOS random access memory, organized as 256 words by 4 bits. It is suitable for low power and high speed applications where battery standby power is required to ensure non-volatility of data. All inputs and outputs are fully TTL compatible and pinning is compatible with 2101-type NMOS static RAMs and 5101-type CMOS static RAMs.

There are two chip enable inputs, $\overline{CE1}$ and CE2, selection being made when $\overline{CE1}$ is LOW and CE2 is HIGH. The memory has an output disable function, OD, which allows the inputs/outputs to be used separately, or to be tied together for use in common data I/O systems.

Features

- Operating supply voltage range — 2,5 to 5,5 V
- Low data retention voltage — min. 1 V
- Low power consumption in both operating and standby modes
- Access time 150 ns at V_{DD} = 5 V; 400 ns at V_{DD} = 3 V
- Three-state outputs
- All inputs and outputs directly TTL compatible
- Choice of two package types

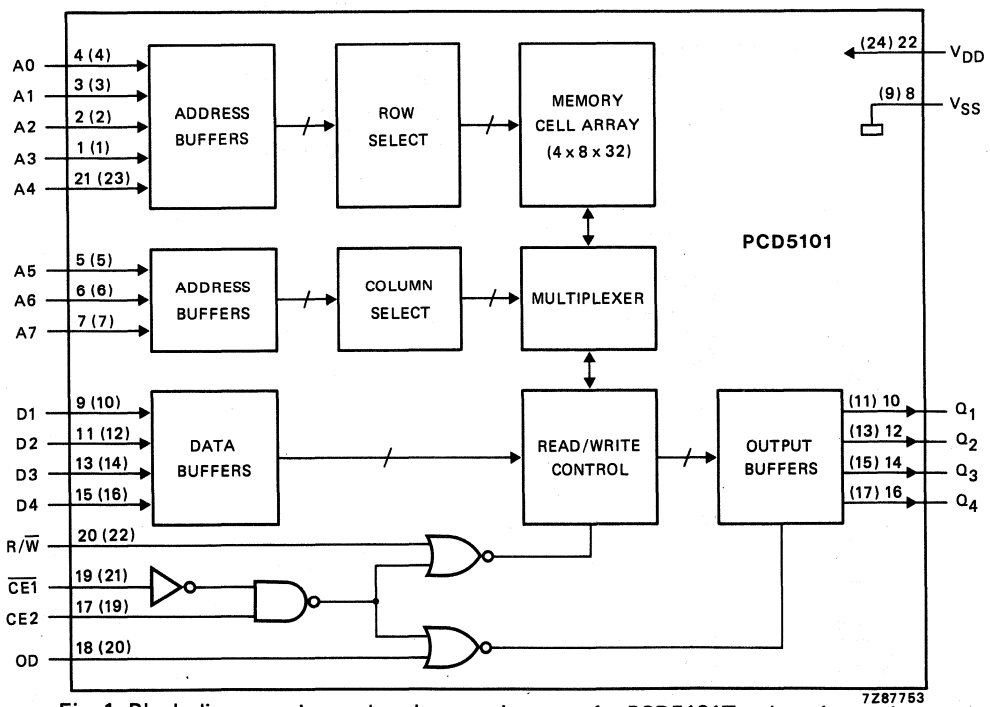


Fig. 1 Block diagram: pin numbers in parentheses are for PCD5101T; other pin numbers are applicable to PCD5101P.

PACKAGE OUTLINES

PCD5101P: 22-lead DIL; plastic (SOT116).
PCD5101T: 24-lead mini-pack; plastic (SO24; SOT137A).

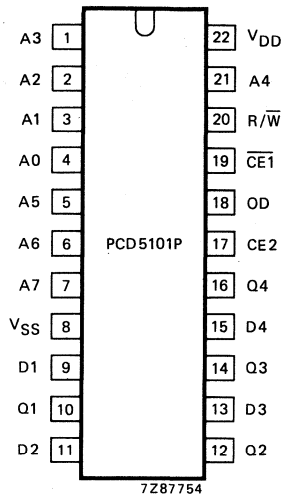


Fig. 2 Pinning diagram for PCD5101P.

PINNING

D1, D2, D3, D4	data inputs
A0, A1, A2, A3, A4, A5, A6, A7	address inputs
R/$\overline{W}$	read/write input
$\overline{CE1}$, CE2	chip enable inputs
OD	output disable
Q1, Q2, Q3, Q4	data outputs
V_{DD}	positive supply
V_{SS}	negative supply
n.c.	not connected

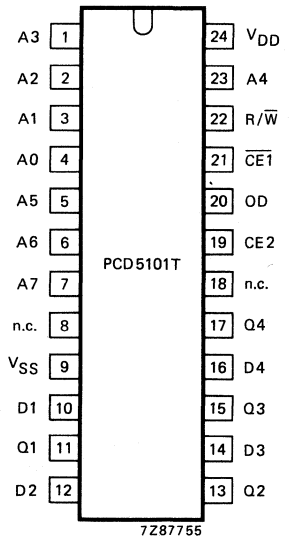


Fig. 3 Pinning diagram for PCD5101T.

D.C. CHARACTERISTICS (V_{DD} = 5 V)

V_{DD} = 5 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	4,5	5,0	5,5	V
Operating supply current					
at V_I = V_{DD} or V_{SS}; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 or 2,0 V; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 or 2,0 V; f = 5 MHz; outputs open	I_{DD}	–	12	20	mA
Standby supply current at CE2 = V_{SS}	I_{SB}	–	0,02	5,0	μA
Input leakage current at V_I = V_{SS} to V_{DD}	$\|I_{IL}\|$	–	–	0,1	μA
Input voltage LOW	V_{IL}	−0,3	–	+0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}+0,3	V
Output leakage current at V_O = V_{SS} to V_{DD}; OD = HIGH or chip disabled	$\|I_{OL}\|$	–	–	0,2	μA
Output voltage LOW at I_{OL} = 4,0 mA	V_{OL}	–	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 2,0 mA	V_{OH}	2,4	–	–	V

D.C. CHARACTERISTICS (V_{DD} = 3 V)

V_{DD} = 3 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	3,0	3,5	V
Operating supply current					
at V_I = V_{DD} or V_{SS}; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
at V_I = 0,4 or 1,6 V; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
Standby supply current at CE2 = V_{SS}	I_{SB}	–	0,02	5,0	μA
Input leakage current at V_I = V_{SS} to V_{DD}	$\|I_{IL}\|$	–	–	0,1	μA
Input voltage LOW	V_{IL}	−0,3	–	+0,4	V
Input voltage HIGH	V_{IH}	1,6	–	V_{DD}+0,3	V
Output leakage current at V_O = V_{SS} to V_{DD}; OD = HIGH or chip disabled	$\|I_{OL}\|$	–	–	0,2	μA
Output voltage LOW at I_{OL} = 1,0 mA	V_{OL}	–	–	0,3	V
Output voltage HIGH at $-I_{OH}$ = 1,0 mA	V_{OH}	1,7	–	–	V

A.C. TEST CONDITIONS (V_{DD} = 5 V)

Input pulse levels	0,8 V to 2,0 V
Input rise and fall times	5 ns
Input timing reference levels	1,5 V
Output timing levels	1,5 V
Output timing levels for high/low impedance	1,2 V and 2,8 V
Output load (2 TTL inputs and load capacitance C_L)	Fig. 4

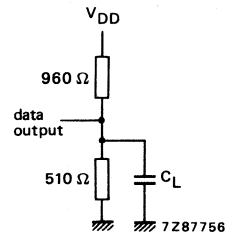


Fig. 4 Test load.

A.C. CHARACTERISTICS (V_{DD} = 5 V)

V_{DD} = 5 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; loads as per Fig. 4 with C_L = 100 pF unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	150	–	–	ns
Address access time	t_{AA}	–	–	150	ns
Chip enable $\overline{CE1}$ to output	t_{CO1}	–	–	150	ns
Chip enable CE2 to output	t_{CO2}	–	–	150	ns
Output disable OD to output	t_{OD}	–	–	70	ns
Data output to high impedance state at C_L = 5 pF	t_{DF}	10	–	70	ns
Previously read data valid with respect to address change	t_{OH1}	10	–	–	ns
Previously read data valid with respect to chip enable	t_{OH2}	10	–	–	ns
Write cycle					
Write cycle time	t_{WC}	150	–	–	ns
Write delay time	t_{AW}	0	–	–	ns
Chip enable $\overline{CE1}$ to write	t_{CW1}	120	–	–	ns
Chip enable CE2 to write	t_{CW2}	120	–	–	ns
Data set-up time	t_{DW}	70	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Write pulse duration	t_{WP}	70	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Output disable OD set-up time	t_{DS}	70	–	–	ns

A.C. TEST CONDITIONS (V_{DD} = 3 V)

Input pulse levels	0,4 V to 1,6 V
Input rise and fall times	5 ns
Input timing reference levels	1,0 V
Output timing levels	1,0 V
Output timing levels for high/low impedance	0,7 V and 1,7 V
Output load	Fig. 5

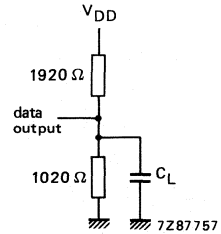


Fig. 5 Test load.

A.C. CHARACTERISTICS (V_{DD} = 3 V)

V_{DD} = 3 ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; loads as per Fig. 5 with C_L = 100 pF unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	400	–	–	ns
Address access time	t_{AA}	–	–	400	ns
Chip enable $\overline{CE1}$ to output	t_{CO1}	–	–	400	ns
Chip enable CE2 to output	t_{CO2}	–	–	400	ns
Output disable OD to output	t_{OD}	–	–	200	ns
Data output to high impedance state at C_L = 5 pF	t_{DF}	10	–	200	ns
Previously read data valid with respect to address change	t_{OH1}	10	–	–	ns
Previously read data valid with respect to chip enable	t_{OH2}	10	–	–	ns
Write cycle					
Write cycle time	t_{WC}	400	–	–	ns
Write delay time	t_{AW}	0	–	–	ns
Chip enable $\overline{CE1}$ to write	t_{CW1}	300	–	–	ns
Chip enable CE2 to write	t_{CW2}	300	–	–	ns
Data set-up time	t_{DW}	200	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Write pulse duration	t_{WP}	200	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Output disable OD set-up time	t_{DS}	200	–	–	ns

LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS

$CE2 \leqslant 0{,}2$ V; $T_{amb} = -25$ to $+70$ °C.

parameter	symbol	min.	typ.	max.	unit
Supply voltage for data retention	V_{DR}	1,0	–	5,5	V
Data retention current at V_{DD} = 1,5 V	I_{DR}	–	0,02	2,0	μA
Chip deselect to data retention time	t_{CDR}	0	–	–	ns
Operation recovery time	t_R	0	–	–	ns

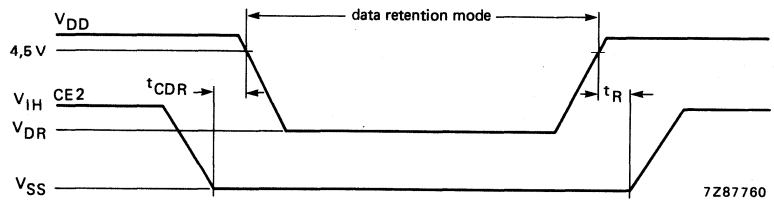


Fig. 8 Low supply voltage data retention characteristics.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

1024 x 4-BIT STATIC RAM

GENERAL DESCRIPTION

The PCD5114 is a low-power, high-speed 4096-bit static CMOS RAM, organized as 1024 words of 4 bits each. The IC is suitable for low power and high speed applications, for battery operation and where battery backup is required. Inputs R/$\overline{W}$ and $\overline{CE}$ control the read/write operation and standby mode respectively. The PCD5114 is pin compatible with the SBB2114 types.

Features

- Operating supply voltage — 2,5 V to 5,5 V
- Low data retention voltage — min. 1,0 V
- Low standby current — max. 5 μA
- Cycle time = access time — max. 200 ns
- Static operation requiring no clock or timing strobe
- Low power consumption
- 3-state common data input/output interface
- All inputs and outputs directly TTL compatible
- Pin compatible with SBB2114 variants
- 18-lead DIL package
- 20-lead SO package

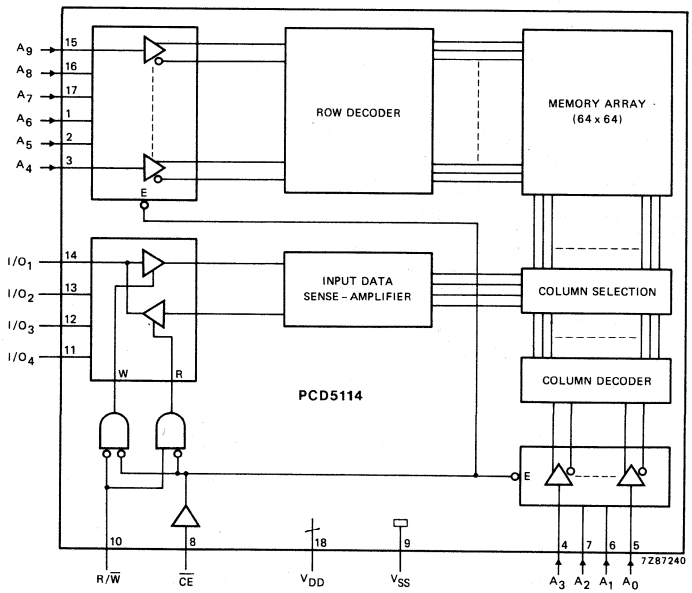


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCD5114D: 18-lead DIL; ceramic (cerdip) (SOT133B).
PCD5114P: 18-lead DIL; plastic (SOT102G).
PCD5114T: 20-lead mini-pack; plastic (SO20; SOT163A).

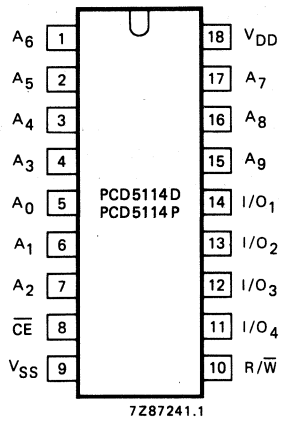


Fig. 2 Pinning diagram: PCD5114D; PCD5114P.

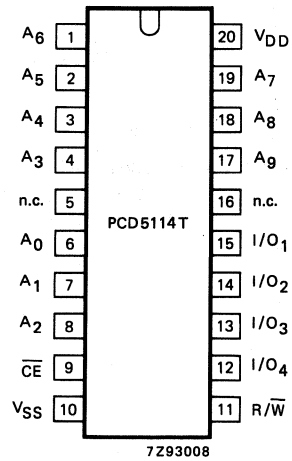


Fig. 3 Pinning diagram: PCD5114T.

A_0 to A_3	column address inputs
A_4 to A_9	row address inputs
$\overline{CE}$	chip enable input
$R/\overline{W}$	read/write input
I/O_1 to I/O_4	data input/output
V_{SS}	negative supply (ground)
V_{DD}	positive supply (+ 5 V)

Table 1 Mode selection

$\overline{CE}$	$R/\overline{W}$	mode	output	power
H	H	not selected	high impedance	standby
H	L	not selected	high impedance	standby
L	H	read	active	active
L	L	write	high impedance	active

H = HIGH logic level (the most positive voltage)
L = LOW logic level (the most negative voltage)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to + 8 V
Input voltage range (any pin)	V_I	V_{SS}−0,3 to V_{DD} + 0,3 V
Storage temperature range	T_{stg}	−55 to + 125 °C
Operating ambient temperature range	T_{amb}	−25 to + 70 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{DD} = 5 V ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply current					
at $V_I = V_{DD}/V_{SS}$; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 V/2,0 V; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 V/2,0 V; f = 5 MHz; outputs open	I_{DD}	–	12	20	mA
Standby current					
at $\overline{CE} = V_{DD}$	I_{SB}	–	0,02	5	μA
Input voltage HIGH	V_{IH}	2,0	–	V_{DD} + 0,3	V
Input voltage LOW	V_{IL}	−0,3	–	+0,8	V
Input leakage current					
at $V_I = V_{SS}$ to V_{DD}	$\pm I_{IL}$	–	–	0,1	μA
Output voltage HIGH					
at $-I_{OH}$ = 2 mA	V_{OH}	2,4	–	–	V
Output voltage LOW					
at I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
Output leakage current					
at $V_O = V_{SS}$ to V_{DD}; $\overline{CE}$ = HIGH	$\pm I_{OL}$	–	–	0,5	μA

D.C. CHARACTERISTICS

V_{DD} = 3 V ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply current					
at $V_I = V_{DD}/V_{SS}$; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
at V_I = 0,4 V/1,6 V; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
Standby current					
at $\overline{CE} = V_{DD}$	I_{SB}	–	0,02	5	μA
Input voltage HIGH	V_{IH}	1,6	–	V_{DD} + 0,3	V
Input voltage LOW	V_{IL}	−0,3	–	+0,4	V
Input leakage current					
at $V_I = V_{SS}$ to V_{DD}	$\pm I_{IL}$	–	–	0,1	μA
Output voltage HIGH					
at $-I_{OH}$ = 1 mA	V_{OH}	1,7	–	–	V
Output voltage LOW					
at I_{OL} = 1 mA	V_{OL}	–	–	0,3	V
Output leakage current					
at $V_O = V_{SS}$ to V_{DD}; $\overline{CE}$ = HIGH	$\pm I_{OL}$	–	–	0,5	μA

A.C. CHARACTERISTICS

V_{DD} = 5 V ±0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; measured in Fig. 4, C_L = 100 pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	200	–	–	ns
Address access time	t_{AA}	–	–	200	ns
Chip select access time	t_{AC}	–	–	200	ns
Output hold from address change	t_{OHA}	20	–	–	ns
Output hold from chip select	t_{OHC}	20	–	–	ns
Output to low impedance from chip selection at C_L = 5 pF	t_{CLZ}	20	–	–	ns
Output to high impedance from chip deselection at C_L = 5 pF	t_{CHZ}	–	–	80	ns
Write cycle					
Write cycle time	t_{WC}	200	–	–	ns
Chip selection to end of write	t_{CW}	120	–	–	ns
Address set-up time	t_{AS}	0	–	–	ns
Write pulse duration	t_{WP}	140	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Data set-up time	t_{DS}	80	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Output to high impedance from write enabled at C_L = 5 pF	t_{WZ}	–	–	60	ns
Output active from end of write at C_L = 5 pF	t_{RZ}	20	–	–	ns

A.C. TEST CONDITIONS (see Fig. 4)

Input pulse levels	0,8 V to 2,0 V
Input rise and fall times	5 ns
Input timing reference levels	1,5 V
Output timing levels	1,5 V
Output timing levels for high/low impedance	1,2 V and 2,8 V
Output load	2 TTL gates and C_L = 100 pF

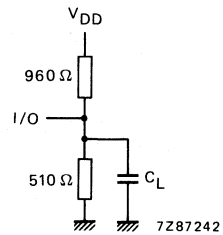


Fig. 4 Load for a.c. test conditions (V_{DD} = 5 V ± 0,5 V).

DEVELOPMENT DATA

A.C. CHARACTERISTICS

V_{DD} = 3 V ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70°C; measured in Fig. 5, C_L = 100 pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	500	–	–	ns
Address access time	t_{AA}	–	–	500	ns
Chip select access time	t_{AC}	–	–	500	ns
Output hold from address change	t_{OHA}	20	–	–	ns
Output hold from chip select	t_{OHC}	20	–	–	ns
Output to low impedance from chip selection at C_L = 5 pF	t_{CLZ}	20	–	–	ns
Output to high impedance from chip deselection at C_L = 5 pF	t_{CHZ}	–	–	200	ns
Write cycle					
Write cycle time	t_{WC}	500	–	–	ns
Chip selection to end of write	t_{CW}	300	–	–	ns
Adress set-up time	t_{AS}	0	–	–	ns
Write pulse duration	t_{WP}	350	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Data set-up time	t_{DS}	200	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Output to high impedance from write enabled at C_L = 5 pF	t_{WZ}	–	–	150	ns
Output active from end of write at C_L = 5 pF	t_{RZ}	20	–	–	ns

A.C. TEST CONDITIONS (see Fig. 5)

Input pulse levels	0,4 V to 1,6 V
Input rise and fall times	5 ns
Input timing reference levels	1,0 V
Output timing levels	1,0 V
Output timing levels for high/low impedance	0,7 V and 1,7 V
Output load	2 TTL gates and C_L = 100 pF

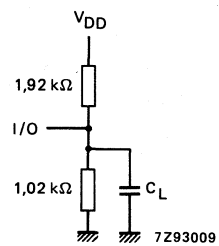


Fig. 5 Load for a.c. test conditions (V_{DD} = 3 V ± 0,5 V).

CAPACITANCE

$f = 1$ MHz; $T_{amb} = 25\ ^{o}C$

parameter	symbol	min.	typ.	max.	unit
Input capacitance at $V_I = V_{SS}$	C_I	–	–	5	pF
Output capacitance at $V_O = V_{SS}$	C_O	–	–	5	pF

LOW V_{DD} DATA RETENTION CHARACTERISTICS

$T_{amb} = -25$ to $+70\ ^{o}C$

parameter	symbol	min.	typ.	max.	unit
V_{DD} for data retention at $\overline{CE} = V_{DDR} \pm 0{,}2$ V; $V_I = V_{DDR}$ to V_{SS}	V_{DDR}	1	–	5,5	V
Data retention current at $V_{DDR} = 1{,}5$ V	I_{DDR}	–	0,02	2	μA
Chip deselect to data retention time	t_{CR}	0	–	–	ns
Operation recovery time	t_R	0	–	–	ns

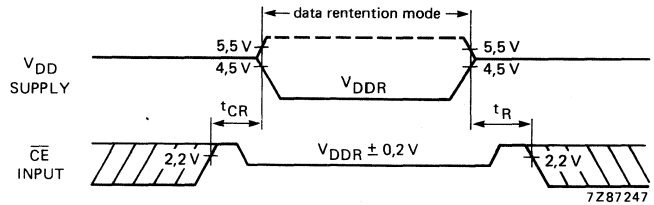


Fig. 10 LOW V_{DD} data retention.

MICROPOWER DC VOLTAGE DETECTOR

GENERAL DESCRIPTION

The PCF1251 is a CMOS micropower DC voltage detector and it is especially designed for power-on/off voltage detection monitoring and reset. The IC has an extremely low current consumption and is therefore particularly suited for battery operated applications. The internal bandgap reference voltage is stable with temperature variations. The voltage trip-point and the hysteresis can be set independently with external resistors. Two of the four outputs can be delayed with an external capacitor.

Features

- Extremely low current consumption
- Built-in bandgap voltage reference
- Wide range of voltage trip-points
- Two pairs of outputs; one pair with delay possibility
- 8-lead DIL or SO8 mini-pack (plastic packages).

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range with respect to V_{SS}	V_{DD}	1	–	6	V
Supply current	I_{DD}	–	1	–	μA
Output currents at V_{DD} = 1 V	I_O	–	2	–	mA
Bandgap voltage reference at 25 °C	V_{REF}	1,05	1,15	1,25	V

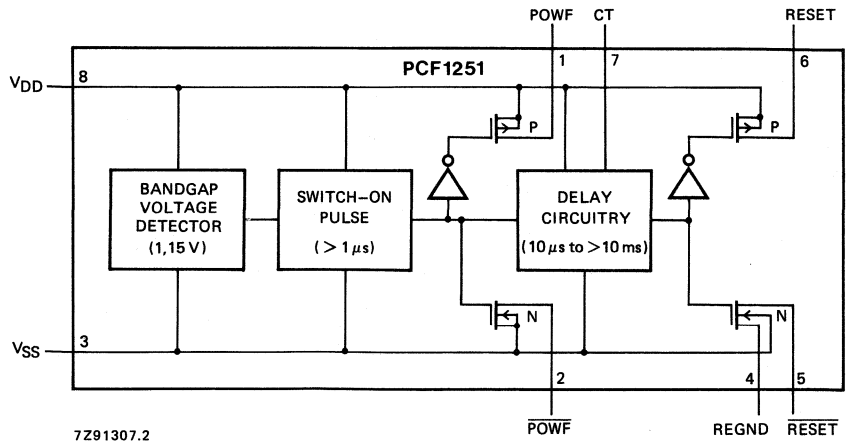


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF1251P: 8-lead DIL; plastic (SOT97).
PCF1251T: 8-lead mini-pack; plastic (SO8; SOT96A).

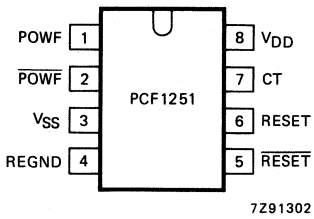


Fig. 2 Pinning diagram.

PINNING

1	POWF	power-fail output
2	$\overline{\text{POWF}}$	power-fail output (inverted)
3	V_{SS}	negative supply voltage
4	REGND	reset ground
5	$\overline{\text{RESET}}$	reset output (inverted; delayed)
6	RESET	reset output (delayed)
7	CT	capacitor for additional delay
8	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

The PCF1251 consists of a bandgap voltage reference, a comparator and delay circuitry (see Fig. 1). The supply voltage of the circuit (V_{DD} with respect to V_{SS}) is compared with an internal bandgap voltage reference by means of a special comparator. This comparator is connected to the circuit supply voltage. As long as the supply voltage is above the reference voltage level, the four open-drain outputs are all switched off and an extended drain-source voltage of up to 6 V is allowed. When the supply voltage is reduced and reaches the reference voltage level (V_{REF}), the power-fail outputs are switched on (p-channel for POWF and n-channel for $\overline{\text{POWF}}$ outputs). After a delay, determined by an external capacitor between pins CT and V_{DD}, the outputs RESET and $\overline{\text{RESET}}$ are switched on. The same delay will be active when the supply voltage is increased again and exceeds the internal voltage reference, resulting in switching off the outputs.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage with respect to V_{SS}	V_{DD}	–	8	V
Output voltage at pin 2 V_{DD} with respect to V_2	V_2	–	8	V
Output voltage at pin 5 (pin 4 at V_{SS}) V_{DD} with respect to V_5	V_5	–	8	V
Output voltage at pin 1 V_1 with respect to V_{SS}	V_1	–	8	V
Output voltage at pin 6 V_6 with respect to V_{SS}	V_6	–	8	V
Voltage at pin 7 (CT)	V_7	−0,5	V_{DD} + 0,5	V
Current at pin 7 (CT)	I_7	–	20	mA
Output currents at pins 1, 2, 5 and 6	$\lvert I_O \rvert$	–	25	mA
Total power dissipation	P_{tot}	–	150	mW
Operating ambient temperature range	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−55	+125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 1 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	1	–	6	V
Operating supply current V_{DD} = 6 V; all outputs open	I_{DD}	–	1	3	μA
Bandgap voltage reference; T_{amb} = 25 °C	V_{REF}	1,05	1,15	1,25	V
V_{REF} temperature coefficient	$\Delta V_{REF}/\Delta T$	–	−0,4	–	mV/K
Output current at pins 2 and 5 T_{amb} = 25 °C; $V_{DD} < V_{REF}$; V_O = 0,4 V with respect to V_{SS}	I_O	1	2	–	mA
Output current at pins 1 and 6 T_{amb} = 25 °C; $V_{DD} < V_{REF}$; $-V_O$ = 0,4 V with respect to V_{DD}	$-I_O$	1	2	–	mA

(1) For correct switching of the outputs the slew rate of the supply voltage should be less than 1 V/ms.

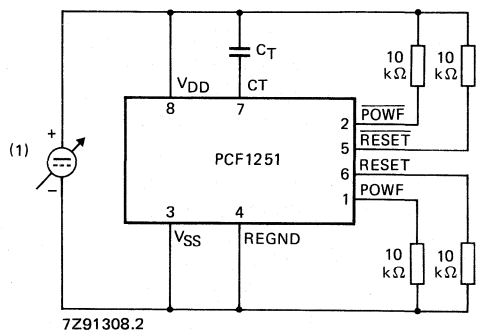


Fig. 3 Test circuit for timing measurements.

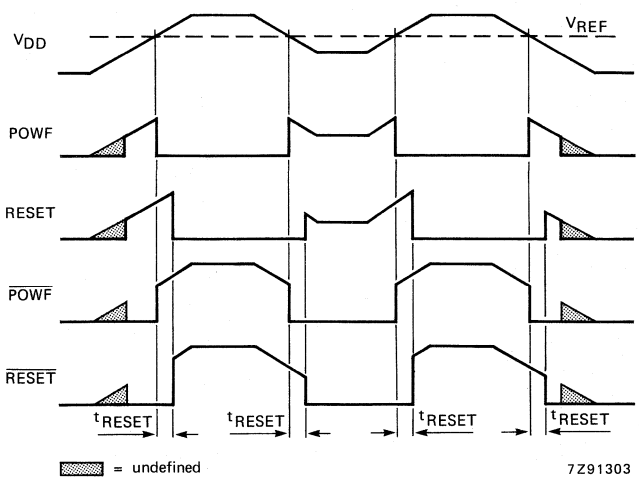


Fig. 4 Timing diagram for slow supply voltage changes.

(1) at $T_{amb} = 25\ ^{o}C$

a) $C_T < 0.1$ nF: $10\ \mu s < t_{RESET} < 750\ \mu s$

b) $C_T \geqslant 0.1$ nF: $t_{RESET} = \left[0{,}1 + 3{,}2\ ms \times C_T\left(\frac{nF}{nF}\right)\right]^{+75\%}_{-50\%}$

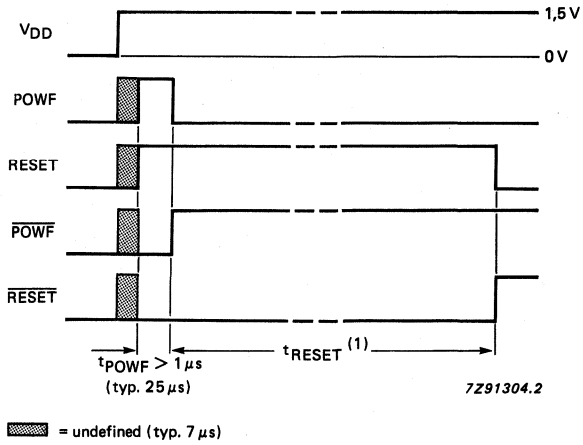


Fig. 5 Timing diagram for fast supply voltage switching on (non-repetitive).

APPLICATION INFORMATION

(1) The value of capacitor C is chosen to limit the slew rate of the supply voltage to less than 1 V/ms (e.g. the hysteresis voltage step on resistor R3).

(2) CT (pin 7) is a high-impedance connection for the capacitor C_T. This capacitor adds to the reset delay time provided by an internal current source (120 nA) and capacitor. Care must be taken to avoid external leakage current at this pin but the pin should not be left open circuit as stray capacitances to V_{SS} can then disturb the delay function.

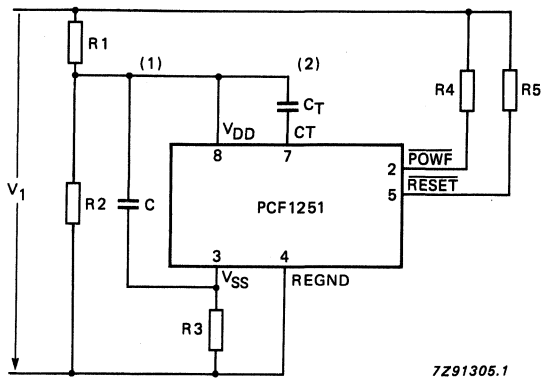


Fig. 6 Application circuit diagram.

(1) $V_{HYST} = V_{TRIP} \times \frac{R3}{R3 + R4}$; (0,2 V max.)

(2) $V_{TRIP} = V_{REF} \times \frac{R1 + R2}{R2}$

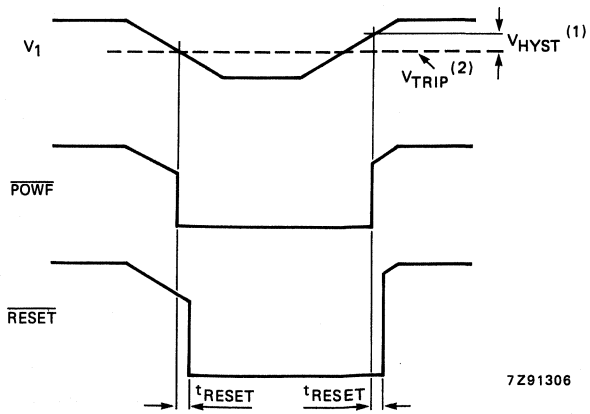


Fig. 7 Timing diagram for the circuit of Fig. 6.

POWER FAILURE DETECTOR AND RESET GENERATOR

GENERAL DESCRIPTION

The PCF1252-X family are CMOS voltage detectors designed especially for power-ON/OFF detection in microcontroller/microprocessor systems (for initialization and data storage purposes). The output $\overline{\text{POWF}}$ is activated at a precise, temperature stable, trip-point. The RESET output has a built-in delay with duration determined by an external capacitor (C_{CT}). A second comparator (comparator 2) has been included to allow for the possibility of a second monitoring point in the system.

Features

- Low current consumption, typically 6 μA
- 10 versions available, trip-points vary from 2.55 V to 4.75 V
- Temperature stable trip-point
- Variable RESET delay
- Reset polarity selection
- Comparator for second level detection (e.g. overvoltage detection)
- Advance warning of power failure

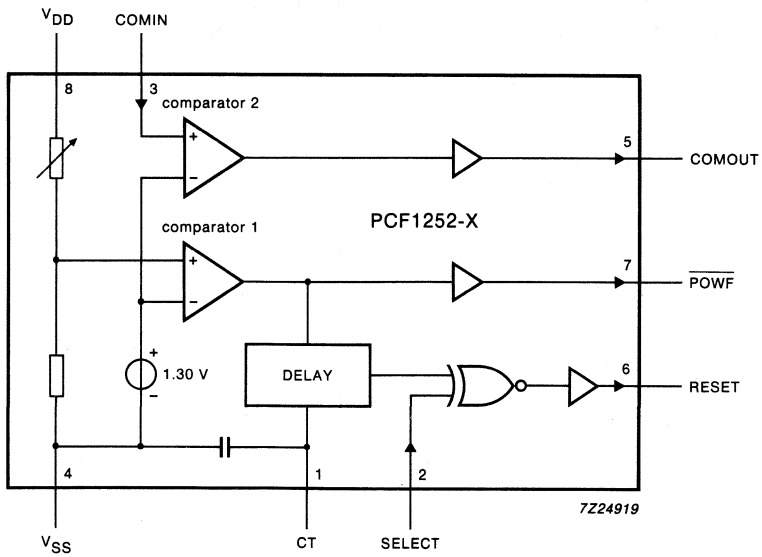


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF1252-XP: 8-lead DIL; plastic (SOT97).
PCF1252-XT: 8-lead mini-pack; plastic (SO8; SOT96A).

PINNING

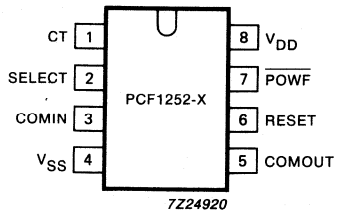


Fig.2 Pinning diagram.

pin no.	mnemonic	description
1	CT	connection for the external capacitor
2	SELECT	select polarity or external reset input
3	COMIN	comparator input
4	V_{SS}	ground (0 V)
5	COMOUT	comparator output
6	RESET	reset output
7	$\overline{POWF}$	power failure signal output
8	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION (see Fig.1)

The PCF1252-X contains a precise factory-programmed voltage reference, two comparators and a delay circuit. The PCF1252-X family is comprised of 10 versions with varying voltage trip-points (V_{TRIP}), see section "Characteristics".

Supply

The supply voltage (V_{DD}) is internally divided before being compared, via comparator 1, with the internal reference voltage.

$\overline{POWF}$ (see Fig.3)

The $\overline{POWF}$ output is:

- LOW, if V_{DD} is below V_{TRIP}.
- HIGH, if V_{DD} is above V_{TRIP}.

Power-ON reset (SELECT = LOW)

As V_{DD} rises past V_{TRIP}, a positive reset pulse is generated at RESET. The duration of the reset pulse (t_R) is determined by the value of the external capacitor (C_{CT}; maximum 1 μF, see Fig.8) connected to CT. With no external capacitor connected, C_{CT} assumes a minimum value of 100 pF. If SELECT is HIGH, the reset pulse is inverted.

Power failure

During a power-OFF condition ($V_{DD} < V_{TRIP}$), $\overline{POWF}$ goes LOW. After a time delay (t_S), also determined by C_{CT}, RESET goes HIGH. Any $\overline{POWF}$ output ($V_{DD} < V_{TRIP}$) will result in a subsequent RESET pulse.

Voltage trip-point

By selecting the voltage trip-point slightly higher than the minimum operating voltage of the microcontroller/microprocessor, there is sufficient time for data storage before the power actually fails.

In order to prevent oscillations around the voltage trip-point, a small hysteresis has been included, resulting in a power-ON switching point that is higher than the voltage trip-point (minimum of 15 mV). The voltage trip-point refers to the value at which power-OFF is signalled.

COMIN

Input to the second comparator (comparator 2). When used in conjunction with an external voltage divider, this allows a second point in the system to be monitored. This input has no built-in hysteresis. When not in use connect to V_{DD}. COMOUT will be LOW or HIGH depending on the voltage at COMIN:

- COMOUT = HIGH, if voltage at COMIN is above the switch point V_{SP} (typically 1.30 V).
- COMOUT = LOW, if voltage at COMIN is below the switch point V_{SP} (typically 1.30 V).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0.5	+ 7	V
Input voltage range		V_I	−0.5	V_{DD} + 0.5	V
DC clamp-diode current	all pins; $V_I < -0.5$ V or $> V_{DD}$ + + 0.5 V	I_I	–	20	mA
Output current		I_O	–	20	mA
Total power dissipation		P_{tot}	–	150	mW
Storage temperature range		T_{stg}	−65	+ 100	°C
Operating ambient tempetature range		T_{amb}	−40	+ 85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

CHARACTERISTICS (see Fig.3)

V_{DD} = 2.4 V to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 °C to + 85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{DD}	2.4	–	6.0	V
Voltage trip-point:	T_{amb} = + 25 °C					
PCF1252-0		V_{TRIP}	4.70	4.75	4.80	V
PCF1252-1		V_{TRIP}	4.50	4.55	4.60	V
PCF1252-2		V_{TRIP}	4.20	4.25	4.30	V
PCF1252-3		V_{TRIP}	4.00	4.05	4.10	V
PCF1252-4		V_{TRIP}	3.70	3.75	3.80	V
PCF1252-5		V_{TRIP}	3.50	3.55	3.60	V
PCF1252-6		V_{TRIP}	3.20	3.25	3.30	V
PCF1252-7		V_{TRIP}	3.00	3.05	3.10	V
PCF1252-8		V_{TRIP}	2.70	2.75	2.80	V
PCF1252-9		V_{TRIP}	2.50	2.55	2.60	V
Supply current	T_{amb} = + 25 °C; see Figs 4 and 5 V_{DD} = V_{TRIP} + 0.5 V; COMIN = V_{DD}	I_{DD}	–	6	10	μA
Voltage trip-point temperature coefficient	note 1	ΔV_{TRIP}	–	±100 x 10^{-6}	±400 x 10^{-6}	/K
Voltage trip-point hysteresis		V_H	15	30	50	mV
COMIN switch point	T_{amb} = + 25 °C	V_{SP}	1.28	1.30	1.32	V
COMIN switch point temperature coefficient	note 1	ΔV_{SP}	–	±0.1	±0.5	mV/K
SELECT input voltage:						
LOW		V_{IL}	–	–	$0.3V_{DD}$	V
HIGH		V_{IH}	$0.7V_{DD}$	–	–	V
SELECT and COMIN leakage current:						
LOW		$-I_{IL}$	–	–	1.0	μA
HIGH		I_{IL}	–	–	1.0	μA
$\overline{\text{POWF}}$, RESET and COMOUT						
Output sink current	see Fig.6; V_O = 0.4 V; V_{DD} = 2.4 V	I_O	1	3	–	mA
Output source current	see Fig.7; V_O = 2.0 V; V_{DD} = 2.4 V	$-I_O$	0.75	2	–	mA
Reset time	note 2; C_{CT} = 1 nF	t_R	400	1000	2000	μs
Save time	note 2; C_{CT} = 1 nF	t_S	40	100	200	μs
Reset to save time ratio		t_R/t_S	–	10	–	

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
CT internal capacitance		C_{INT}	–	100	–	pF

Notes to the characteristics

1. Value given per degree Kelvin. Tested on a sample basis.
2. Conformance to these specifications is only guaranteed when the slew rate of V_{DD} is less than 25 V/ms.

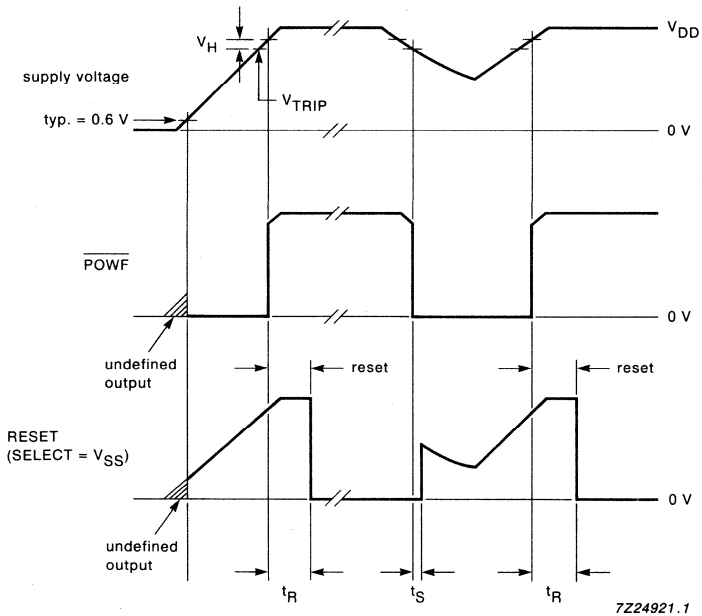


Fig.3 Timing diagram.

DEVELOPMENT DATA

Typical performance characteristics

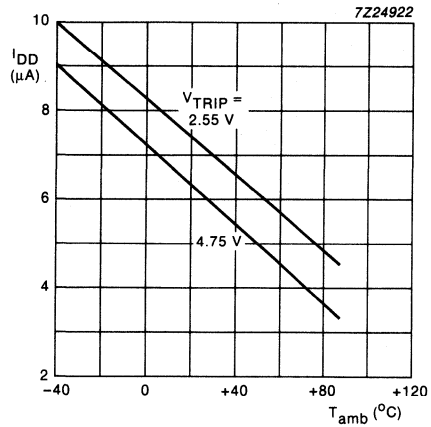


Fig.4 Supply current as a function of temperature; V_{DD} = 5 V; COMIN = V_{DD}.

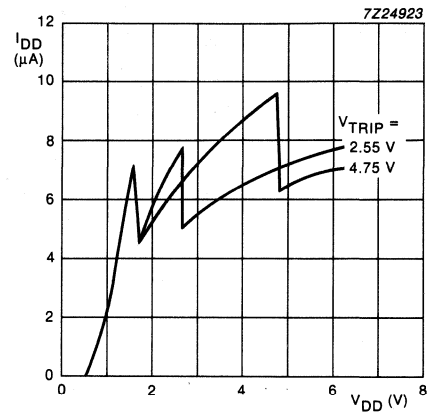


Fig.5 Supply current as a function of the supply voltage; T_{amb} = + 25 °C.

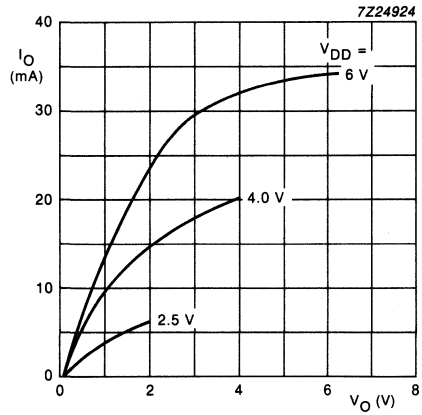


Fig.6 Output sink current as a function of the output voltage.

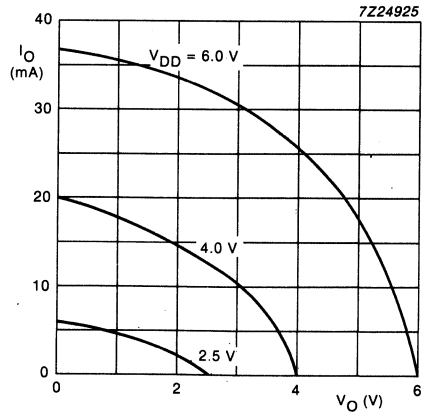


Fig.7 Output source current as a function of the output voltage.

DEVELOPMENT DATA

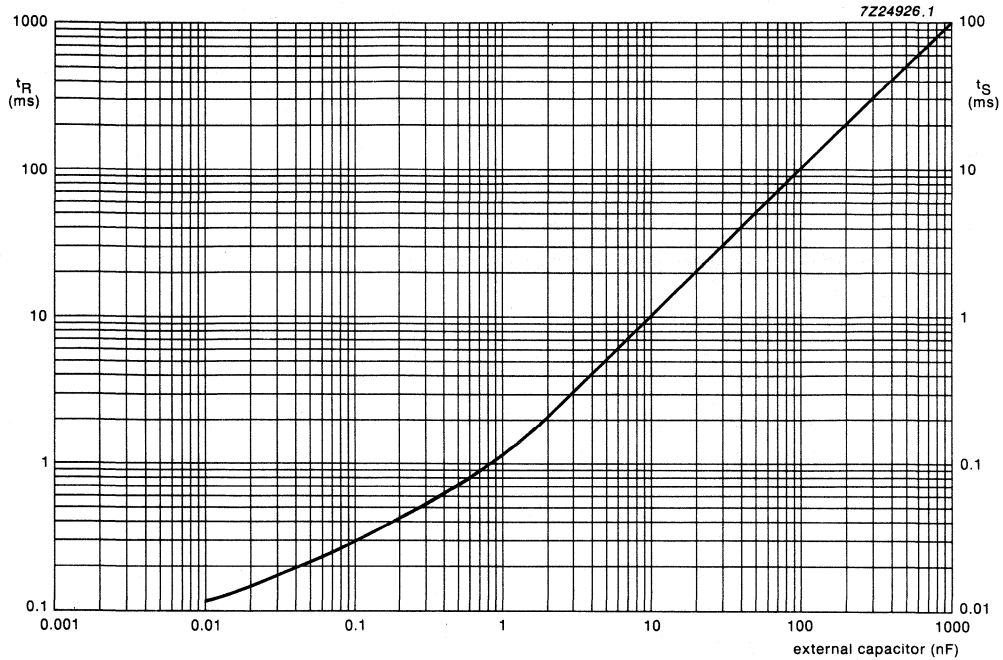


Fig.8 Reset and save times as a function of the external capacitor (C_{CT}).

Notes to Fig.8

1. t_R (typ.) = (0.1 + C_{CT}) ms.
2. t_S (typ.) = (0.01 + 0.1C_{CT}) ms.

APPLICATION INFORMATION

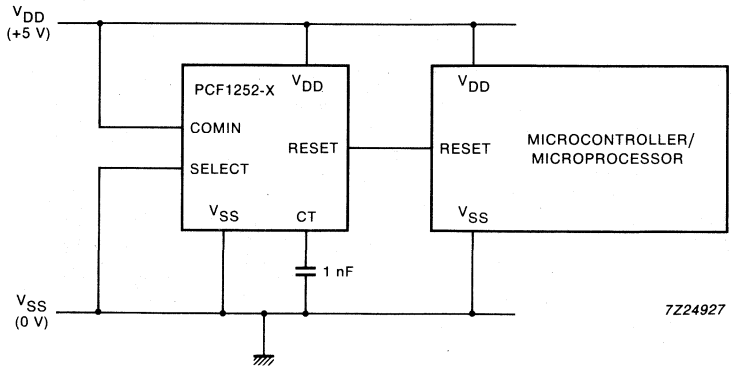


Fig.9 Typical power-ON reset circuit for a microcontroller/microprocessor system; (when not used, COMIN must be connected to V_{DD}).

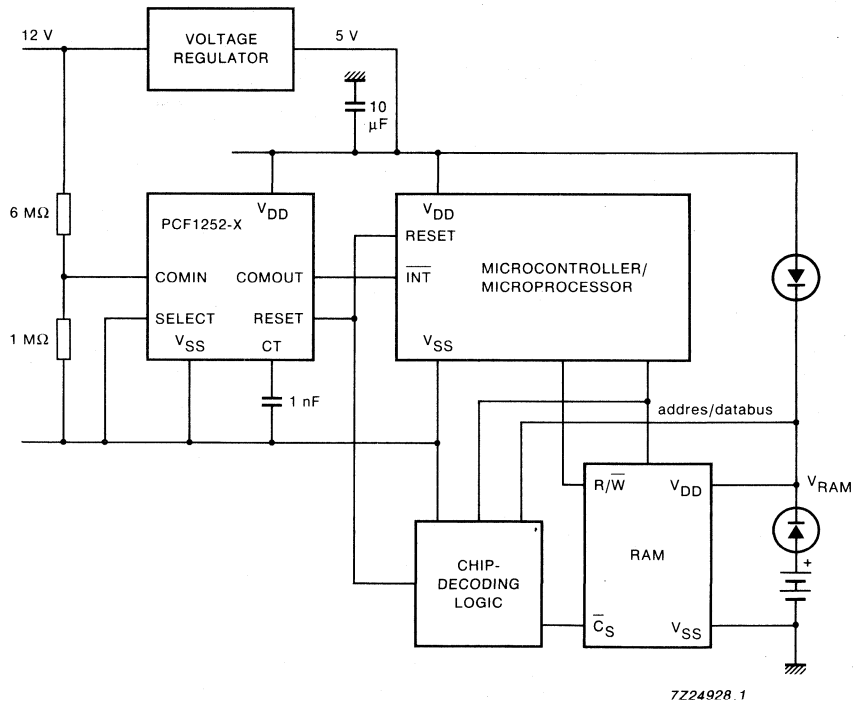


Fig.10 Data retention circuit for memory back-up systems.

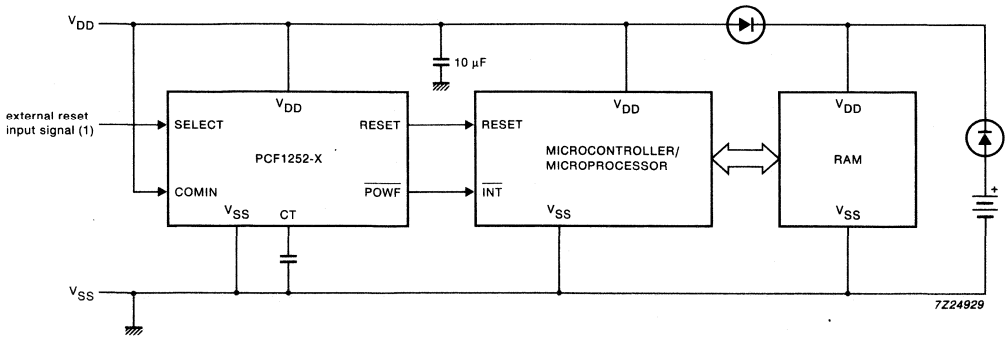


Fig.11 Data retention circuit with external switchable reset for systems with a single voltage supply.

Note to Fig.11

1. For external reset application, the SELECT input must be debounced.

DEVELOPMENT DATA

LCD DRIVER

GENERAL DESCRIPTION

The members of the PCF21XX family are single chip, silicon gate CMOS circuits. A three-line bus (CBUS) structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possibility
- Power-on reset clear

	PCF2100	PCF2110	PCF2111	PCF2112
• LCD segments	40	60	64	32
• LED segments	–	2	–	–
• Multiplex rate	1:2	1:2	1:2	1:1
• Word length	22 bit	34 bit	34 bit	34 bit

PACKAGE OUTLINES

PCF2100P: 28-lead DIL; plastic (SOT117).

PCF2110P:
PCF2111P: 40-lead DIL; plastic (SOT129).
PCF2112P:

PCF2100T: 28-lead mini-pack; plastic (SO28; SOT136A).

PCF2110T:
PCF2111T: 40-lead mini-pack; plastic (VSO40; SOT158A).
PCF2112T:

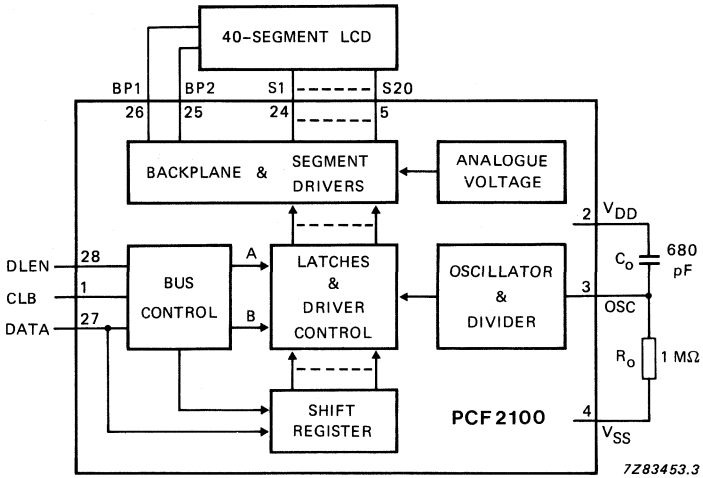


Fig. 1 Block diagram; PCF2100

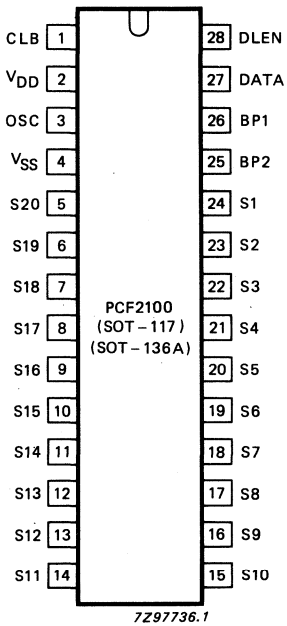


Fig. 2 Pinning diagram; PCF2100

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)
3	OSC	oscillator input
27	DATA	data line (CBUS)
28	DLEN	data line enable (CBUS)

Outputs

5 to 24	S20 to S1	LCD driver outputs
25	BP2	backplane drivers (commons of LCD)
26	BP1	backplane drivers (commons of LCD)

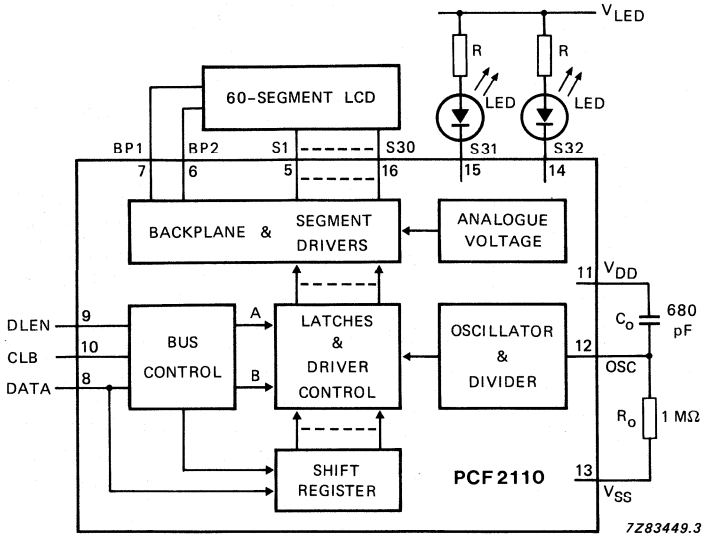


Fig. 3 Block diagram; PCF2110 (SOT-129).

DEVELOPMENT DATA

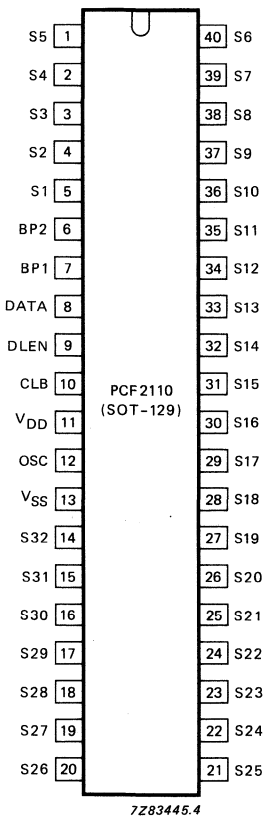


Fig. 4 Pinning diagram; PCF2110

PINNING (SOT-129)

Supply

11	V_{DD}	positive supply
13	V_{SS}	negative supply

Inputs

8	DATA	data line	CBUS
9	DLEN	data line enable	CBUS
10	CLB	clock burst	CBUS
12	OSC	oscillator input	

Outputs

1 to 5	S5 to S1	LCD driver outputs
6	BP2	backplane drivers (commons of LCD)
7	BP1	backplane drivers (commons of LCD)
14	S32	LED driver outputs
15	S31	LED driver outputs
16 to 40	S30 to S6	LCD driver outputs

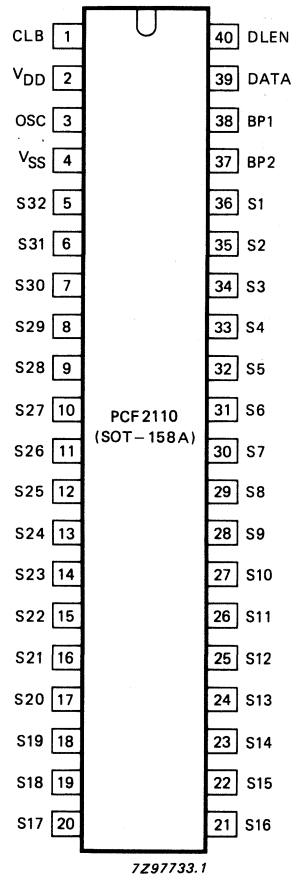


Fig. 5 Pinning diagram; PCF2110

PINNING (SOT-158A)

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)
3	OSC	oscillator input
39	DATA	data line } CBUS
40	DLEN	data line enable } CBUS

Outputs

5	S32	} LED driver outputs
6	S31	} LED driver outputs
7 to 36	S30 to S1	LCD driver outputs
37	BP2	} backplane drivers (commons of LCD)
38	BP1	} backplane drivers (commons of LCD)

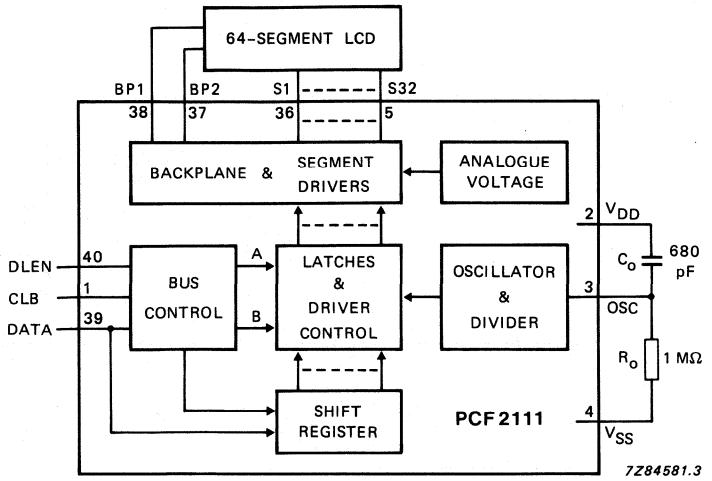


Fig. 6 Block diagram; PCF2111

DEVELOPMENT DATA

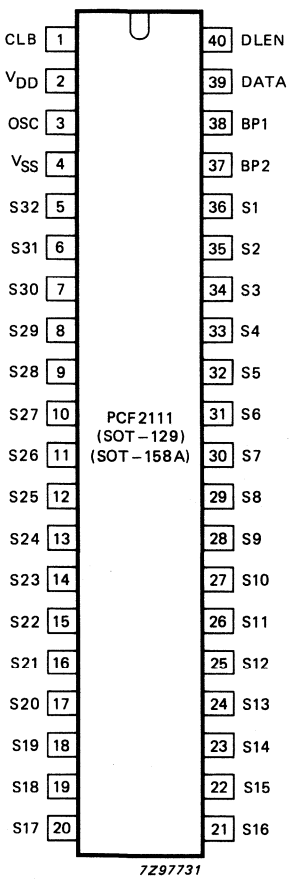


Fig. 7 Pinning diagram; PCF2111

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
39	DATA	data line	CBUS
40	DLEN	data line enable	CBUS

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP1	backplane drivers (commons of LCD)
37	BP2	backplane drivers (commons of LCD)

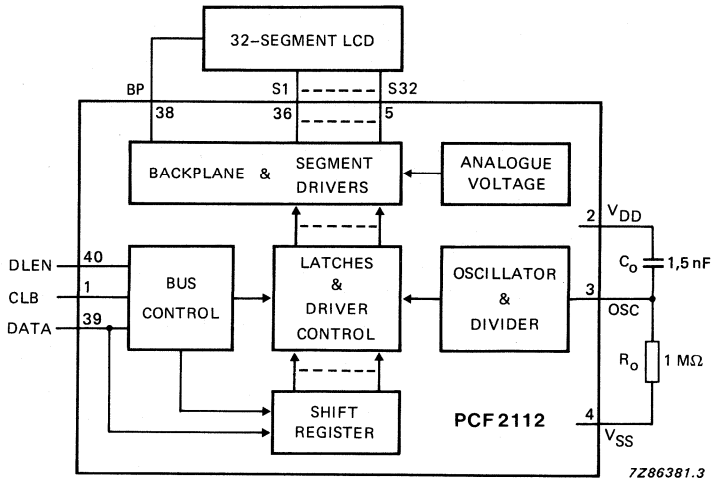


Fig. 8 Block diagram; PCF2112

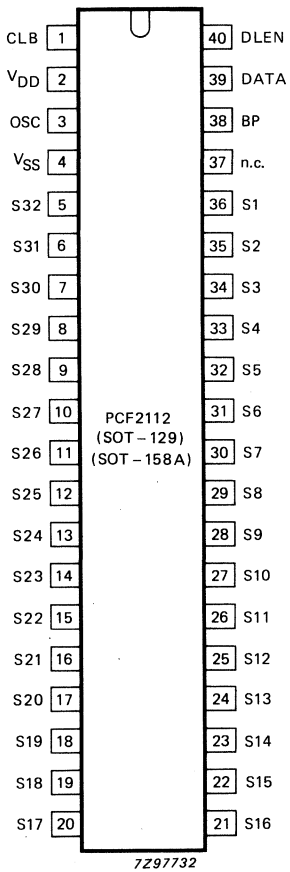


Fig. 9 Pinning diagram; PCF2112

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
39	DATA	data line	CBUS
40	DLEN	data line enable	CBUS

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP	backplane driver (common of LCD)
37	n.c.	not connected

FUNCTIONAL DESCRIPTION

An LCD segment or LED output is activated when the corresponding DATA-bit is HIGH.

PCF2100

When DATA-bit 21 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 21 LOW, the B-latches (BP2) are loaded. CLB-pulse 23 transfers data from the shift register to the selected latches.

PCF2110

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. Bits 31 and 32 contain the LED output information. With DATA-bit 33 LOW, the B-latches (BP2) are loaded and bits 31 and 32 are ignored. CLB-pulse 35 transfers data from the shift register to the selected latches.

PCF2111

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 33 LOW, the B-latches (BP2) are loaded. CLB-pulse 35 transfers data from the shift register to the selected latches.

PCF2112

When DATA-bit 33 is HIGH, the latches are loaded. CLB-pulse 35 transfers data from the shift register to the selected latches.

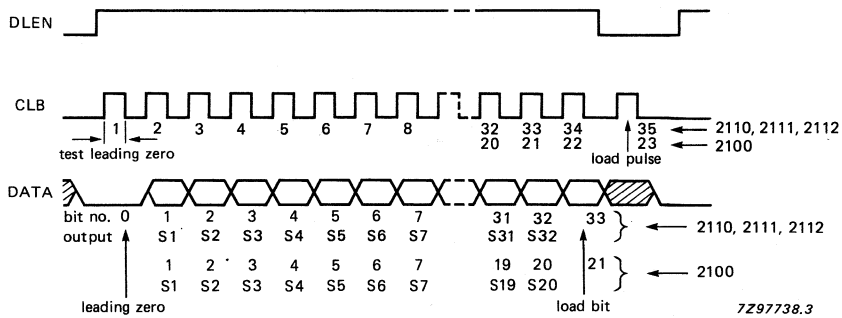


Fig. 10 CBUS data format.

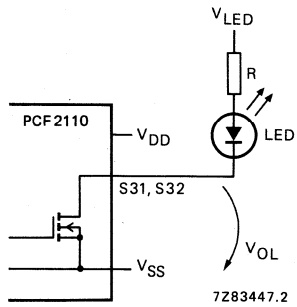


Fig. 11 LED driver circuitry.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN LOW) and the driver is ready to receive new data.

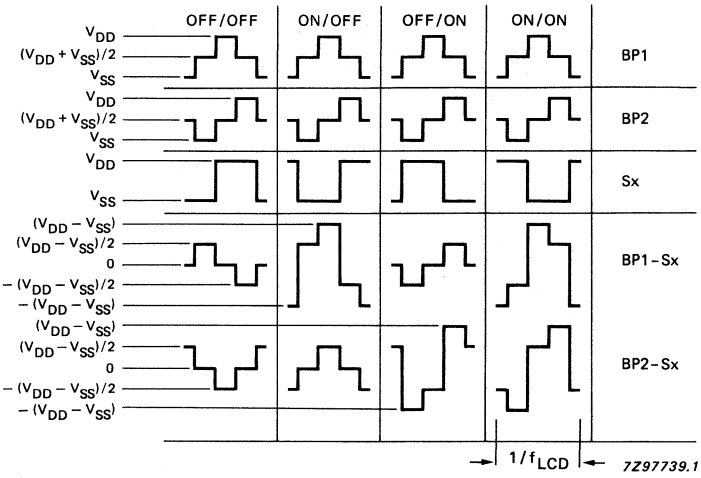


Fig. 12 Timing diagram (except PCF2112).

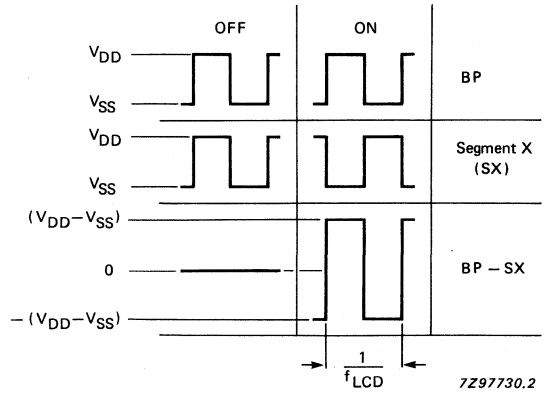


Fig. 13 Timing diagram for PCF2112.

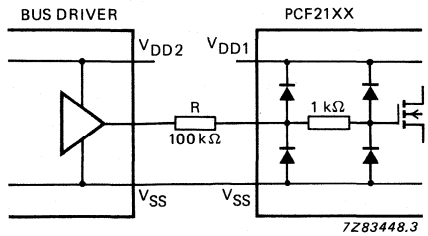


Fig. 14 Input circuitry.

Note to Fig. 14

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection. Maximum input current $\leqslant 40\,\mu$A.

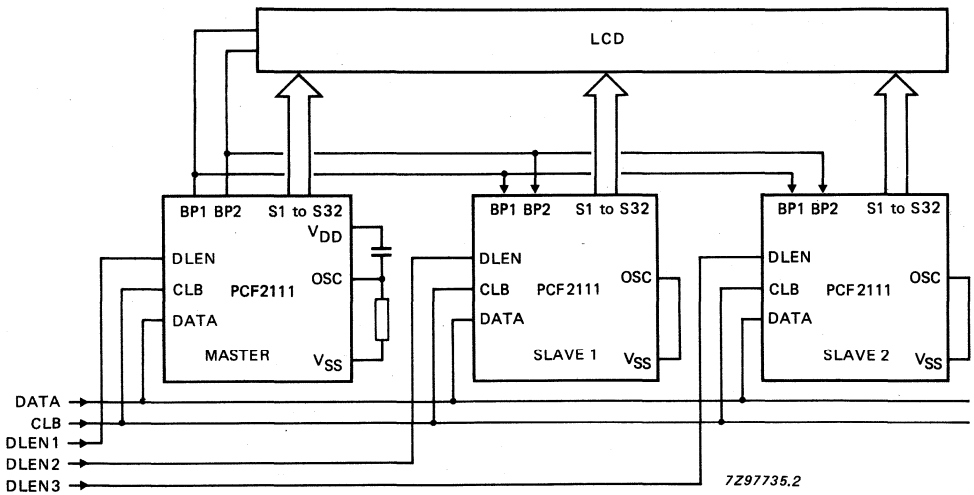


Fig. 15 Diagram showing expansion possibility (using PCF2111).

Note to Fig. 15

By connecting OSC to V_{SS} the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several members of the PCF21XX family up to the BP drive capability of the master. The PCF2112 can only function as a master for other PCF2112s.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0,5	9,0	V
Input voltage range DLEN, CLB, DATA and OSC		V_I	V_{SS}−0,5	V_{DD}+0,5	V
Output voltage range BP1, BP2 and S1 to S32		V_O	V_{SS}−0,5	V_{DD}+0,5	V
Supply current		$\pm I_{DD}, \pm I_{SS}$	−	50	mA
DC input current		$\pm I_I$	−	20	mA
DC output current		$\pm I_O$	−	25	mA
Total power dissipation per package	note 1	P_{tot}	−	500	mW
Power dissipation per output		P_O	−	100	mW
Storage temperature range		T_{stg}	−65	+150	°C

Note to the ratings

1. Derate by 7,7 mW/°C when $T_{amb} > 60$ °C.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2,25 to 6,5 V; T_{amb} = −40 to + 85 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	2,25	–	6,5	V
Supply current	note 1	I_{DD1}	–	20	50	μA
Supply current	note 1; T_{amb} = 25 °C	I_{DD2}	–	20	30	μA
Power-on reset level	note 2	V_{POR}	–	1,0	1,6	V
Inputs CLB, DATA DLEN						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,0	–	–	V
Leakage current	$V_I = V_{SS}$ or V_{DD}	$\pm I_I$	–	–	1	μA
Input capacitance	note 3	C_I	–	–	10	pF
Input OSC						
Oscillator start-up current	$V_I = V_{SS}$	I_{OSC}	0,5	1,2	5,0	μA
LCD outputs						
DC component of backplane drivers		$\pm V_{BP}$	–	20	–	mV
Backplane driver output impedance	note 4; V_{DD} = 5 V	R_{BP}	–	0,5	5	kΩ
Segment driver output impedance	note 4; V_{DD} = 5 V	R_S	–	1	7	kΩ
LED outputs (S31 and S32 in PCF2110)						
Output current LOW	V_{OL}=0,4 V; V_{DD}=5 V	I_{OL}	8	14	–	mA
Output leakage current	$V_O = V_{DD}$	$\pm I_O$	–	–	1	μA
Load current		I_{LED}	–	–	20	mA

AC CHARACTERISTICS (note 5)

V_{SS} = 0 V; V_{DD} = 2,25 to 6,5 V; T_{amb} = −40 to + 85 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs CLB, DATA DLEN						
Data set-up time		t_{SUDA}	3	–	–	μs
Data hold time		t_{HDDA}	3	–	–	μs
Enable set-up time		t_{SUEN}	1	–	–	μs
Disable set-up time		t_{SUDI}	2	–	–	μs
Load pulse set-up time		t_{SULD}	2,5	–	–	μs
Busy time		t_{BUSY}	3	–	–	μs
CLB HIGH time		t_{WH}	1	–	–	μs
CLB LOW time		t_{WL}	5	–	–	μs
CLB period		t_{CLB}	10	–	–	μs
Rise and fall times		t_r, t_f	–	–	10	μs
LCD timing						
LCD frame frequency		f_{LCD}	60	75	100	Hz
LCD frame frequency for PCF2112	C_O = 1,5 nF	f_{LCD}	30	35	50	Hz
Transfer time with test loads	V_{DD} = 5 V	t_{BS}	–	20	100	μs
Driver delay with test loads	V_{DD} = 5 V	t_{PLCD}	–	20	100	μs

Notes to the characteristics

1. Outputs open; CBUS inactive.
2. Resets all logic, when $V_{DD} < V_{POR}$.
3. Periodically sampled (not 100% tested).
4. Outputs measured one at a time.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

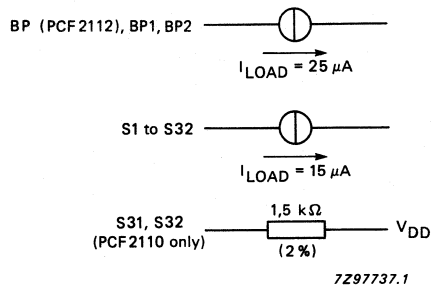
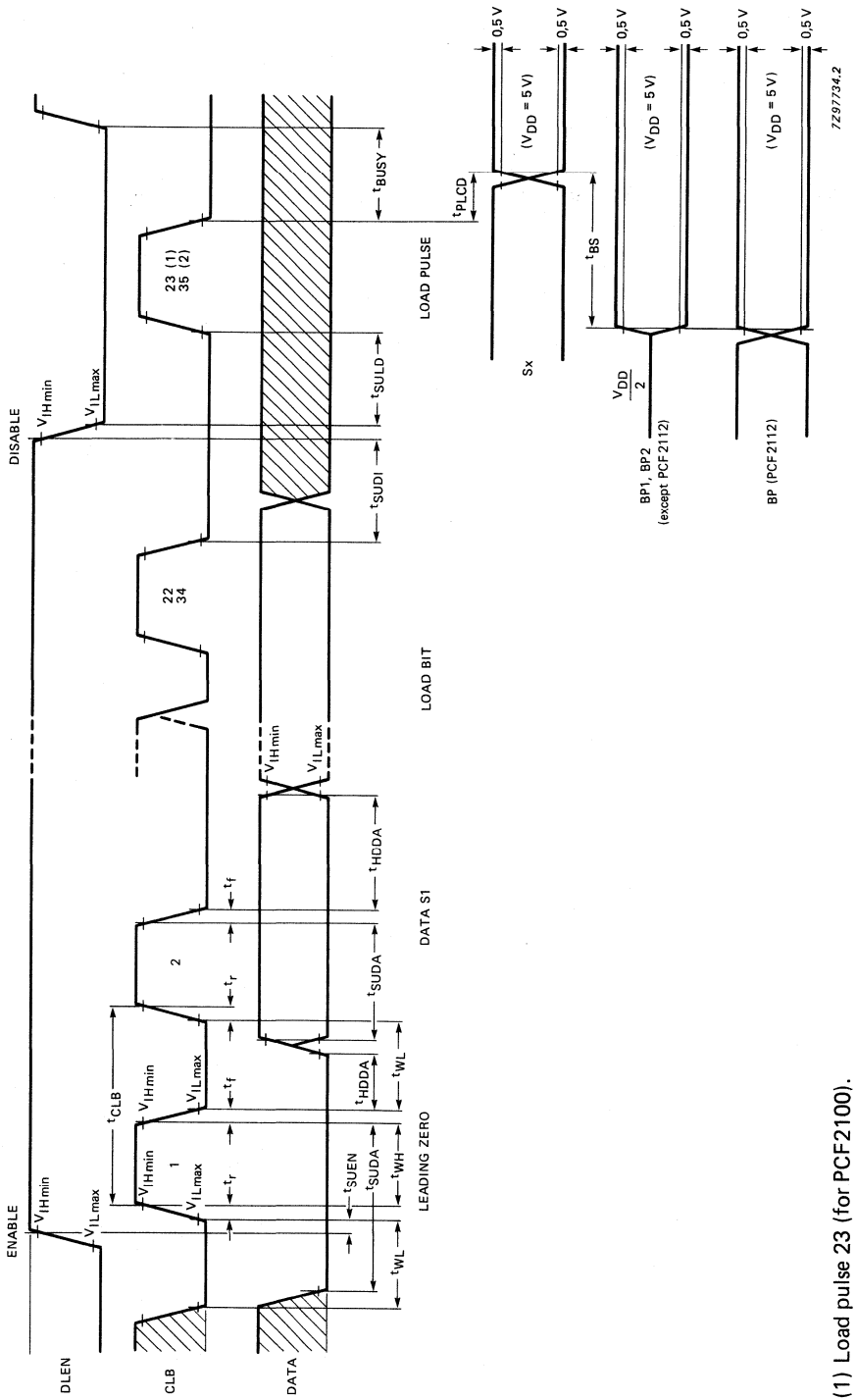


Fig. 16 Test loads.



(1) Load pulse 23 (for PCF2100).
(2) Load pulse 35 (for PCF2110, PCD2111 and PCF2112; see Fig. 10).

Fig. 17 CBUS timing.

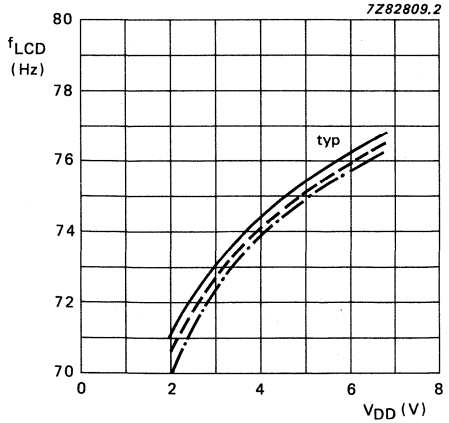


Fig. 18 Displays frequency as a function of supply voltage; C_O = 680 pF (except PCF2112).
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

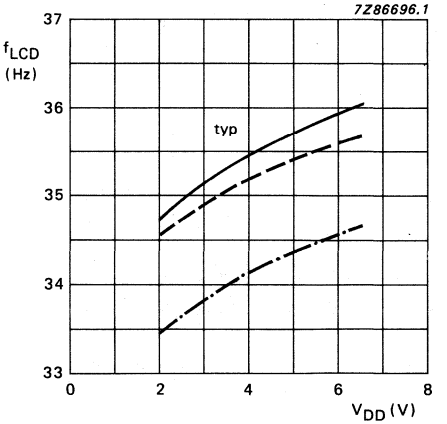


Fig. 19 Display frequency as a function of supply voltage; C_O = 1,5 nF (only PCF2112).
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

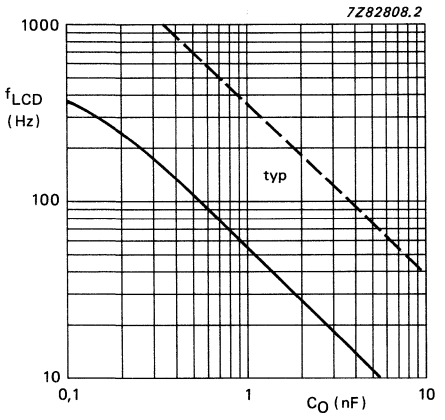


Fig. 20 Display frequency as a function of R_O and C_O; T_{amb} = + 25 °C; V_{DD} = 5 V.
——— R_O = 1 MΩ;
– – – – R_O = 100 kΩ.

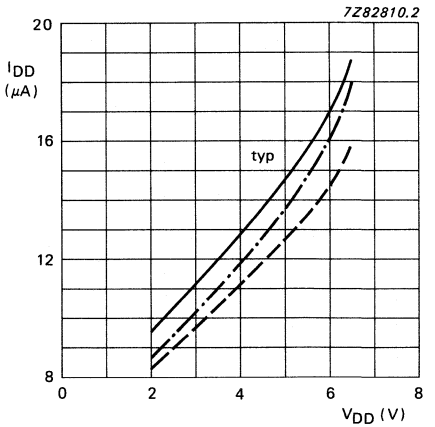


Fig. 21 Supply current as a function of supply voltage.
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

DEVELOPMENT DATA

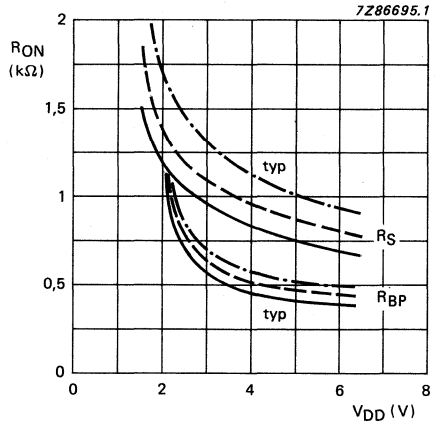


Fig. 22 Output resistance of backplane and segments.
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

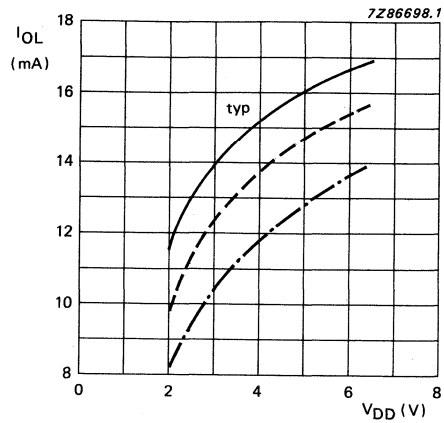


Fig. 23 Output current as a function of supply voltage (only PCF2112).
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

LCD FLAT-PANEL ROW/COLUMN DRIVER

GENERAL DESCRIPTION

The PCF2201 is a row or column LCD driver, designed to drive LCD flat-panels at multiplex rates of up to 1 : 256. The PCF2201 converts serial or parallel 4-bit display data into parallel LCD drive waveforms, capable of driving up to 81 rows or 80 columns of an LCD matrix. The PCF2201 is cascadable, enabling it to drive any LCD flat-panel matrix. The PCF2201 is controlled by an alphanumeric/graphic controller.

Features

- Row or column drive capability
- 80 data latches
- 81 stage bidirectional shift register
- 81 LCD drive outputs
- Proprietary margin control drive output
- Low drive impedance
- LCD drive voltage of up to 25 V
- 5 V logic compatibility
- High speed operation (4 MHz)
- Multiplex rates of up to 1 : 256
- Externally adjusted bias voltages
- Maximum LCD voltage and V_{DD} may be separated
- 64/65 pin programmable output operation mode
- Low power consumption
- Overall flat-panel power consumption minimized
- Pin programmable right/left orientation for convenience of flat-panel construction
- Optimized pinning for single plane wiring
- Space-saving 120-lead Tape-Automated Bonding package
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINE

PCF2201V: 120-lead Tape-Automated Bonding (TAB) module (SOT235)

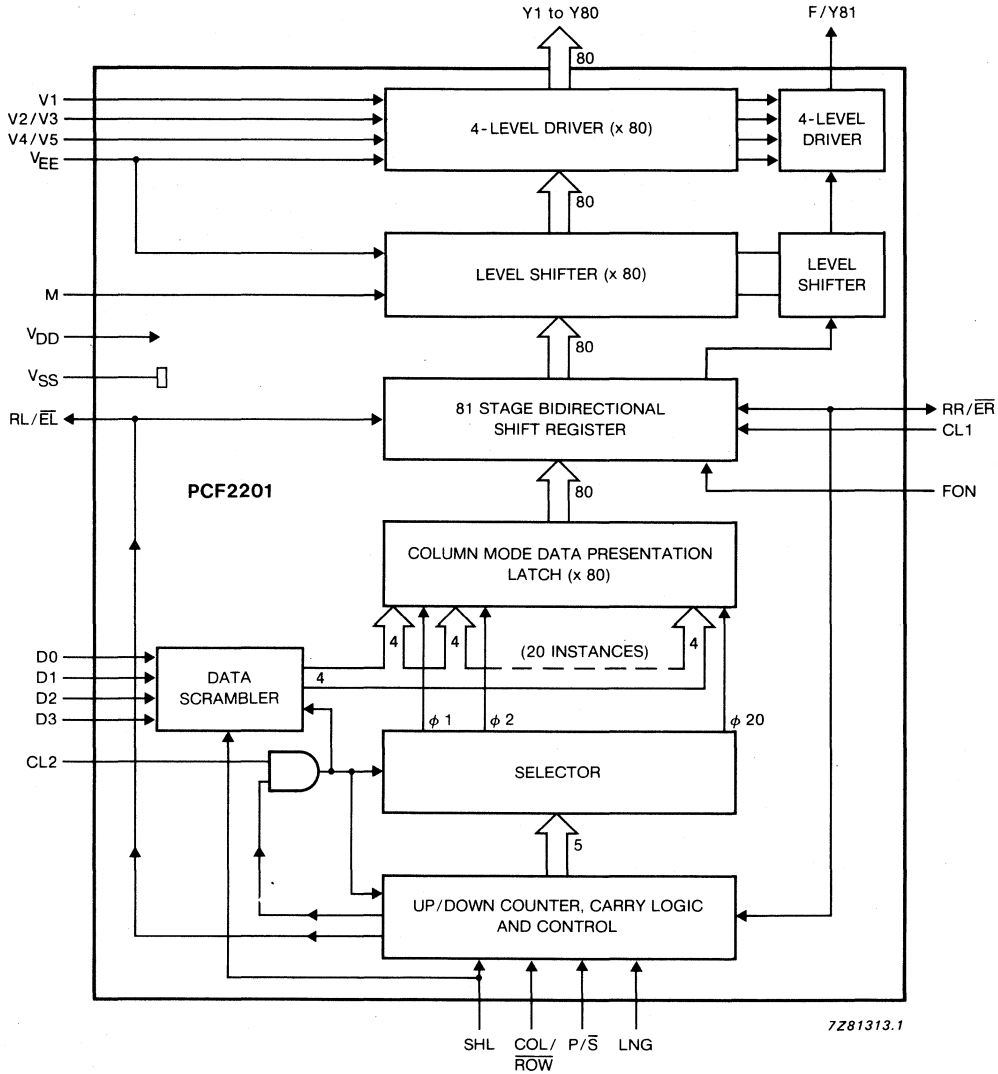


Fig. 1 Block diagram.

DEVELOPMENT DATA

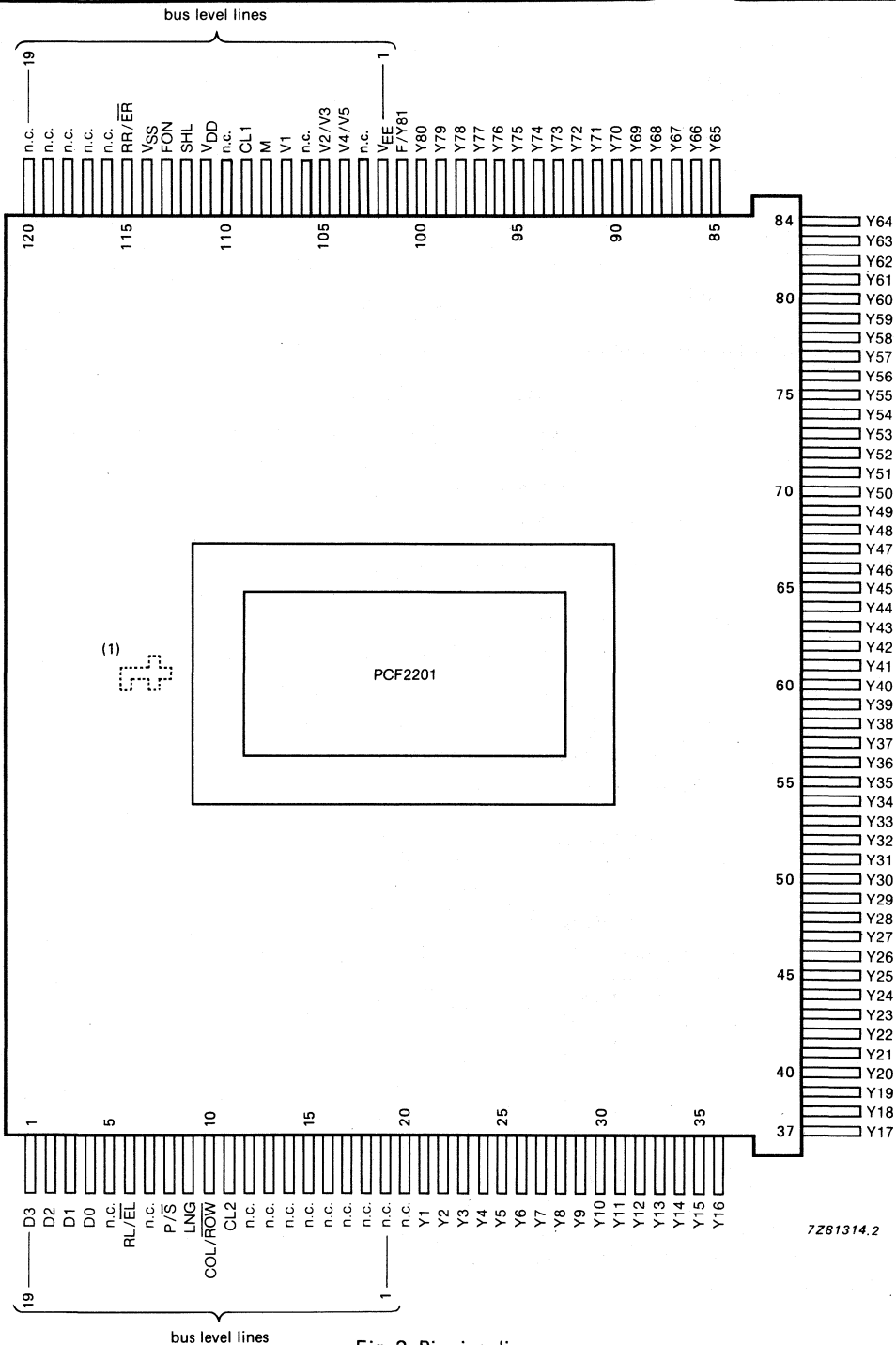


Fig. 2 Pinning diagram.

(1) mark orientation

PINNING FUNCTIONS

mnemonic	I/O	function
V_{DD}	P	Positive supply voltage (5 V)
V_{SS}	P	Logic ground (0 V)
V_1	P	Most positive LCD supply voltage ($\leqslant V_{DD}$), selection level
V_2/V_3	P	Upper non-selection level for row (V2) or column (V3) driver
V_4/V_5	P	Lower non-selection level for row (V5) or column (V4) driver
V_{EE}	P	Most negative LCD supply voltage (−20 V), selection level
Y1 to Y80	O	Liquid crystal driver outputs
CL1	I	Clock for 81 stage bidirectional shift register Loads parallel data from the data presentation latch and frame control in column driver mode Shifts data in row driver mode Negative edge triggered
CL2	I	Data transfer clock in column driver modes Data must be valid on the negative edge of CL2 Unused in row driver mode (may be left open)
COL/$\overline{\text{ROW}}$	I	Column/row driver mode select
P/$\overline{\text{S}}$	I	Parallel/serial mode select for column drivers Tie to V_{SS} in row driver mode
SHL	I	Shift direction select
D0 to D3	I	Data inputs in column driver modes Unused in row driver mode (may be left open) Filling order:

COL/$\overline{\text{ROW}}$	P/$\overline{\text{S}}$	SHL	D0	D1	D2	D3
H	L	L	Y1, Y2, Y3,.	unused	unused	unused
H	L	H	Y80, Y79,...	(may be left open)	(may be left open)	(may be left open)
H	H	L	Y1, Y5, Y9,.	Y2, Y6, Y10,.	Y3, Y7, Y11,.	Y4, Y8, Y12,..
H	H	H	Y80, Y76,...	Y79, Y75,....	Y78, Y74,....	Y77, Y73,.....

Also in the **serial** column driver mode, a multiple of 4 data bits must always be transferred. Add dummy bits if necessary

DEVELOPMENT DATA

<table>
<tr><th>mnemonic</th><th>I/O</th><th>function</th></tr>
<tr><td>RL/$\overline{EL}$
RR/$\overline{ER}$</td><td>I/O</td><td>Left/right serial input/outputs in row driver mode, left/right enable input/outputs in column driver modes
<table>
<tr><th>COL/$\overline{ROW}$</th><th>P/$\overline{S}$</th><th>SHL</th><th>RL/$\overline{EL}$</th><th>RR/$\overline{ER}$</th><th>comments</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>I</td><td>O</td><td>shift direction:
RL/$\overline{EL}$ –> RR/$\overline{ER}$ (Y1 –> F/Y81)</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>O</td><td>I</td><td>shift direction:
RR/$\overline{ER}$ –> RL/$\overline{EL}$ (F/Y81 –> Y1)</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>I</td><td>O</td><td>RR/$\overline{ER}$ goes LOW 80 CL2 pulses after RL/$\overline{EL}$</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>O</td><td>I</td><td>RL/$\overline{EL}$ goes LOW 80 CL2 pulses after RR/$\overline{ER}$</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>I</td><td>O</td><td>RR/$\overline{ER}$ goes LOW 20 CL2 pulses after RL/$\overline{EL}$</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>O</td><td>I</td><td>RL/$\overline{EL}$ goes LOW 20 CL2 pulses after RR/$\overline{ER}$</td></tr>
</table>
In the serial column mode, the device accepts one bit of display data at each CL2 pulse after RL/$\overline{EL}$ (or RR/$\overline{ER}$ respectively) goes LOW
When 80 bits of display data have been accepted, the device accepts no further display data and takes its output RR/$\overline{ER}$ (or RL/$\overline{EL}$ respectively) LOW, thereby enabling the next PCF2201 to accept display data
The sequence is reset when CL1 is HIGH and CL2 is LOW

In the parallel column mode, the device accepts one nibble of display data at each CL2 pulse after RL/$\overline{EL}$ (or RR/$\overline{ER}$ respectively) goes LOW
When 20 nibbles of display data have been accepted, the device accepts no further display data and takes its output RR/$\overline{ER}$ (or RL/$\overline{EL}$ respectively) LOW, thereby enabling the next PCF2201 to accept display data.
The sequence is reset when CL1 is HIGH and CL2 is LOW</td></tr>
<tr><td>LNG</td><td>I</td><td>Length control
<table>
<tr><th>COL/$\overline{ROW}$</th><th>LNG</th><th>SHL</th><th>description</th><th>valid Yi</th><th>undefined Yi</th></tr>
<tr><td>L
L</td><td>L
L</td><td>L
H</td><td>65-bit row mode
operation</td><td>Y1...Y65
Y17...Y80, F/Y81</td><td>Y66...Y80, F/Y81
Y1...Y16</td></tr>
<tr><td>L
L</td><td>H
H</td><td>L
H</td><td>81-bit row mode
operation</td><td>Y1...Y80, F/Y81
Y1...Y80, F/Y81</td><td>–
–</td></tr>
<tr><td>H
H</td><td>L
L</td><td>L
H</td><td>64-bit column
mode operation</td><td>Y1...Y64
Y17...Y80</td><td>Y65...Y80
Y1...Y16</td></tr>
<tr><td>H
H</td><td>H
H</td><td>L
H</td><td>80-bit column
mode operation</td><td>Y1...Y80
Y1...Y80</td><td>–
–</td></tr>
</table>
In 80/81-bit operation, the device behaves as previously described
In 64/65-bit operation, the device behaves as if all resources have been reduced to 64/65 instances; i.e. 16 outputs (determined by SHL) can no longer be accessed and should be left open circuit.</td></tr>
</table>

PINNING FUNCTIONS (continued)

<table>
<tr><th>mnemonic</th><th>I/O</th><th>function</th></tr>
<tr><td>F/Y81*</td><td>O</td><td>Frame output in column driver mode
It continuously delivers the select or non-select column driver LCD voltages depending on the state of the frame control
The frame output is used to blank the flat-panel display margin outside the actual LCD matrix
Liquid crystal driver output, number 81 in row driver mode</td></tr>
<tr><td>FON</td><td>I</td><td>Frame control
Defines the contents of the shift register cell corresponding to F/Y81 in column driver mode
Tie to V_{DD} or V_{SS} in row driver mode</td></tr>
<tr><td>M</td><td>I</td><td>Signal to convert LCD drive waveform into a.c.:
<table>
<tr><th>COL/$\overline{\text{ROW}}$</th><th>SR data</th><th>M</th><th>output level (Y_i or F/Y81)</th><th>note</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>V_2/V_3</td><td rowspan="4">row driver</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>V_4/V_5</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>V_{EE}</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>V_1</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>V_2/V_3</td><td rowspan="4">column driver</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>V_4/V_5</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>V_1</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>V_{EE}</td></tr>
</table></td></tr>
<tr><td>n.c.</td><td>—</td><td>not connected</td></tr>
</table>

* Patent application pending.

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 4,5 to 5,5 V;

V_{EE} = 0 to −20 V; $V_{DD} \geqslant V_1 \geqslant V_2/V_3 \geqslant \frac{V_{DD} + V_{EE}}{2} - 1\ V \geqslant V_4/V_5 \geqslant V_{EE}$; f_M = 100 Hz

T_{amb} = −40 to + 85 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Positive supply voltage		V_{DD}	4,5	–	5,5	V
Negative LCD supply voltage		V_{EE}	$V_{DD}-25$	–	$V_{DD}-5$	V
Static supply current	$f_{CL1} = f_{CL2}$ = 0 Hz; COL/$\overline{\text{ROW}}$ = H; M = L; note 2	I_{DD1}	–	15	40	μA
Operating supply current	COL/$\overline{\text{ROW}}$ = H; f_{CL1} = 25 kHz; f_{CL2} = 4 MHz; note 2	I_{DD2}	–	0,4	1	mA
Operating supply current	COL/$\overline{\text{ROW}}$ = H; RL/$\overline{\text{EL}}$ = H (SHL = L) or RR/$\overline{\text{ER}}$ = H (SHL = H); f_{CL1} = 25 kHz; note 2	I_{DD3}	–	50	150	μA
Operating supply current	COL/$\overline{\text{ROW}}$ = L; f_{CL1} = 100 kHz; note 2	I_{DD4}	–	75	200	μA
Logic						
Input voltage LOW HIGH		V_{IL} V_{IH}	0 0,7 V_{DD}	– –	0,3 V_{DD} V_{DD}	V
Output voltage LOW to RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$	I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH to RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$	I_O = 0 mA	V_{OH}	$V_{DD}-0,05$	–	–	V
Output current LOW to RL/$\overline{\text{EL}}$ and RR/$\overline{\text{ER}}$	V_{OL} = 1 V	I_{OL}	1	–	–	mA

DC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output current HIGH RL/$\overline{EL}$ and RR/$\overline{ER}$	$V_{OH} = V_{DD} - 1$ V	I_{OH}	–	–	1	mA
Leakage current at CL1, CL2, COL/$\overline{ROW}$, P/$\overline{S}$, SHL, D0 to D3, RL/$\overline{EL}$, RR/$\overline{ER}$, LNG, FON and M		$\pm I_{L1}$	–	–	1	μA
Input capacitance	note 3	C_I	–	–	7	pF
LCD outputs						
Leakage current at V_1, V_2/V_3, V_4/V_5		$\pm I_{L2}$	–	–	2	μA
Resistance ON between V_1, V_2/V_3, V_4/V_5, V_{EE} and Y1 to Y80, F/Y81	$I_O = 100$ μA; $V_{EE} = V_{DD} - 25$ V note 4	R_{ON}	–	–	2	kΩ

AC CHARACTERISTICS (note 5)

$V_{SS} = 0$ V; $V_{DD} = 4{,}5$ to $5{,}5$ V;
$V_{EE} = 0$ to -20 V; $V_{DD} \geqslant V_1 \geqslant V_2/V_3 \geqslant \frac{V_{DD} + V_{EE}}{2} - 1\text{ V} \geqslant V_4/V_5 \geqslant V_{EE}$;
$f_M = 100$ Hz; see Figs 4 and 5; $T_{amb} = -40$ to $+85$ °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Column driver data transfer rate		f_{CL2}	–	–	4	MHz
CL2 HIGH time		t_{CL2H}	100	–	–	ns
CL2 LOW time		t_{CL2L}	100	–	–	ns
CL2 rise time		t_{CL2r}	–	–	25	ns
CL2 fall time		t_{CL2f}	–	–	25	ns
Row driver clock rate		f_{CL1}	–	–	100	kHz
CL1 HIGH time		t_{CL1H}	275	–	–	ns
CL1 LOW time		t_{CL1L}	5	–	–	μs
CL1 rise time		t_{CL1r}	–	–	50	ns
CL1 fall time		t_{CL1f}	–	–	50	ns

DEVELOPMENT DATA

AC CHARACTERISTICS (continued)

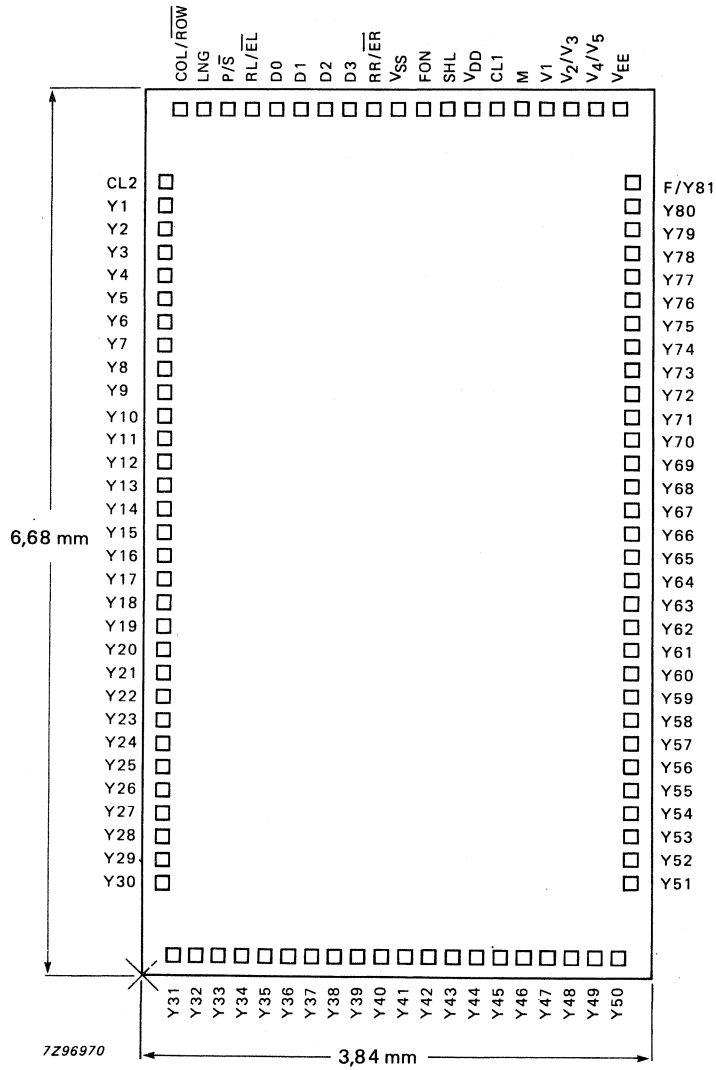
parameter	conditions	symbol	min.	typ.	max.	unit
Column data set-up time	COL/$\overline{\text{ROW}}$ = H	t_{SUC}	50	–	–	ns
Column data hold time	COL/$\overline{\text{ROW}}$ = H	t_{HDC}	30	–	–	ns
Row data set-up time	COL/$\overline{\text{ROW}}$ = L	t_{SUR}	200	–	–	ns
Row data hold time	COL/$\overline{\text{ROW}}$ = L	t_{HDR}	0	–	–	ns
Enable HIGH to CL2 set-up time	COL/$\overline{\text{ROW}}$ = H	t_{ECH}	90	–	–	ns
Enable LOW to CL2 set-up time	COL/$\overline{\text{ROW}}$ = H	t_{ECL}	85	–	–	ns
Propagation delay to enable HIGH	COL/$\overline{\text{ROW}}$ = H	t_{PEH}	–	–	185	ns
Propagation delay to enable LOW	COL/$\overline{\text{ROW}}$ = H	t_{PEL}	–	–	140	ns
CL2 to CL1 time	COL/$\overline{\text{ROW}}$ = H	t_{CL21}	50	–	–	ns
CL1 to CL2 time	COL/$\overline{\text{ROW}}$ = H	t_{CL12}	50	–	–	ns
Overlap time of CL2 = LOW and CL1 = HIGH	COL/$\overline{\text{ROW}}$ = H	t_{ov}	275	–	–	ns
Propagation delay HIGH to RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$	COL/$\overline{\text{ROW}}$ = L	t_{PLH}	20	–	200	ns
Propagation delay LOW to RL/$\overline{\text{EL}}$, RR/$\overline{\text{ER}}$	COL/$\overline{\text{ROW}}$ = L	t_{PHL}	20	–	200	ns
Propagation delay to Y1 . . . Y80, F/Y81	$V_{EE} = V_{DD}$ −20 V	t_{PY}	–	–	3	μs

Notes to characteristics

1. Maintain $V_{DD} \geqslant V_1 \geqslant V_2/V_3 \geqslant \frac{V_{DD} + V_{EE}}{2} - 1\text{ V} \geqslant V_4/V_5 \geqslant V_{EE}$.
2. Outputs open, inputs at V_{SS} or V_{DD}.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

Fig. 3 Test loads.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 25,65 mm^2

Bonding pad dimensions: 104 μm x 104 μm

Fig. 11 Bonding pad locations.

DEVELOPMENT DATA

Table 2 Bonding pad centre locations (dimensions in μm)

All x/y co-ordinates are referenced to the bottom left corner, see Fig. 11.

pad	X	Y	pad	X	Y
D3	1556	6526	Y43	2364	154
D2	1372	6526	Y44	2540	154
D1	1188	6526	Y45	2716	154
D0	1004	6526	Y46	2892	154
RL/$\overline{EL}$	820	6526	Y47	3068	154
P/$\overline{S}$	636	6526	Y48	3244	154
LNG	452	6526	Y49	3420	154
COL/$\overline{ROW}$	268	6526	Y50	3596	154
CL2	156	5982	Y51	3684	702
Y1	156	5806	Y52	3684	878
Y2	156	5630	Y53	3684	1054
Y3	156	5454	Y54	3684	1230
Y4	156	5278	Y55	3684	1406
Y5	156	5102	Y56	3684	1582
Y6	156	4926	Y57	3684	1758
Y7	156	4750	Y58	3684	1934
Y8	156	4574	Y59	3684	2110
Y9	156	4398	Y60	3684	2286
Y10	156	4222	Y61	3684	2462
Y11	156	4046	Y62	3684	2638
Y12	156	3870	Y63	3684	2814
Y13	156	3694	Y64	3684	2990
Y14	156	3518	Y65	3684	3166
Y15	156	3342	Y66	3684	3342
Y16	156	3166	Y67	3684	3518
Y17	156	2990	Y68	3684	3694
Y18	156	2814	Y69	3684	3870
Y19	156	2638	Y70	3684	4046
Y20	156	2462	Y71	3684	4222
Y21	156	2286	Y72	3684	4398
Y22	156	2110	Y73	3684	4574
Y23	156	1934	Y74	3684	4750
Y24	156	1758	Y75	3684	4926
Y25	156	1582	Y76	3684	5102
Y26	156	1406	Y77	3684	5278
Y27	156	1230	Y78	3684	5454
Y28	156	1054	Y79	3684	5630
Y29	156	878	Y80	3684	5806
Y30	156	702	F/Y81	3684	5982
Y31	252	154	V_{EE}	3580	6526
Y32	428	154	V_4/V_5	3396	6526
Y33	604	154	V_2/V_3	3212	6526
Y34	780	154	V1	3028	6526
Y35	956	154	M	2844	6526
Y36	1132	154	CL1	2660	6526
Y37	1308	154	V_{DD}	2476	6526
Y38	1484	154	SHL	2292	6526
Y39	1660	154	FON	2108	6526
Y40	1836	154	V_{SS}	1924	6526
Y41	2012	154	RR/$\overline{ER}$	1740	6526
Y42	2188	154			

VOICE SYNTHESIZER

GENERAL DESCRIPTION

The PCF8200 is a CMOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately.
Applications include automotive, telephony, personal computers, annunciators, aids for the handicapped, and general industrial devices.

Features

- Male and female speech with good quality
- Speech-band from 0 to 5 kHz
- Bit-rate between 455 bits/second and 4545 bits/second
- Programmable frame duration
- Programmable speaking speed
- CMOS technology
- Operating temperature range −40 to + 85 °C
- Single 5 V supply with low power consumption and power-down stand-by mode
- Interfaces easily with most popular microcomputers and microprocessors through 8 bit parallel bus or I^2C bus
- Software readable status word (parallel bus or I^2C bus)
- BUSY-signal and $\overline{REQ}$-signal hardware readable
- Internal low-pass filter and 11-bit D/A converter

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	–	5	–	V
Supply current	I_{DD}	–	12	#	mA
Supply current (stand-by)	$I_{DD(SB)}$	–	1	–	μA
Inputs					
Input voltage	V_{IH}	2,0	–	V_{DD}	V
Input voltage	V_{IL}	0	–	0,8	V
Input capacitance	C_I	–	7	–	pF
Outputs (D5 to D7)					
Output voltage high	V_{OH}	3,5	–	V_{DD}	V
Output voltage low	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

Value not yet available.

PACKAGE OUTLINE

24-lead DIL; plastic (SOT101A).

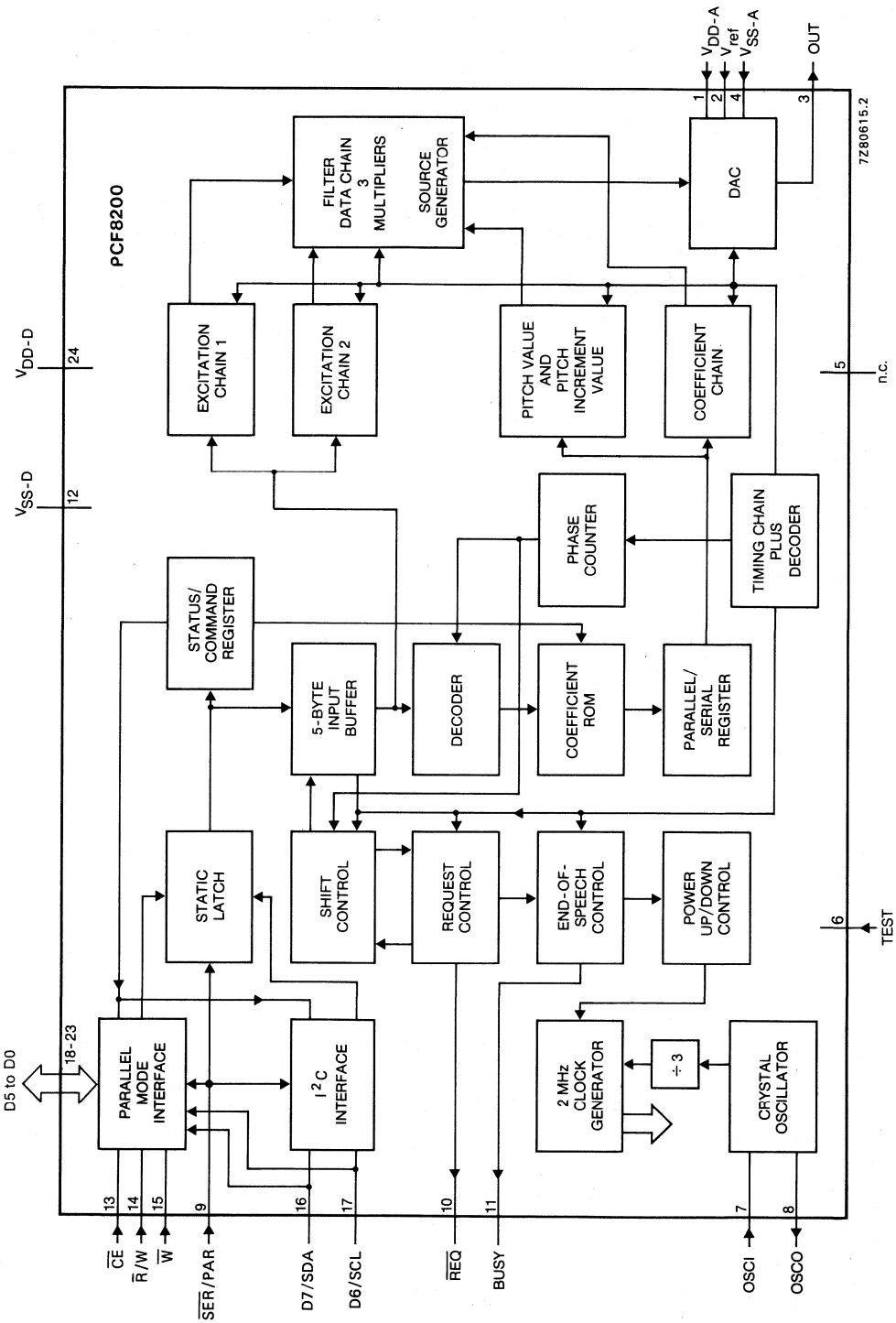


Fig. 1 Block diagram.

PINNING

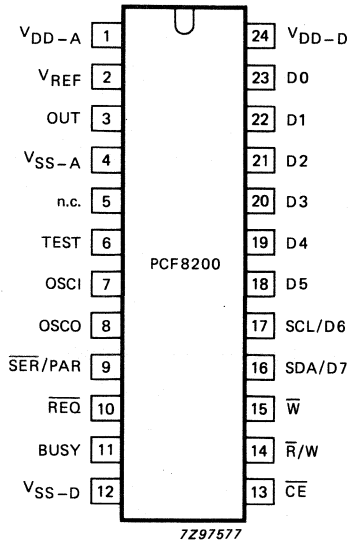


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

1	V_{DD-A}	positive supply voltage for DAC output stage
2	V_{REF}	DAC reference voltage input
3	OUT	speech output
4	V_{SS-A}	negative supply voltage for DAC stage
5	n.c.	not connected
6	TEST	for normal operation this pin must be grounded (V_{SS})
7	OSCI	oscillator input
8	OSCO	oscillator output
9	$\overline{SER}$/PAR	for parallel data bus operation this pin is hard-wired to V_{DD}, or to V_{SS} to enable the I^2C bus
10	$\overline{REQ}$	status bit indicating request for data
11	BUSY	status indicating synthesizer busy
12	V_{SS-D}	negative supply voltage for digital circuits
13	$\overline{CE}$	chip-enable input
14	R/$\overline{W}$	read/write control input
15	$\overline{W}$	write input
16	SDA/D7	I^2C bus serial data input/output (serial mode) or parallel data input/output D7 (parallel mode)
17	SCL/D6	I^2C bus serial clock input/output (serial mode) or parallel data input/output D6 (parallel mode)
18	D5	parallel data input/outputs
19	D4	
20	D3	
21	D2	
22	D1	
23	D0	
24	V_{DD-D}	positive supply voltage for digital circuits

FUNCTIONAL DESCRIPTION

The synthesizer has been designed for a vocal tract modelling technique of voice synthesis. An excitation signal is fed to a series of resonators. Each resonator simulates one of the formants in the original speech. It is controlled by two parameters, one for the resonant frequency and one for the bandwidth. Five formants are needed for male speech and four for female speech. The output of this system is defined by the excitation signal, the amplitude values and the resonator settings. By periodic updating of all parameters very high quality speech can be produced.

OPERATION

Speech characteristics change quite slowly, therefore the control parameters for the speech synthesizer can be adequately updated every few tens of milliseconds with interpolation during the interval to ensure a smooth changeover from one parameter value to the next. In the PCF8200 the standard-frame duration can be set to 8,8 , 10,4, 12,8 or 17,6 milliseconds with the speed-option, speaking speed, in the command-register.
The duration of each individual speech frame is programmable to be 1, 2, 3 or 5 times the standard-frame duration.

FD1, FD0	10	01	00	11	FS0, FS1
00	8,8	10,4	12,8	17,6	ms
01	17,6	20,8	25,6	35,2	ms
10	26,4	31,2	38,4	52,8	ms
11	44,0	52,0	64,0	88,0	ms

Table 1. Frame duration as a function of speed-option (FS1, FS0) and frame-duration (FD1, FD0).

The excitation signal is a random noise source for unvoiced sounds and a programmable pulse generator for voiced sounds. Both sources have an amplitude modulator which is updated 8 times in one speech-frame by linear interpolation. The pitch is updated every 1/8 of a standard frame.

The excitation signal is filtered with a five formant filter for male speech and a four formant filter for female speech. The formant filter is a cascade of all second-order sections. The control parameters, formant-frequency and formant-bandwidth, are updated eight times per speech frame by linear interpolation.
A block diagram of the formant synthesizer is shown in Fig. 3.

The filter output is upsampled to 80 kHz and filtered with a digital low-pass filter. Before the signal is digital to analogue converted (DAC), with an 11-bit switched capacitor DAC, the signal is multiplied with a DAC-amplitude factor. The use of a digital filter means that no external audio filtering is required for low-medium applications and minimal filtering is required for those applications requiring very high quality speech.

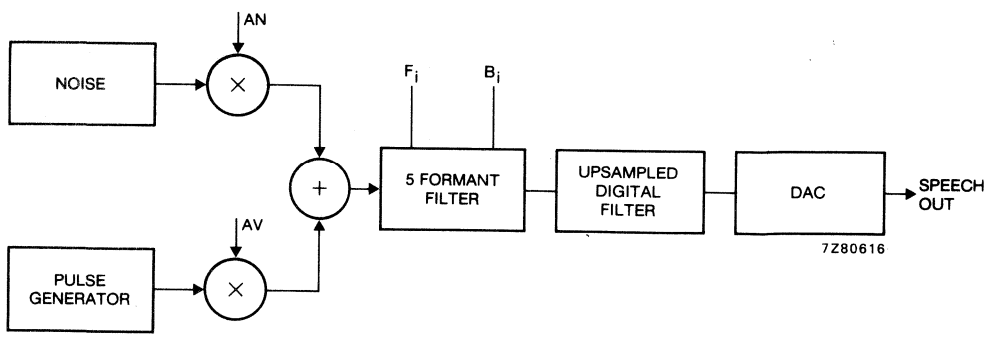


Fig. 3 Block diagram of formant synthesizer.

DATA FORMAT

Three types of format are used for data transfer to the synthesizer.

DAC-amplitude factor

The DAC-amplitude factor is one byte, which is used to optimize the digital speech signal to the 11-bit DAC. It is the first byte after a STOP or a BADSTOP or V_{DD} on. Table 2 indicates the amplitude factor.

byte	factor	dB
01110000	3,5	10,88
10110000	3,25	10,24
00110000	3,0	9,54
11010000	2,75	8,97
01010000	2,5	7,96
10010000	2,25	7,04
00010000	2,0	6,02
11100000	1,75	4,86
01100000	1,5	3,52
10100000	1,25	1,94
00100000	1,0	0,00
11000000	0,75	−2,50
01000000	0,5	−6,02
10000000	0,25	−12,04
00000000	0,0	
11110000	HEX code F0 is not allowed as a DAC amplitude	

Table 2 DAC amplitude factor.

Start pitch

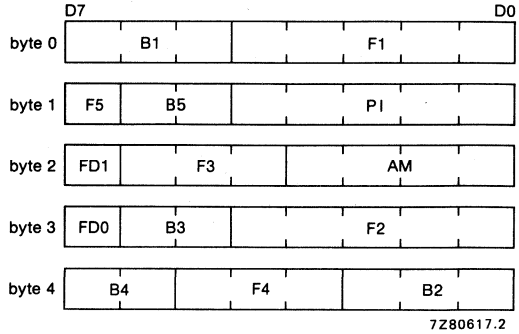
The second byte after a STOP or BADSTOP, or V_{DD} on is the start pitch. It is a one byte start value for the on-chip pitch-period generator.

Frame Data

The frame data is a five byte block which contains the filter and source information:

pitch increment/decrement value	5 bits
amplitude	4 bits
frame duration	2 bits
frequency of 1st formant	5 bits
frequency of 2nd formant	5 bits
frequency of 3rd formant	3 bits
frequency of 4th formant	3 bits
frequency of 5th formant	1 bit
bandwidth of 1st formant	3 bits
bandwidth of 2nd formant	3 bits
bandwidth of 3rd formant	2 bits
bandwidth of 4th formant	2 bits
bandwidth of 5th formant	2 bits
	40 bits = 5 bytes

The frame-data bits are organized as shown in Fig. 4.



It is not allowed to set byte 0 to the hexadecimal value 00.

Fig. 4 Format of frame-date.

CONTROL FORMAT

Command Write

A command write consists of two bytes, and it may occur before a data block. The four bits which can be written are shown in Fig. 5.

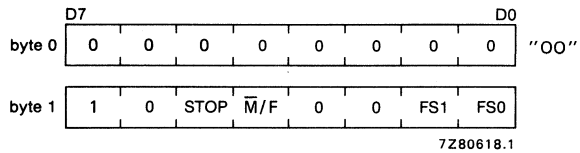


Fig. 5 Control write: first byte fixed, second byte control.

FS0, FS1 speed option

FS1	FS0	speech speed	standard-frame duration
0	0	100%	12,8 ms
0	1	145%	8,8 ms
1	0	123%	10,4 ms
1	1	73%	17,6 ms

$\overline{M}$/F, male/female option

$\overline{M}$/F = 0 male quantization table
= 1 female quantization table

STOP

STOP = 1 stop; repeat last complete frame with amplitude = 0 (no excitation signal)
= 0 if the frame data is not sent within the duration of a half frame, there will be a BADSTOP:

1. $\overline{REQ}$ = 1 STOP = 0
2. Repeat last frame with amplitude = 0
3. BUSY = 0

Status Read

Three status bits can be read out at any time without a preceding byte (00).
This is shown in Fig. 6.

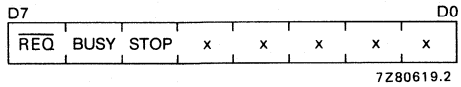


Fig. 6 Status read.

$\overline{REQ}$	= 1	No data required
	= 0	Synthesizer requesting for new data
BUSY	= 1	Busy (an utterance is pronounced)
	= 0	Idle, $\overline{REQ}$ will set to 1; the synthesizer is in STOP or BADSTOP mode
STOP		The STOP bit is the same as the stop bit written to the synthesizer during a command write. STOP = 1, BUSY = 0 stopped by the user. STOP = 0, BUSY = 0 BADSTOP because the data was not sent in time.

After initial power-up the status/command register is set to the following status:

FS0, FS1	= 0	Standard-frame duration of 12,8 ms
$\overline{M}$/F	= 0	Male quantization table
STOP	= 0	
BUSY	= 0	Idle
$\overline{REQ}$	= 1	No data required

DEVELOPMENT DATA

INTERFACE PROTOCOL

Data can be written to the synthesizer when $\overline{REQ}$ = 0 or, when $\overline{REQ}$ = 1 and BUSY = 0. Figure 7 shows the interface protocol of the synthesizer.

In parallel mode the synthesizer is activated by sending the DAC-amplitude factor. In serial mode the DAC-amplitude factor can be sent as soon as the synthesizer is powered-up.

The I²C transmitter/receiver will then acknowledge. When the request for the pitch-byte occurs the byte must be provided within the duration of a half standard frame. If the byte is not provided in time a BADSTOP will be generated.

During each data write operation, the status bit $\overline{REQ}$ will be set to '1'.
Within a frame data block, it disappears within a few microseconds, asking for the next byte of that block. If the bytes of frame data are not provided within the time-duration of a half frame, a BADSTOP will be generated.

I²C ADDRESS

On chip there is a I²C slave receiver/transmitter with the address:

7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	R/W

POWER UP

The synthesizer will be set to power-up on a parallel-write sequence.

PAR-mode: The input-latches are active so they can receive the first byte

SER-mode: The I^2C transmitter/receiver will not acknowledge until the synthesizer has powered-up. To power up the synthesizer a parallel write sequence (Fig. 9) must be made to the synthesizer by using external logic for the control lines; at least one line must be toggled, $\overline{CE}$, while $\overline{W} = 0$ and $\overline{R}/W = 1$.
The synthesizer can be set to permanent power-up by hard-wired control pins ($\overline{CE} = 0$, $\overline{R}/W = 1$, $\overline{W} = 0$).

POWER DOWN MODE

When BUSY = 0 the synthesizer will be set to power-down. In the power-down mode the status/command register will be retained.
In power-down mode the clock-oscillator is switched off. After initial V_{DD} the synthesizer is in power-down mode.

HANDLING

All inputs and outputs are protected against electrostatic charge under normal handling conditions.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	any pin with respect to V_{SS}	V_{DD}	−0,3	7,5	V
Input voltage	any pin with respect to V_{SS}	V_I	−0,3	7,5	V
Output voltage	any pin with respect to V_{SS}	V_O	−0,3	7,5	V
D.C. input diode current	$V_I < V_{SS}$	$-I_{IK}$	–	20	mA
	$V_I > V_{DD}$	I_{IK}	–	20	mA
D.C. output diode current	$V_O < V_{SS}$	$-I_{OK}$	–	20	mA
	$V_O > V_{DD}$	I_{OK}	–	20	mA
Operating ambient temperature range		T_{amb}	−40	85	°C
Storage temperature range		T_{stg}	−55	125	°C

DEVELOPMENT DATA

CHARACTERISTICS

T_{amb} = −45 to + 85 °C; supply voltage (V_{DD} to V_{SS}) = 4,5 to 5,5 V with respect to V_{SS}, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	10	–	mA
Standby current	$I_{DD(SB)}$	–	200	–	μA
Inputs					
$\overline{CE}$, $\overline{R}/W$, $\overline{W}$					
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current V_{in} = 0 to 5,5 V	I_{IR}	−10	–	10	μA
Rise and fall times (note 2)	t_{rf}	–	–	50	ns
Input capacitance	C_I	–	–	7	pF
OSCI					
Input voltage HIGH	V_{IH}	2,2	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current V_{in} = 0 to 5,5 V	I_{IR}	−10	–	10	μA
Rise and fall times (note 2)	t_{rf}	–	–	50	ns
Input capacitance	C_I	–	–	7	pF
PARALLEL MODE					
Input Characteristics (D0 to D7)					
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current (V_{in} = 0 to 5,5 V, output off)	I_{IR}	−10	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output Characteristics (D5 to D7 only)					
Output voltage HIGH (I_{OH} = −100 μA)	V_{OH}	3,5	–	V_{DD}	V
Output voltage LOW (I_{OL} = 3,2 mA)	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Rise and fall times (note 3)	t_{rf}	–	–	50	ns
SERIAL MODE					
Input characteristics (SDA and SDL)					
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input leakage current (V_{in} = 0 to 5,5 V, output off)	I_{IR}	−10	–	10	μA
Input capacitance	C_I	–	–	10	pF

parameter	symbol	min.	typ.	max.	unit
Output Characteristics (SDA only, open drain)					
Output voltage LOW (I_{OL} = 3 mA)	V_{OL}	0	–	0,4	V
OSCILLATOR					
Crystal frequency	f_{XTAL}	–	6	6,1	MHz
V_{REF}					
Reference voltage	V_{REF}	1,9	–	$\frac{V_{DD}-1,5}{1,25}$	V
Input leakage current (active)	I_{IR}	–	5	–	μA
Outputs					
$\overline{REQ}$, BUSY					
Output voltage HIGH (I_{OH} = 100 μA)	V_{OH}	3,5	–	V_{DD}	V
Output voltage LOW (I_{OL} = 3,2 mA)	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Rise and fall times (note 3)	t_{rf}	–	–	50	ns
OUT					
Output voltage	V_{OUT}	0,66 x V_{REF}		1,34 x V_{REF}	V
Minimum external load		600	–	–	Ω
Timing characteristics (note 1) (Figs 8 and 9)					
Write enable	t_{WR}	200	–	–	ns
Data set-up for write	t_{DS}	150	–	–	ns
Data hold for write	t_{DH}	30	–	–	ns
Read enable	t_{RD}	200	–	–	ns
Data delay for read (note 2)	t_{DD}	–	–	150	ns
Data floating for read (note 2)	t_{DF}	–	–	150	ns
Control set-up	t_{CS}	0	–	–	ns
Control hold	t_{CH}	0	–	–	ns
REQ new (new byte of the same speech frame)	t_{RN}	–	# (≈ 3)		μs
REQ Valid	t_{RV}	0	–	–	ns
REQ Hold	t_{RH}	–	250	#	ns

NOTES TO THE CHARACTERISTICS

1. Timing reference level is 1,5 V; supply 5 V ± 10%; temperature range of −40 °C to 85 °C.
2. Levels greater than 2 V for a '1' or less than 0,8 V for a '0' are reached with a load of one TTL input and 50 pF.
3. Rise and fall times between 0,6 V and 2,2 V levels.

Values not yet available.

DEVELOPMENT DATA

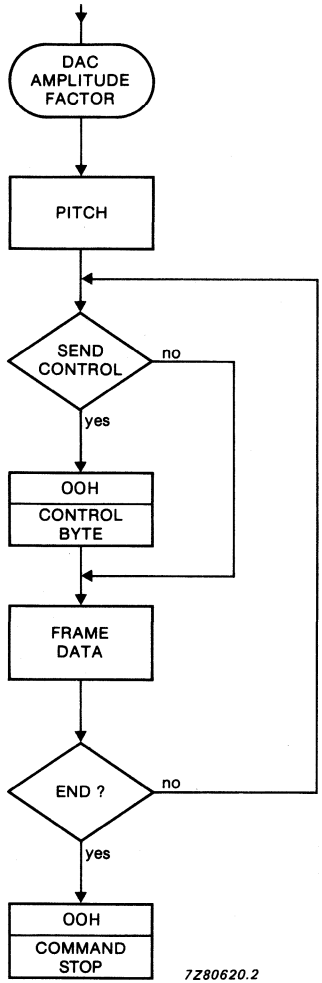
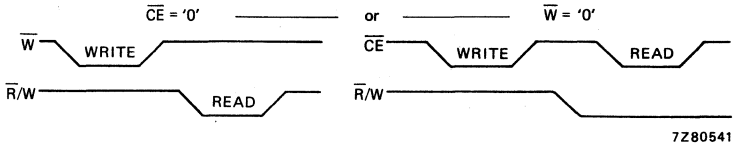


Fig. 7 Interface protocol.

Timing diagrams

The control signals $\overline{CE}$, $\overline{R}/W$ and $\overline{W}$ have been specified to enable easy interface to most microprocessors and microcomputers. For instance with connection to an MAB8048 microcomputer the $\overline{R}/W$ and $\overline{W}$ inputs can be used as the RD and WR strobe inputs.



Typical connection of control signals.

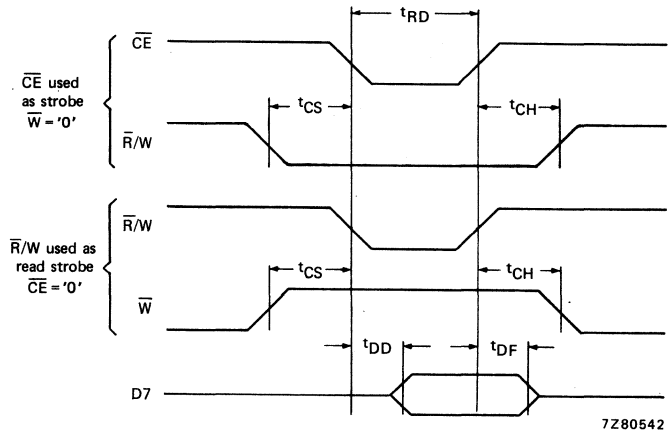


Fig. 8 Read timing.

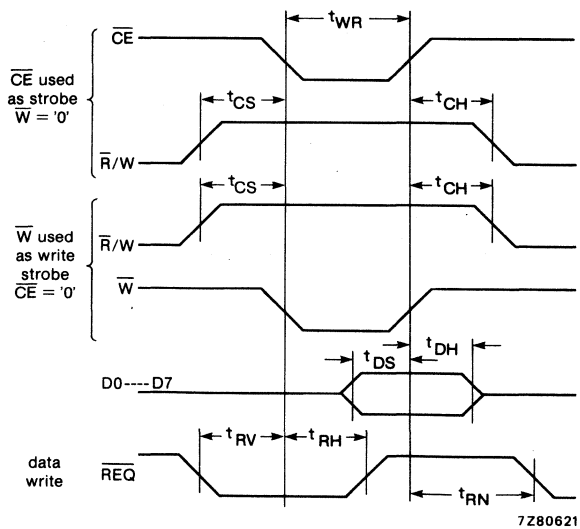


Fig. 9 Write timing.

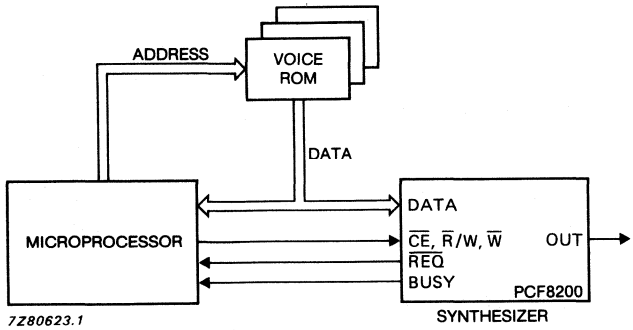


Fig. 10 Typical application configuration with parallel interface.

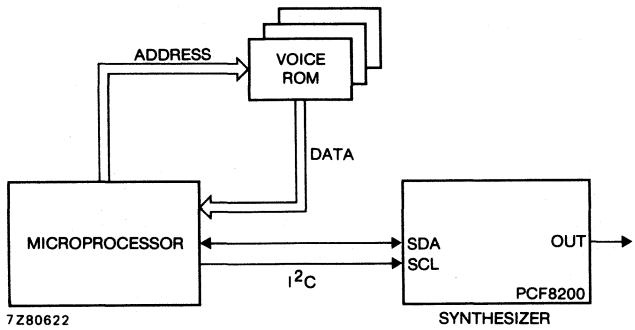


Fig. 11 Typical application configuration with series interface.

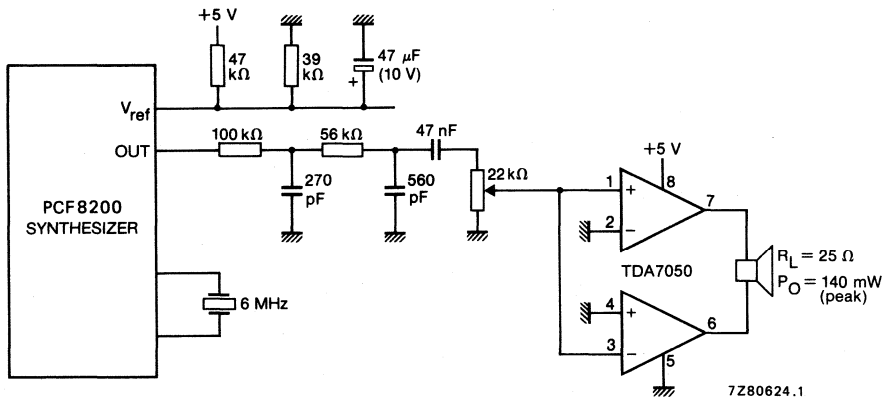


Fig. 12 An example of an output configuration.

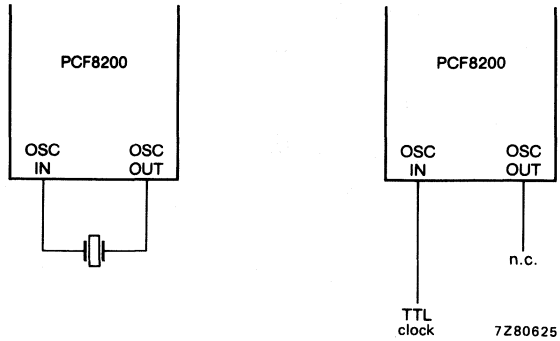


Fig. 13 Oscillator clock configurations.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Single-chip 8-bit microcontroller family specification

PCF84CXXX

1 INTRODUCTION

This family data sheet describes the microcontroller core which is common for all members of the PCF84CXXX family. For complete information of a particular microcontroller, consult both the specific microcontroller data sheet and this family data sheet.

2 FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single package
- Up to 8 K bytes ROM
- Up to 256 bytes RAM
- Over 80 instructions, all instructions 1 or 2 cycles
- 8 or more quasi bi-directional I/O port lines
- 8-bit programmable timer/event counter
- 3 single-level vectored interrupts (external, 8-bit programmable timer/counter, SIO/derivative)
- 2 Test inputs: T0 (may also be used as an interrupt) and T1 (may also be used as an input to an 8-bit counter)
- Serial I/O interface (not all devices)
- Power-on-reset
- 2 power reduction modes: Idle and Stop
- V_{DD} supply range: 2.5 V to 5.5 V
- Clock frequency range: 450 kHz to 10 MHz
- Operating temperature range: −40 °C to 85 °C
- Silicon gate CMOS fabrication process

3 GENERAL DESCRIPTION

The PCF84CXXX single-chip 8-bit microcontroller family consists of a wide range of derivatives containing up to 8 K bytes of on-chip mask programmable program ROM and up to 256 bytes RAM. All devices include flexible I/O ports, an 8-bit programmable timer/event counter and a choice of single-level vectored interrupts. The instruction set is based on that of the MAB8048.
A number of PCF84CXXX family members may be used as CMOS replacements for their NMOS counterparts, where lower power consumption and higher speed are required.

The family is well supported with:

- Cross assemblers
- In-circuit emulation tools
- Window debugger
- Piggy-back versions for prototyping.

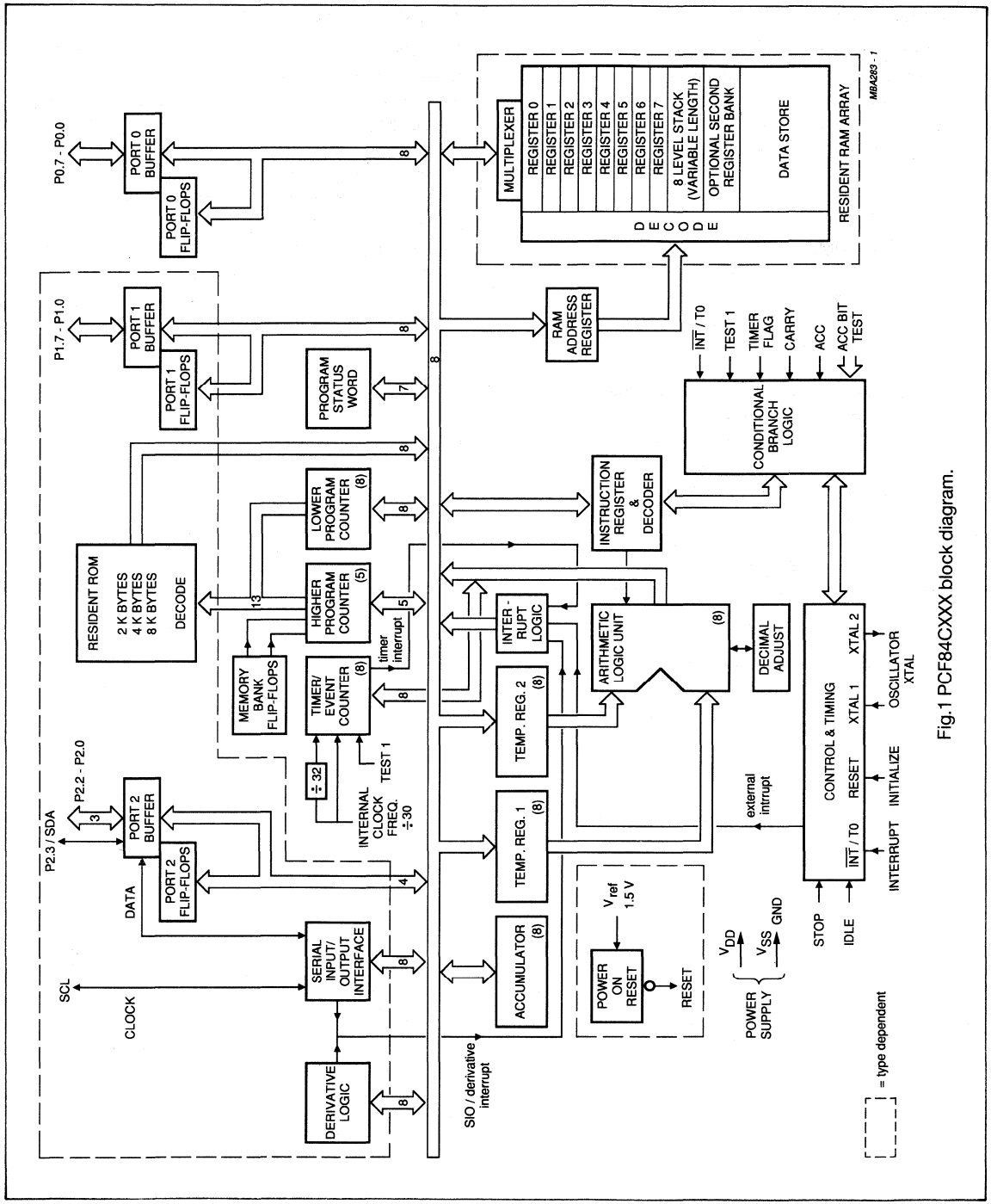


Fig.1 PCF84CXXX block diagram.

4 FUNCTIONAL DESCRIPTION

4.1 Program memory

Program memory consists of up to 8 K bytes of read-only memory (ROM). Each location is directly addressable by the program counter. The program memory is mask-programmed at the factory. Figure 2 shows the program memory map.

Four program memory locations are of special importance:

- Location 0: first instruction to be executed after the microcontroller is reset.
- Location 3: first instruction of an external interrupt ($\overline{INT}$/T0) service routine.
- Location 5: first instruction of an SIO/derivative interrupt service routine.
- Location 7: first instruction of a timer/event counter interrupt service routine.

Of the 13-bits in the program counter, only 11 function as a counter. The two most significant bits are preset by SEL MB instructions. Thus, program memory is arranged in banks of 2 K bytes. Memory bank boundaries can only be crossed using unconditional branches (JMP) or subroutine calls (CALL) after the appropriate memory bank has been selected by a SEL MB instruction.

Each program memory bank is further divided into 8 pages of 256 bytes. Indirect (JMPP) and conditional branches can't cross page boundaries.

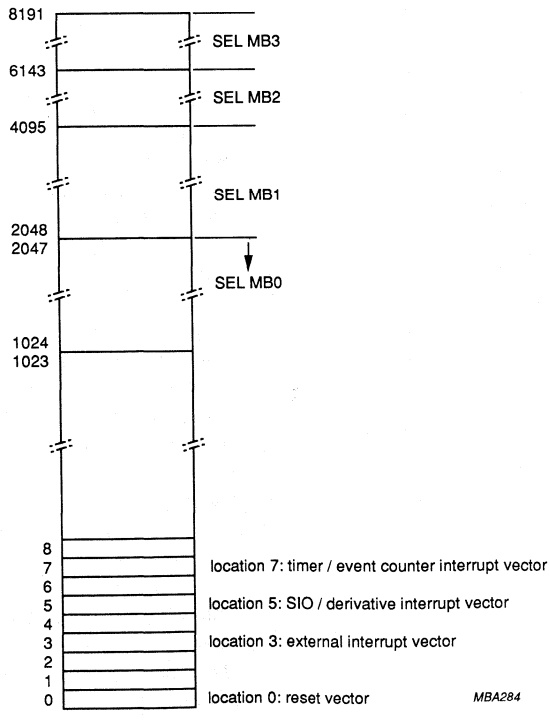


Fig.2 Program memory map.

4.2 Data memory

Data memory consists of up to 256 bytes of random access memory (RAM). All locations are indirectly addressable using RAM pointer registers. Up to 16 register locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. All RAM locations make efficient program loop counters when used with the 'decrement register and test' instruction DJNZ. Figure 3 shows the data memory map.

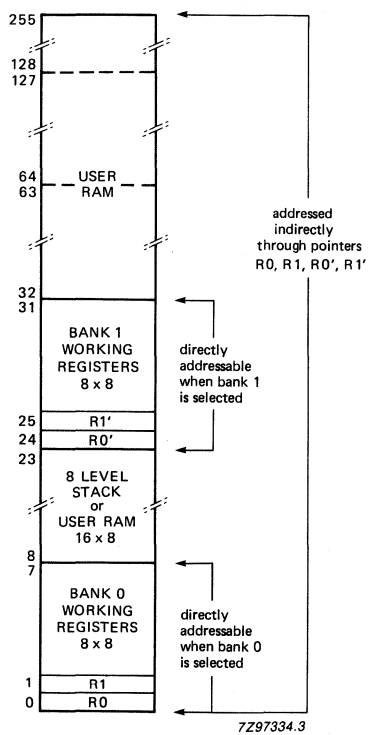


Fig.3 Data memory map.

4.2.1 Working registers

Locations 0 to 7 may be selected as working registers by the SEL RB0 instruction. These locations may then be accessed using efficient one byte, one cycle instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents make the working registers ideal for frequently accessed intermediate results.

Instead of locations 0 to 7, locations 24 to 31 may be selected as working registers by the SEL RB1 instruction. Register bank 1 may be used as an extension of register bank 0, as an alternative register bank for use by interrupt service routines, or as general purpose data memory.

The first two locations of each bank contain the RAM pointer registers (R0, R1, R0' and R1') which indirectly address all RAM locations.

4.2.2 Program counter stack

Locations 8 to 23 may be used as an 8-level program counter stack reserving 2 locations per level, or as general purpose RAM. The stack (Fig.4) saves return addresses and status during interrupt or subroutine servicing. Up to 8 levels of subroutine/interrupt nesting is possible.

A 3-bit stack pointer always points to the next free stack level. Following a device reset, the stack pointer points to level 0 (locations 8 and 9). On each subroutine call or interrupt, the contents of the 13-bit program counter and bits 4, 6 and 7 of the program status word are transferred to the level indicated by the stack pointer. The stack pointer increments and points to the next free level. Overflow from level 7 to level 0 occurs after nesting eight levels deep. Further subroutine calls and/or interrupts should be avoided since the contents of level 0 would be overwritten and lost.

The RETR instruction must be used to terminate an interrupt service routine. The RETR instruction decrements the stack pointer, and restores the program counter and status word. A subroutine should be terminated with the RET instruction. The RET instruction restores the program counter but does not restore the program status word.

As a general rule, the use of RETR in conjunction with a subroutine call is not recommended. RETR must not be used to terminate a subroutine which has been called within an interrupt routine since it would prematurely terminate the interrupt routine.

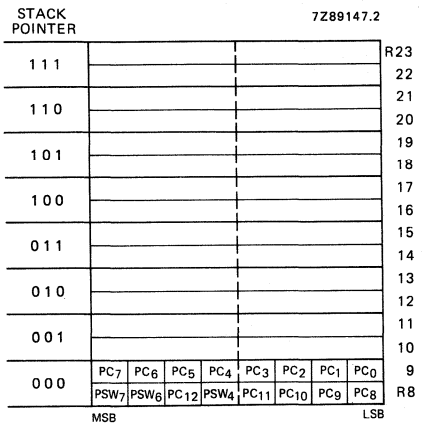


Fig.4 Program counter stack.

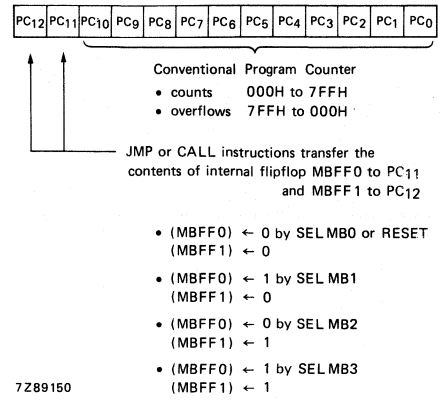


Fig.5 Program counter.

4.3 Program counter

The 13-bit program counter can address up to 8 K bytes of ROM (Fig.5). The least significant 11 bits (PC0 to PC10) are auto-incrementing. The two most significant bits, PC11 and PC12, are loaded with the contents of two internal flip flops (MBFF0 and MBFF1 respectively) when a JMP or CALL instruction is executed. The contents of these two internal flip-flops can be altered by the SEL MB instructions.

4.4 Program status word

The program status word (PSW) is an 8-bit register in the CPU which stores information about the current status of the microcontroller (Fig.6).

All bits can be read using the MOV A,PSW instruction. Only the PS bit can be written using the MOV PSW,A instruction. Table 1 describes the PSW bits and how they are affected.

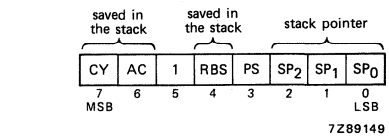


Fig.6 Program status word.

Table 1 Program status word.

BIT	NAME	FUNCTION	AFFECTED BY
7	CY	Carry, signals accumulator overflow	ADD, ADDC, DA, RLC, RRC, CLR C and CPL C instructions
6	AC	Auxiliary Carry, half carry	ADD and ADDC instructions
5	-	Not used, always 1 when read	
4	RBS	Register Bank Select 0: select register bank 0 1: select register bank 1	SEL RB instructions
3	PS	Timer Prescaler Select 0: prescaler selected (÷32) 1: prescaler not selected (÷1)	MOV PSW,A instruction
2 1 0	SP2 SP1 SP0	Stack Pointer bits 2-0	CALL, RET, RETR instructions and interrupts

Table 2 Interrupts.

INTERRUPT			INSTRUCTION	
PRIORITY	TYPE	VECTOR LOCATION	ENABLE	DISABLE
1 (highest)	external	003 (ROM)	EN I	DIS I
2	SIO/derivative interrupt	005 (ROM)	EN SI	DIS SI
3 (lowest)	timer/event counter	007 (ROM)	EN TCNTI	DIS TCNTI

4.5 Central processing unit

The PCF84CXXX instruction set provides arithmetic, logical, branching, input/output, and control facilities. The DA A, SWAP A, and XCHD instructions simplify BCD arithmetic and nibble handling. The MOVP A,@A instruction enables efficient table look-up within the current ROM page. The instruction set also has facilities for conditional branching and loop control (DJNZ).

4.6 Interrupts

The PCF84CXXX family handles external, SIO/derivative and timer/event counter interrupts. The interrupt mechanism is single level. An executing interrupt routine can only be interrupted by a hardware RESET; it can't be interrupted by other interrupts (which are latched).
If several interrupt requests are detected simultaneously, they are serviced in order of priority (see Table 2).

An interrupt request will only be serviced if the corresponding interrupt enable flag is set (Fig.7). When a request is serviced, the contents of the program counter, and bits 4, 6 and 7 of the program status word are saved on the program counter stack. The program counter is loaded with the appropriate interrupt vector which points to the start of the interrupt service routine. Since the accumulator is not automatically saved, it must be saved and restored by user software. The interrupt routine must be terminated by the RETR (return and restore) instruction. At least one instruction in the main program will then be executed before another interrupt routine is serviced.

To avoid erroneous real-time programs, a few words of caution:

- While the interrupt is in progress, the two most significant bits of the program counter are frozen at zero. Thus, interrupt routines and subroutines called from interrupt routines must reside (entirely) in memory bank 0.
- The SEL MB instruction should not be used within interrupt routines or in subroutines called within interrupt routines because altering the contents of MBFF0 and MBFF1 (Fig.5) may lead to erroneous JMP and CALL destinations after return from interrupt.
- Subroutines and nested subroutines called within an interrupt routine must all end with RET since RETR clears the IIP (interrupt in progress) flag (Fig.7 and Fig.8). Further pending interrupts would then interfere with the interrupt routine in progress.

4.6.1 EXTERNAL INTERRUPT

A HIGH-to-LOW transition on the $\overline{INT}$/T0 pin is latched in the digital filter latch if the LOW state exceeds 7 clock periods after a HIGH state of more than 4 clock periods. If the external interrupt is enabled, then the external interrupt flag (EIF) will also be asserted, constituting a valid external interrupt request. As soon as the IIP is clear, indicating that no interrupt routine is in progress, the external interrupt is invoked by a forced CALL to location 3. The EIF flag is simultaneously cleared (Fig.7 and Fig.8). The interrupt routine may acknowledge the interrupt via port lines.

Execution of a DIS I (disable external interrupt) instruction cancels a stored interrupt request by clearing both the digital filter latch and the EIF.

EI	External Interrupt
SI	SIO/Derivative Interrupt
TI	Timer/event counter Interrupt
EIF	External Interrupt Flag
TIF	Timer Interrupt Flag
PIN	Pending Interrupt Not
IIP	Interrupt In Progress Flag

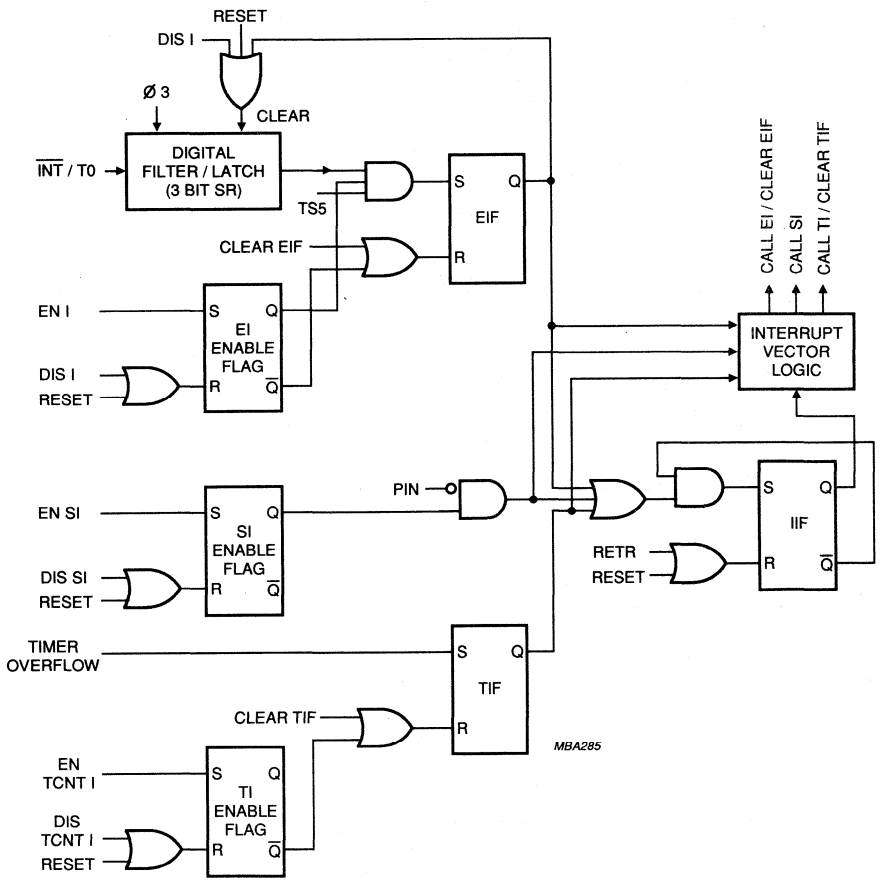
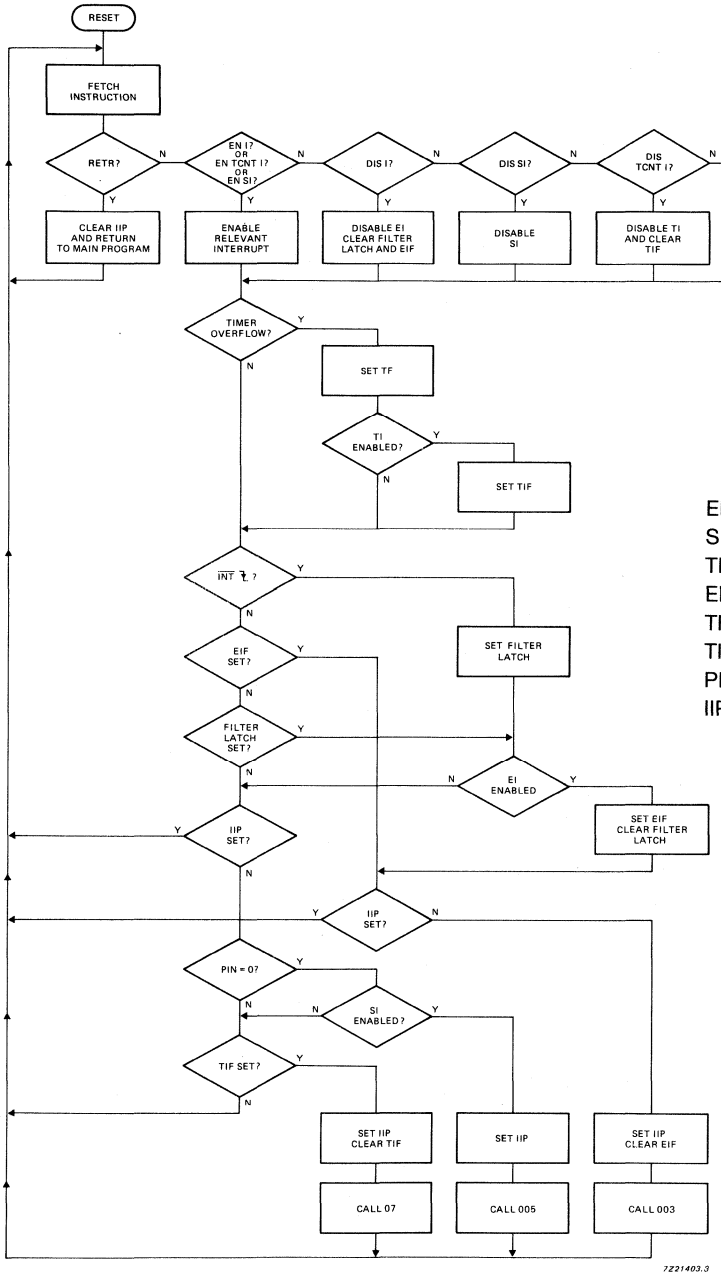


Fig.7 Simplified interrupt logic schematic (the R input overrules the S input for all flags).



EI	External Interrupt
SI	SIO/Derivative Interrupt
TI	Timer/event counter Interrupt
EIF	External Interrupt Flag
TF	Timer Flag
TIF	Timer Interrupt Flag
PIN	Pending Interrupt Not
IIP	Interrupt In Progress Flag

Fig.8 Flow chart illustrating CPU control in the presence of interrupts.

4.6.2 SIO/Derivative interrupt

The SIO/derivative interrupt is shared between the serial I/O interface (if available) and the derivative logic (if available). Software polling may be necessary to determine the origin of a request.

An interrupt request from the SIO or derivative logic will force the PIN flag to its active LOW state. This action is independent of the Enable SIO interrupt enable flag. If the SIO/derivative interrupt is enabled and no interrupt routine is in progress, the active LOW PIN flag will invoke the SIO/derivative interrupt routine by forcing a CALL to program memory location 5. Invoking the SIO/derivative interrupt routine does not automatically clear the PIN flag. PIN must be cleared to its inactive HIGH state by software during the interrupt routine.

More details on SIO interrupts are given in the section on the serial I/O interface. For specific information on derivative interrupts, consult the relevant data sheet.

4.6.3 Timer/event counter interrupt

When the timer/event counter interrupt is enabled, a timer/event counter overflow sets the Timer Interrupt Flag (TIF). As soon as the Interrupt in Progress (IIP) flag is clear (indicating that no interrupt routine is in progress), the timer/event counter interrupt routine is invoked by a forced CALL to program memory location 7, and the TIF flag is simultaneously cleared (Fig.7 and Fig.8).

Execution of a DIS TCNTI (disable timer/event counter interrupt) instruction cancels a stored interrupt request by clearing the TIF flag.

An additional external interrupt may be simulated by enabling the timer/event counter (EN TCNTI) and loading the counter with FFH (one less than overflow). If the event counter mode is enabled by executing the STRT CNT instruction, a rising edge on the T1 input will cause a counter overflow and set TIF.

4.7 Interrupt/Test 0 input ($\overline{INT}$/T0)

The $\overline{INT}$/T0 input may be used as:

- an external interrupt
- a test 0 input for branch instructions JT0 and JNT0.

When used as a test 0 input (external interrupt disabled):

- the conditional branch instruction JT0 will cause a branch if $\overline{INT}$/T0 = logic 1
- the conditional branch instruction JNT0 will cause a branch if $\overline{INT}$/T0 = logic 0.

There is no internal pull-up or pull-down resistor connected to the $\overline{INT}$/T0 input. When $\overline{INT}$/T0 is not used, it must be tied to V_{DD} or V_{SS}.

4.8 Timer/event counter

The internal 8-bit up-counter may be configured to count external events, modulo-32 machine cycles, or machine cycles directly. The MOV A,T and MOV T,A instructions can be used to read and preset the counter.

After a STRT T (start timer) instruction, the counter will increment either every machine cycle (30 oscillator periods) or every 32 machine cycles. If the PS bit in the program status word is set, the counter increments every machine cycle. If the PS bit is reset, it increments every 32 machine cycles. STRT T clears the prescaler which is not otherwise accessible (see Fig.9).

After a STRT CNT (start event counter) instruction, the counter will count each LOW-to-HIGH transition on pin T1 provided that the HIGH state exceeds 4 oscillator periods after a LOW state of more than 4 oscillator periods. The maximum count rate is one increment per machine cycle (f_{XTAL}/30).

The timer/event counter is inhibited after reset or by executing a STOP TCNT (stop timer/event counter) instruction (see Fig.9).

When a T1 overflow occurs:

- if the timer/event counter interrupt is enabled, the Timer Interrupt Flag (TIF) is set and an interrupt request is generated
- the Timer Flag (TF) is set. TF can be tested by conditional branch instructions JTF (jump if TF = logic 1) and JNTF (jump if TF = logic 0). When a JTF or JNTF instruction is executed, TF is reset. The only other way to clear TF is to reset the microcontroller.

Table 3 Timer/event counter control.

FUNCTION	TIMER MODE	COUNTER MODE
clear	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
preset	MOV T,A	MOV T,A
start	STRT T	STRT CNT
stop	STOP TCNT or RESET	STOP TCNT or RESET
test	JTF/JNTF	JTF/JNTF
read	MOV A,T	MOV A,T

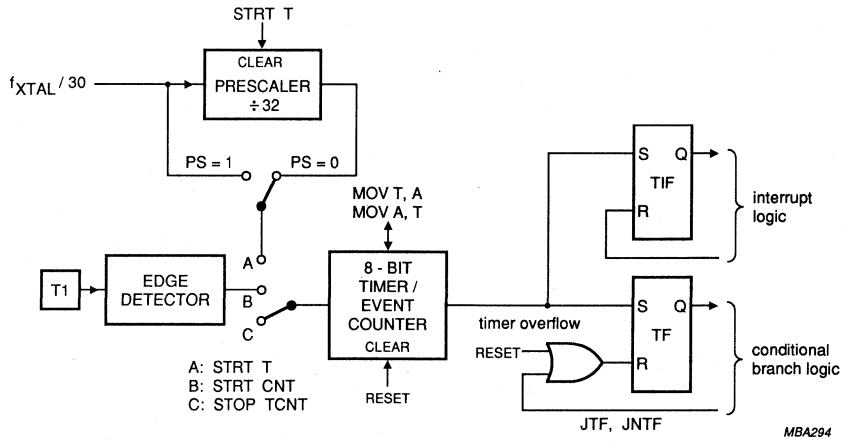


Fig.9 Timer/event counter.

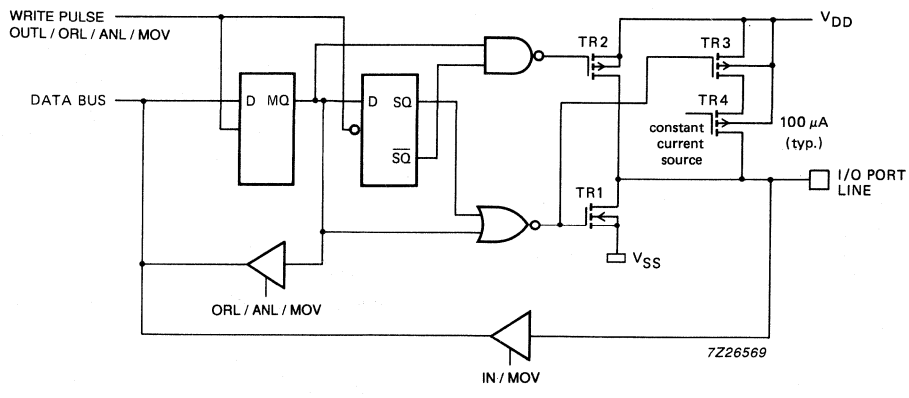


Fig.10 Standard port with switched pull-up current source (mask option 1).

4.9 Test 1/Count input (T1)

The T1 input may be used as:
- a count input to the 8-bit timer/event counter
- a test 1 input for branch instructions JT1 and JNT1.

When used as a test input:
- the conditional branch instruction JT1 will cause a branch if T1 = logic 1
- the conditional branch instruction JNT1 will cause a branch if T1 = logic 0.

There is no internal pull-up or pull-down resistor connected to the T1 input. When T1 is not used, it must be tied to V_{DD} or V_{SS}.

4.10 Parallel ports

The PCF84CXXX family provides up to three standard quasi-bidirectional I/O ports:
- Port 0: 8-bit parallel port (P0.0 to P0.7)
- Port 1: 8-bit parallel port (P1.0 to P1.7)
- Port 2: 4-bit parallel port (P2.0 to P2.2, P2.3/SDA)

Several members of the PCF84CXXX family provide all 20 I/O lines and all members contain port 0.

In addition to the standard ports, many PCF84CXXX microcontrollers provide a variety of derivative ports. For specific details, consult the relevant data sheet.

In general, all parallel ports lines can be individually configured as outputs or inputs. Output data written to a port is latched and remains unchanged until rewritten. Input data is not latched and must be stable when read by an input instruction.

The standard port configuration is shown in Fig.10. When a logic 0 is written to the master/slave flip-flop, TR2 and TR3 are turned off, turning off the constant current source. Current sinking is provided by TR1 which is simultaneously turned on, and the output is pulled LOW to V_{SS}.

When a logic 1 is written to the master/slave flip-flop for the first time (MQ = 1, SQ = 0), TR1 is turned off and TR3 is turned on. TR2 is also switched on for the duration of the internal write pulse (one oscillator period), driving the output rapidly to V_{DD}. TR3 turns on the constant current source TR4 which sources sufficient current for a TTL HIGH level; however, the port line can be pulled LOW by an external CMOS device, enabling the same pin to be used for both input and output. This arrangement also facilitates wired-OR applications. Subsequent writing of a logic 1 to the port line will not switch TR2 on. Booster transistor TR2 is only turned on for one oscillator period during a 0-to-1 transition at the output of the master/slave flip-flop.

To use the port line as an input, a logic one must written to the port line to turn TR1 off.

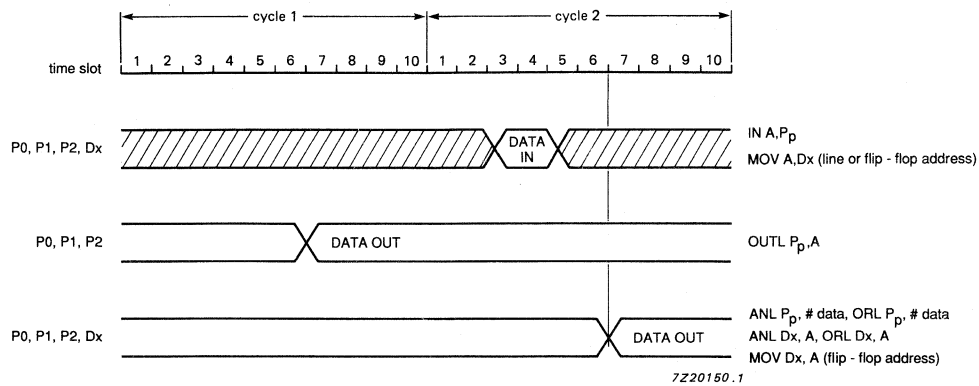


Fig.11 Input/output timing of standard and derivative ports.

Table 4 Derivative port addressing.

DERIVATIVE ADDRESS	TYPE	ACCESS
8-bit line address	R	derivative port line
8-bit flip-flop address	R/W	derivative port flip-flop

Ports 0, 1 and 2 are accessed using the parallel input/output instructions IN, OUTL, ANL and ORL. IN inputs port data to the accumulator. OUTL outputs accumulator data to the port. ANL and ORL are used to manipulate data in the port flip-flops.

Derivative ports are accessed by the derivative input/output instructions MOV, ANL and ORL. ANL and ORL are used to manipulate data in the port flip-flops. MOV is used for all data transfers between the port and the accumulator. When reading data into the accumulator, the data source can be a port line or the port flip-flop. Thus, two derivative addresses are provided per port (see Table 4).

All standard and derivative port accesses are performed by two-cycle instructions. Instruction timing is shown in Fig.11. For input operations, data is read during time slots 3 and 4 of machine cycle 2. For output operations, the data is written during time slot 7. For OUTL, data is written during machine cycle 1. For ANL, ORL and MOV Dx,A, data is transferred during machine cycle 2.

Three I/O mask options make it possible for every parallel I/O port line to be individually configured as follows:

Option 1 Standard Port: quasi-bidirectional I/O with switched pull-up current source (100 μA typ.) and p-channel booster transistor TR2. TR2 is only active for 1 clock cycle during 0-to-1 transitions (Fig.10).

Option 2 Open Drain: quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires the connection of an external pull-up resistor (Fig.12). If unused, an option 2 output should be tied to V_{SS} to prevent undesirable current flow through input stages.

Option 3 Push-Pull: outputs can sink or source 2 mA (typ.) at V_{DD} = 3 V. Push-pull lines may not be used as inputs (Fig.13).

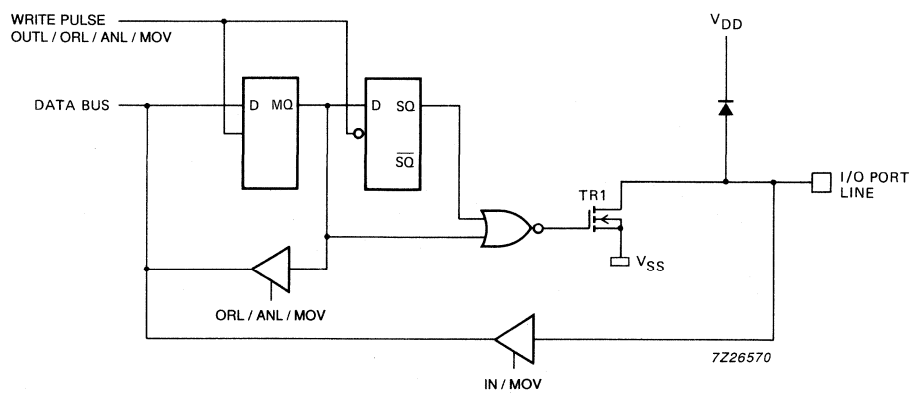


Fig.12 Open drain (mask option 2).

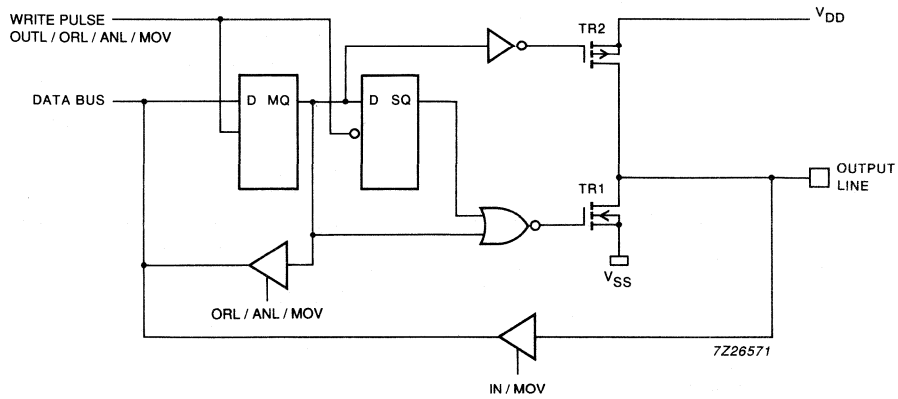


Fig.13 Push-pull (mask option 3).

For devices with a serial I/O interface, P2.3 becomes SDA and must be configured as an open drain (option 2) I/O line.

For the remaining port lines (P0.0 to P2.2), all three options are generally available. For some family members, option 3 on port 0 and port 1 lines may be restricted for emulation purposes. For specific information, refer to the relevant data sheet.

4.11 Serial I/O interface

Many members of the PCF84CXXX family have an on-chip serial I/O interface (I^2C). This two-line serial bus extends the microcontroller capabilities since it fully supports the PCF85XX (clips) family of I^2C-bus peripheral devices.

Microcontrollers that do not have dedicated serial I/O hardware can use port pins and software to simulate a serial interface. However, such microcontrollers must continuously monitor the serial bus, the data transfer rate is slower, and this approach may require significant processing and memory resources.

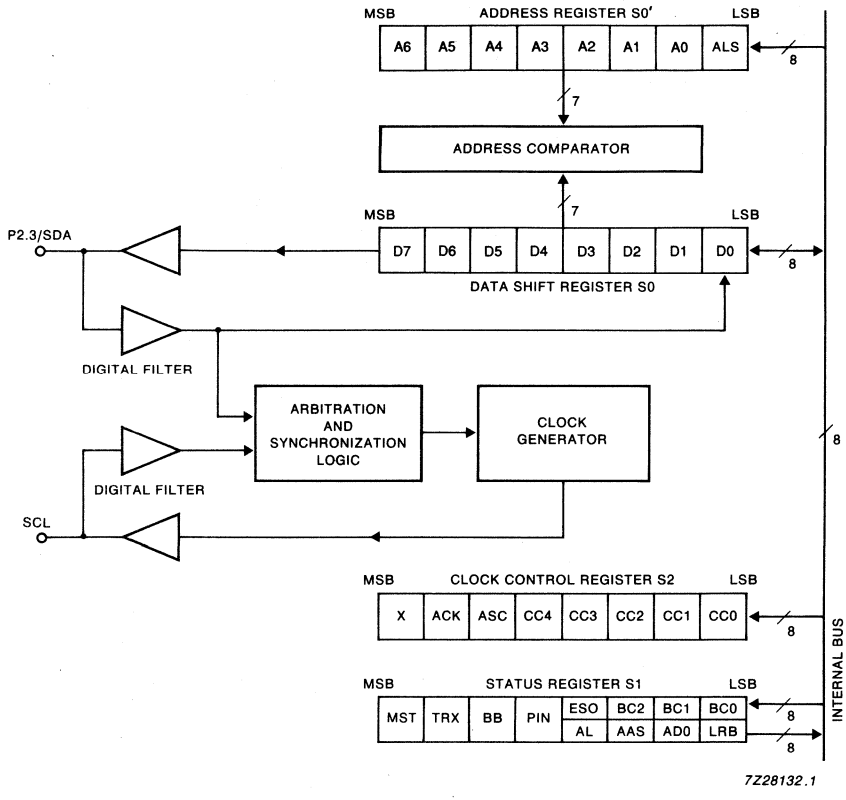
Each device on the I^2C-bus is allocated a 7-bit address. Address recognition is performed by the serial interface hardware and the microcontroller is interrupted only after a valid address (own address or general call address) has been recognized. The SIO hardware also transfers data serially and performs parallel-to serial and serial-to-parallel conversion without disrupting program execution. The microcontroller is interrupted only after a complete data byte has been transferred; the next data byte can then be written to or read from the serial I/O interface.

The serial I/O interface also facilitates the implementation of multimaster systems in which two or more microcontrollers communicate via the same I^2C-bus. An automatic arbitration procedure handles bus conflicts.

The I^2C-bus consists of a dedicated bidirectional clock line (SCL) and a bidirectional data line (P2.3/SDA) which also functions as parallel port line P2.3. When the serial I/O interface is enabled, P2.3 is disabled as a port line. Input signals on SCL and SDA are filtered for enhanced noise immunity. SCL and SDA are open drain and require external pull-up resistors if they are to be used as outputs. If unused, these two pins should be tied to V_{SS}.

The CPU and serial I/O interface communicate via the following four serial I/O interface registers (see Fig.14):

- Data Shift Register (S0)
- Address Register (S0')
- Clock Control Register (S2)
- Status Register (S1)



X = don't care

Fig.14 Serial I/O interface block diagram.

4.11.1 Data shift register (S0)

The data shift register converts serial data to parallel format and vice versa. The most significant bit is transferred first. An interrupt request is generated after a complete byte has been transferred or after a valid I²C-bus address has been detected. The MOV A,S0 instruction may be used to read S0; the MOV S0,A and MOV S0,#data instructions may be used to write to S0 if the ESO (enable serial I/O) bit in the status register (S1) is set.

4.11.2 Address register (S0')

The address register contains the device's 7-bit I²C-bus address and the ALS (always selected) bit. When ALS is zero (the recommended operating mode) bus transfers are ignored unless the START condition is immediately followed by the valid device address or the 'general call' address (00H). If ALS is set, any transfer on the bus is stored in the data shift register. The address register S0' is write-only. The MOV S0,A and MOV S0,#data instructions may be used to write to S0' if the ESO (enable serial I/O) bit in the status register (S1) is zero.

4.11.3 CLOCK CONTROL REGISTER (S2)

The clock control register is a write only register. Bits 0 to 4 of S2 define the serial clock frequency (f_{SCL}) as an integer multiple of the microcontroller clock frequency (Table 5).

Bit 5 (ASC) defines the asymmetrical clock duty cycle. If ASC is set, SCL has a duty cycle of approximately 75%. The asymmetrical clock limits the I²C-bus transmission rate to below 55 kHz. Divisors 39, 45 and 51 are not allowed if ASC is set. Resetting ASC (recommended operating mode) sets the SCL duty cycle to approximately 50%, allowing higher I²C-bus transmission rates of up to 100 kHz, and all of the divisors in Table 5 may be used.

For normal I²C-bus operation, bit 6 (ACK) must be set. After each byte transfer, an extra SCL pulse is generated during which the receiver may acknowledge reception. If ACK is reset, no acknowledge phase is available. This mode is used when a master receiver refuses to acknowledge a transfer in order to signal the 'end of transmission' to a slave transmitter.

Table 5 f_{SCL} as defined by the clock control register S2.

CC0 to CC4 (HEX)	f_{XTAL} DIVIDED BY	f_{SCL} (kHz) @ f_{XTAL} = 6 MHz	f_{SCL} (kHz) @ f_{XTAL} = 10 MHz
0	not allowed		
1	39	154*	256*
2	45	133*	222*
3	51	118*	196*
4	63	95	159*
5	75	80	133*
6	87	69	115*
7	99	61	101*
8	123	49	81
9	147	41	68
A	171	35	58
B	195	31	51
C	243	25	41
D	291	21	34
E	339	18	29
F	387	16	26
10	483	12	21
11	579	10	17
12	675	8.9	15
13	771	7.8	13.4
14	963	6.2	10.4
15	1155	5.2	8.7
16	1347	4.5	7.4
17	1539	3.9	6.5
18	1923	3.1	5.2
19	2307	2.6	4.3
1A	2691	2.2	3.7
1B	3075	2.0	3.3
1C	3843	1.6	2.6
1D	4611	1.3	2.2
1E	5379	1.1	1.9
1F	6147	1.0	1.6

* not permitted; f_{SCL} max. = 100 kHz in I²C systems

4.11.4 STATUS REGISTER (S1)

The status register controls the serial I/O interface and provides feedback about on-going bus transfers. Register S1 can be accessed by the MOV A,S1, MOV S1,A and MOV S1,#data instructions. The lower nibble of the status register is duplicated: control bits BC0-BC2 and ESO are write only, whereas feedback bits LRB, AD0, AAS and AL are read only. The status bits interact in intricate ways with each other. This must be kept in mind when developing an I²C-bus application. Table 6 describes the status bits.

4.11.4.1 Master bit (MST) and transmitter bit (TRX)

The MST and TRX bits determine the operating mode of the serial I/O interface. When not engaged in a bus transfer, MST and TRX should always be zero, placing the SIO in the slave receiver mode (see Fig.15). Return to the slave receiver mode is always performed by software. If the previous mode was a master mode, the transition (MOV S1,#D8H) involves a STOP condition, which automatically clears both MST and TRX.

The transition to the master transmitter mode is also performed by software. However, transitions to the master receiver and slave transmitter modes occur automatically if ALS = 0 (standard I²C-bus protocol). A slave receiver becomes a slave transmitter if the R/$\overline{W}$ bit in the valid address immediately following a START condition is set. A master transmitter becomes a master receiver if R/$\overline{W}$ is set in the transmitted address.

Table 6 Serial I/O status register (S1).

BIT	NAME	TYPE	DESCRIPTION
MST	Master	R/W	MST = 0: Slave (SCL input) MST = 1: Master (SCL output)
TRX	Transmitter	R/W	TRX = 0: Receiver (SDA/P2.3 input) TRX = 1: Transmitter (SDA/P2.3 output)
BB	Bus Busy	R/W	BB = 0: Bus inactive (R)/generates STOP condition (W) BB = 1: Bus busy (R)/generates START condition (W)
PIN	Pending Interrupt Not	R/W	PIN = 0: Serial interrupt pending (after byte transfer, valid address or lost arbitration); SCL forced to V_{SS} PIN = 1: No serial interrupt pending
ESO	Enable Serial I/O	W	ESO = 0: Serial I/O interface disabled; write access to S0' possible ES0 = 1: Serial I/O interface enabled; write access to S0 possible
BC0, BC1, BC2	Bit Counter	W	Preset of the Bit Counter for 1 up to 8 serial data bits. (001) = 1 bit, (010) = 2 bits, etc. (000) = complete byte (8 bits) = default value.
AL	Arbitration Lost	R	AL = 1: Arbitration Lost (bus conflict) AL = 0: When corresponding serial interrupt (PIN) is cancelled
AAS	Addressed As Slave	R	AAS = 1: Following a START condition if a valid address is detected (ALS = 0), or if the first byte is received (ALS = 1) AAS = 0: When corresponding serial interrupt (PIN) is cancelled
AD0	Address Zero	R	AD0 = 1: Following a START condition if the general call address (00H) is detected AD0 = 0: After a repeated START or a STOP condition
LRB	Last Received Bit	R	Set or reset depending on last bit transferred, acknowledgement bit if ACK = 1

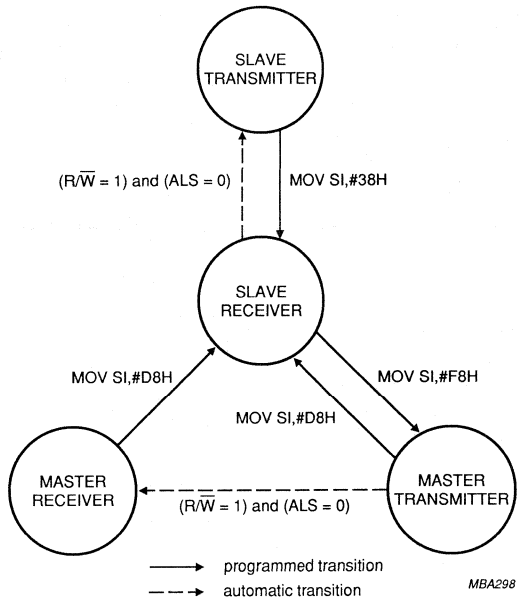


Fig.15 State diagram of the serial I/O interface.

4.11.4.2 Pending interrupt not bit (PIN)

If either MST or ALS is set, PIN is reset to zero (activated) after every byte transfer. If MST and ALS are both reset, PIN becomes zero (generating a serial interrupt request) when the valid address is detected and after each byte of the following transfer. Clock synchronization is implemented as follows: the SCL line is pulled to V_{SS} as long as PIN is zero enabling a slave to delay a master in order to read the data register (in the case of a slave receiver) or to write to the data register (in the case of a slave transmitter). PIN is automatically deactivated when S0 is accessed; it may also be deactivated by explicitly setting PIN to logic 1.

If the SIO/derivative interrupt is disabled, the serial I/O interface may be serviced by testing PIN directly in user software.

4.11.4.3 Bus busy bit (BB)

The status of the BB bit is controlled by the serial I/O interface or by bus master software. When a master clears BB (MOV S1,D8H), the serial I/O interface automatically clears MST and TRX, returning to the slave receiver mode (see Fig.15). If BB is set, write access to S1 other than accesses by the master or an addressed slave are inhibited. If BB is inadvertently set by excessive noise on the bus, the deadlock can be resolved by executing two consecutive MOV S1,18H instructions, the first of which just clears BB.

When a slave transmitter detects an end of transmission (signalled by the absence of an acknowledgment from the master receiver), it has to access S1 to inactivate PIN and become a slave receiver. However, BB should remain set. This is reflected by the MOV S1,38H instruction in Fig.15. When PIN = logic 1, clock synchronization terminates, enabling the master to generate the STOP condition.

A START condition must only be generated when BB = logic 0. Otherwise, the serial I/O interface responds as if bus arbitration had been lost.

4.11.4.4 Arbitration lost bit (AL)

The AL bit is set by the serial I/O interface when it loses bus arbitration in the master transmitter mode. Simultaneously, MST and TRX are cleared to enable the interface (now in the slave receiver mode) to determine if it is validly addressed by the device that won the arbitration. PIN is activated when the byte transfer is complete. AL will be cleared when the serial interrupt is terminated.

4.11.4.5 Addressed as slave bit (AAS)

AAS is set by the serial I/O interface following a START condition when the valid address is detected (ALS = logic 0 in register S0') or when the first byte is received (ALS = logic 1 in register S0'). AAS is cleared when the serial interrupt is terminated.

4.11.4.6 Address zero bit (AD0)

AD0 is set by the serial I/O interface independently of ALS when the 'general call' address (00H) is detected following a START condition. AD0 is cleared after a repeated START or a STOP condition.

4.11.4.7 Last received bit (LRB)

LRB contains the last bit transferred. If ACK = logic 1, LRB contains the acknowledgement bit. It remains valid as long as PIN = logic 0.

4.11.4.8 Enable serial I/O bit (ESO)

The ESO bit enables/disables the serial I/O interface. When ESO = logic 0, access to register S0' is enabled, the SCL pin is in a high impedance state and the P2.3/SDA pin is made available as a normal I/O port line.

When ESO = logic 1, the serial I/O interface is enabled and access to register S0 is possible. The remaining S1 bits can only be altered when ESO is set. The SCL and P2.3/SDA pins are enabled as serial clock and data lines respectively.

To avoid bus deadlock, ESO must be reset before a STOP instruction is executed.

4.11.4.9 Bit counter bits (BC0, BC1 and BC2)

BC0, BC1 and BC2 should all be zero for normal I^2C-bus operation. The bit counter is always cleared by a START condition; thus all eight bits of the first byte are transferred.

If a non-zero bit counter value is chosen, it is only valid for one S0 transfer since the counter decrements to zero. The bit counter is useful when a master receiver signals an end of transmission by sending a negative acknowledge after the last byte received; the last byte is received with ACK = logic 0 in register S2. The negative acknowledge is then issued by setting the bit counter to one and 'receiving' one bit from the HIGH level on the SDA line. The slave transmitter interprets the same signals as a negative acknowledgement.

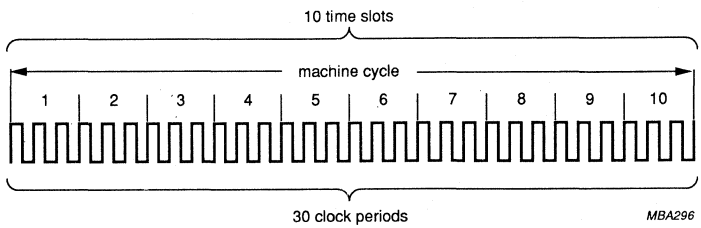


Fig.16 Machine cycle timing.

4.12 Timing

Every machine cycle consists of 10 time slots. Each time slot consists of 3 clock periods (see Fig.16).

The clock frequencies range is from 100 kHz to a maximum which is a function of supply voltage. When $V_{DD} \geq 4.5$ V, operation at 10 MHz is guaranteed.

The clock signal may be internally generated by the on-chip oscillator and an external crystal. Alternatively, an external clock may be applied to the XTAL1 pin.

4.13 Oscillator

The on-chip oscillator consists of an invertor stage including a feedback resistor and load capacitors (see Fig.17). A quartz crystal is usually connected between XTAL1 and XTAL2. Alternatively, a ceramic resonator or an inductor may be used as the timing element; however, external load capacitors should then be added for good frequency stability.

When the supply voltage drops below the power-on-reset level, the oscillator is inhibited. The internal oscillator may also be inhibited by the STOP instruction.

Oscillator start-up time depends on the external timing element. The start-up time of a quartz crystal is several milliseconds due to the narrow crystal bandwidth.

For proper oscillator start-up, the transconductance (gm) of the invertor stage must satisfy the following relationship (see Fig.17 and Fig.18):

$$4.2[R_1\omega^2(C_L + C_0 + C_f)^2 + 1/R_f] < gm < C_1C_2/[R_1(C_0 + C_f)^2 + 1/\omega^2R_f]$$

where:

R_1 = resonator series resistance
C_0 = static resonator capacitance
R_f = feedback resistor
C_L = $C_1C_2/[C_1 + C_2]$
C_f = parasitic feedback capacitance (typically 2 pF on-chip, external value depends on PC board wiring)
ω = $2\pi f_{XTAL}$

For more information on crystal oscillators and start-up conditions see the application note 'Crystal Oscillators for CMOS Circuits'.

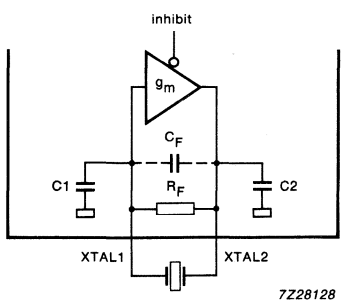


Fig.17 Oscillator with integrated elements.

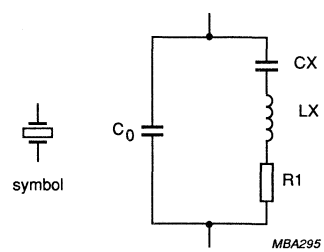


Fig.18 Crystal unit equivalent circuit.

4.14 Reset

After a falling edge on the internal reset, 1866 clock cycles are required to initialize the microcontroller to a defined state. The first instruction is then executed.

4.14.1 Passive reset

A passive reset is generated by the RC circuit shown in Fig.19. As V_{DD} rises, the discharged C_{reset} pulls the RESET pin close to V_{DD}. When V_{DD} crosses the power-on reference level V_{ref} (typically 1.5 V), the device generates a reset pulse of approximately 50 µs which helps to pull the RESET pin to V_{DD}. To ensure a correct reset, the RESET voltage should reach at least 70% of the final value of V_{DD} before C_{reset} charges through TR2 and R_{reset}. If the RESET voltage and V_{DD} rise exponentially, this requirement is satisfied when the time constant τ ($C_{reset}R_{reset}$) of the RESET pulse is greater than eight times the time constant of V_{DD}. If V_{DD} rises linearly, the requirement is satisfied when the time constant of the RESET pulse is greater than twice the time constant of V_{DD}.

In the event of a drop in the supply voltage, the diode rapidly discharges C_{reset}, ensuring reliable power-on-reset even after short supply voltage interruptions.

In battery-powered systems where V_{DD} quickly reaches its minimum operating value, passive reset can be performed without external components since the 50 µs reset pulse guarantees proper initialization.

4.14.2 Active reset

An active reset can be generated by driving the RESET pin HIGH with external logic. This pulse should be present until V_{DD} has reached its minimum operating value.

4.14.3 Reset state

After a reset, the microcontroller is initialized as follows:

The program counter points to 00H. Memory bank 0, register bank 0, and stack pointer 0 (locations 8 and 9) are selected. All interrupts are disabled. The timer/event counter is stopped and cleared, the timer flag is cleared, and the timer prescaler is set to modulo 32 (PS = 0). All port flip-flops (except P2.3/SDA) are set to logic 1. P2.3/SDA and SCL are high impedance 30 clock pulses (max.) after the end of the internal reset pulse. The serial I/O interface is disabled (ESO = 0) and in the slave receiver mode 30 clock pulses (max.) after the end of internal reset pulse (S0, S0', S1 and S2 are cleared except when PIN = logic 1). The Idle and Stop modes are terminated.

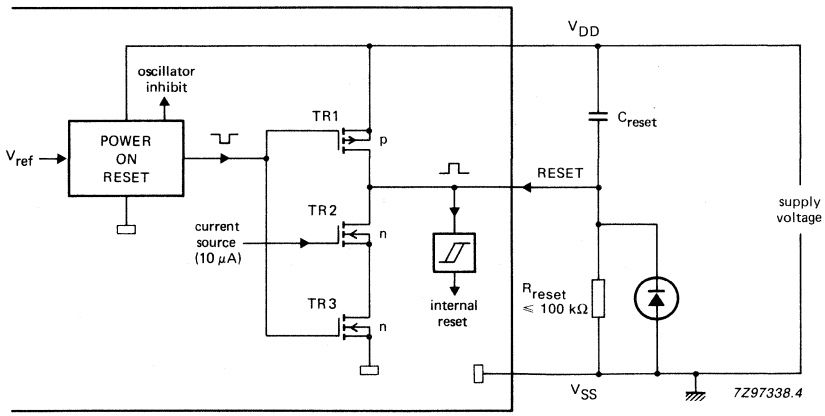


Fig.19 Passive power-on-reset.

4.15 Idle mode

The Idle mode is very useful in low power applications. When all computational tasks are completed, the device can be placed in the Idle mode instead of a power consuming waiting loop.

When the microcontroller enters the Idle mode by executing an IDLE instruction, all activity is halted except for the oscillator, the timer/event counter and the serial I/O interface (if available).

The Idle mode is terminated when an enabled interrupt (or reset) occurs. The interrupt routine is executed and program execution resumes at the instruction immediately following the IDLE instruction.

For timer/event counter interrupts and SIO/derivative interrupts, termination of the Idle mode is straightforward. However, care must be taken when the Idle mode is terminated by the external interrupt since $\overline{INT}$/T0 is negative-edge triggered. If $\overline{INT}$/T0 was LOW prior to entering the Idle mode, it must go HIGH before a negative edge can be generated. Fig.20 shows the exact timing for Idle mode termination with an external interrupt $\overline{INT}$/T0.

If no interrupt is enabled, the Idle mode can only be terminated by an active signal on the RESET pin. A normal reset sequence is executed (Fig.20).

4.16 Stop mode

The Stop mode enables very low power operation. When all computational tasks are completed, the device can be virtually shut down by stopping the oscillator.

When the microcontroller enters the Stop mode by executing a STOP instruction, the oscillator is switched off. All internal states (CPU status, RAM) and I/O levels are maintained.

The Stop mode is terminated by a LOW level on the $\overline{INT}$/T0 pin or a reset. In the latter case, a normal reset sequence is executed (see Fig.21).

Unlike the Idle mode, the microcontroller responds to a LOW level on the $\overline{INT}$/T0 pin (i.e. not to a negative edge). If the $\overline{INT}$/T0 pin is LOW when the STOP instruction is executed, the Stop mode will not be entered.

A negative edge on $\overline{INT}$/T0 causes program execution to continue after a delay of 1866 clock cycles. If the external interrupt is enabled, the microcontroller executes the instruction immediately following the STOP instruction before executing the interrupt routine. If the external interrupt is disabled, program execution continues with the instruction following the STOP instruction (see Fig.21).

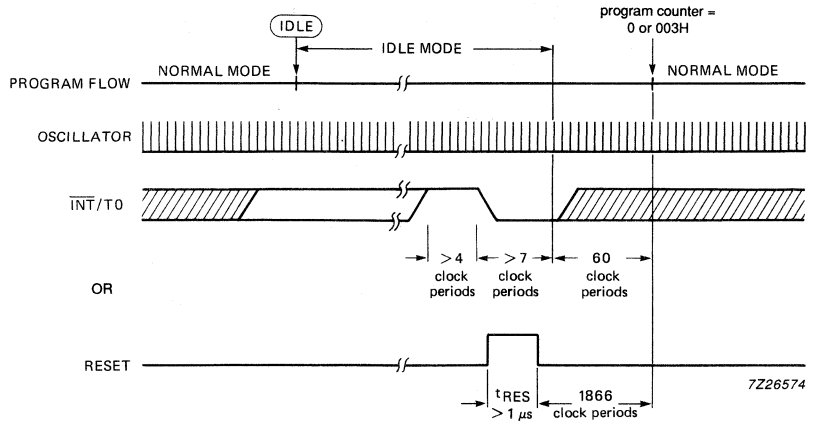


Fig.20 Entering and leaving the Idle mode.

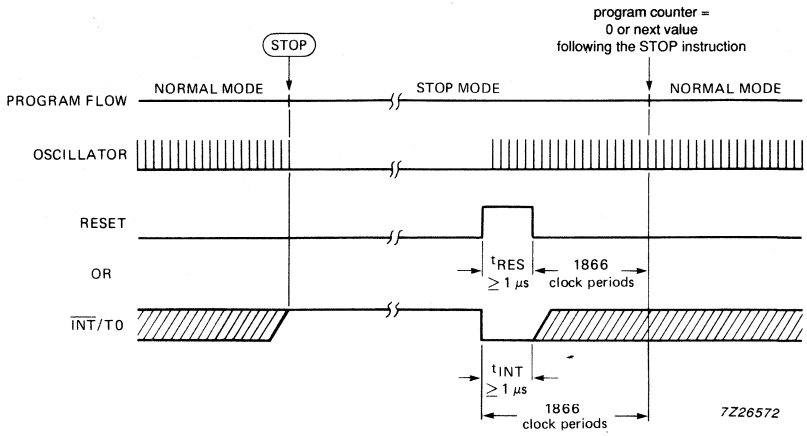


Fig.21 Entering and leaving the Stop mode.

4.17 Derivative logic

Several members of the PCF84CXXX family contain derivative logic. For specific information on a particular device, refer to the relevant data sheet.

The derivative registers are write only, read only or read/write (see Fig.22). They may be accessed internally via the derivative address register using the derivative input/output instructions (MOV A,Dx, MOV Dx,A, ANL Dx,A and ORL Dx,A).

Derivative interrupts share the PIN flag with the SIO interrupt (if available). When the derivative interrupt routine is executed, the PIN flag must be deactivated by software.

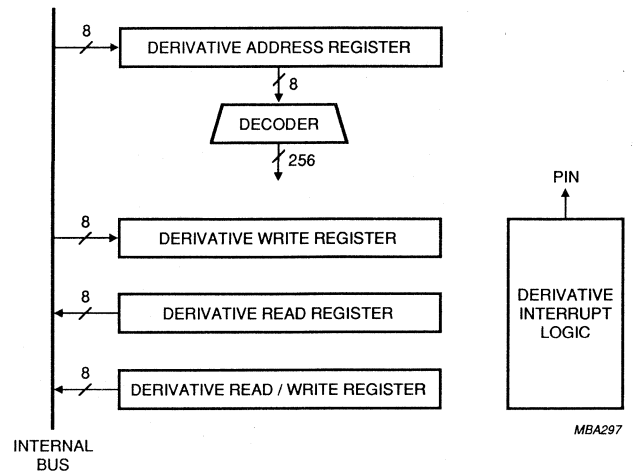


Fig.22 Block diagram of derivative logic.

5 INSTRUCTION SET

The PCF84CXXX family instruction set consists of over 80 one and two byte instructions. Program code efficiency is high because all RAM locations and all ROM locations on a 256 byte page require only a single byte address.

Table 8 contains the instruction set of the PCF84CXXX. Figure 23 shows the instruction map and Table 7 describes the symbols that are used.

Table 7 Symbols and definitions.

SYMBOL	DESCRIPTION
A	accumulator
addr	program memory address
Bb	bit designation (b = 0 to 7)
C	carry bit (bit CY)
CNT	event counter
Dx	mnemonic derivative register (x = 0 to 255)
direct	8-bit derivative register address
data	8-bit immediate data
I	interrupt
MBn	memory bank (n = 0 to 3)
MBFFn	memory bank flip-flop (n = 0 or 1)
P	mnemonic for 'in-page' operation
PC	program counter
Pp	port designation (p = 0, 1, or 2)
PS	Timer prescaler select
PSW	program status word
RB	register bank
RBS	register bank select flag
@Rr	8-bit address register (r = 0, 1)
Rr	8-bit register (r = 0 to 7)
Sn	serial I/O register (n = 0, 1, or 2)
SP	stack pointer
T	timer
TCNT	timer/event counter
TF	timer flag
T0, T1	test 0 and test 1 inputs
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with
< >	represents a hex digit

PCF84CXXX PCD33XX

first hexadecimal character of opcode

second hexadecimal character of opcode

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A, #data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp 0	IN A,Pp 1	IN A,Pp 2		MOV A,Sn 0	MOV A,Sn 1		
1	INC @ Rr 0	INC @ Rr 1	JB0 addr	ADDC A,#data	CALL page 0	DIS I	JTF addr	INC A	INC Rr 0	INC Rr 1	INC Rr 2	INC Rr 3	INC Rr 4	INC Rr 5	INC Rr 6	INC Rr 7
2	XCH A, @Rr 0	XCH A, @Rr 1	STOP	MOV A, #data	JMP page 1	EN TCNTI	JNT0 addr	CLR A	XCH A,Rr 0	XCH A,Rr 1	XCH A,Rr 2	XCH A,Rr 3	XCH A,Rr 4	XCH A,Rr 5	XCH A,Rr 6	XCH A,Rr 7
3	XCHD A, @Rr 0	XCHD A, @Rr 1	JB1 addr		CALL page 1	DIS TCNTI	JT0 addr	CPL A	OUTL Pp,A 0	OUTL Pp,A 1	OUTL Pp,A 2		MOV Sn,A 0	MOV Sn,A 1	MOV Sn,A 2	
4	ORL A, @Rr 0	ORL A, @Rr 1	MOV A, T	ORL A, #data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr 0	ORL A,Rr 1	ORL A,Rr 2	ORL A,Rr 3	ORL A,Rr 4	ORL A,Rr 5	ORL A,Rr 6	ORL A,Rr 7
5	ANL A, @Rr 0	ANL A, @Rr 1	JB2 addr	ANL A, #data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr 0	ANL A,Rr 1	ANL A,Rr 2	ANL A,Rr 3	ANL A,Rr 4	ANL A,Rr 5	ANL A,Rr 6	ANL A,Rr 7
6	ADD A, @Rr 0	ADD A, @Rr 1	MOV T, A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr 0	ADD A,Rr 1	ADD A,Rr 2	ADD A,Rr 3	ADD A,Rr 4	ADD A,Rr 5	ADD A,Rr 6	ADD A,Rr 7
7	ADDC A, @Rr 0	ADDC A, @Rr 1	JB3 addr		CALL page 3			RR A	ADDC A,Rr 0	ADDC A,Rr 1	ADDC A,Rr 2	ADDC A,Rr 3	ADDC A,Rr 4	ADDC A,Rr 5	ADDC A,Rr 6	ADDC A,Rr 7
8				RET	JMP page 4	EN SI			ORL Pp,#data 0	ORL Pp,#data 1	ORL Pp,#data 2		MOV A,Dx	MOV Dx,A	ANL Dx,A	ORL Dx,A
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,#data 0	ANL Pp,#data 1	ANL Pp,#data 2		MOV Sn,#data 0	MOV Sn,#data 1	MOV Sn,#data 2	
A	MOV @ Rr,A 0	MOV @ Rr,A 1		MOVP A,@A	JMP page 5	SEL MB2		CPL C	MOV Rr,A 0	MOV Rr,A 1	MOV Rr,A 2	MOV Rr,A 3	MOV Rr,A 4	MOV Rr,A 5	MOV Rr,A 6	MOV Rr,A 7
B	MOV @Rr, #data 0	MOV @Rr, #data 1	JB5 addr	JMPP @A	CALL page 5	SEL MB3			MOV Rr,#data 0	MOV Rr,#data 1	MOV Rr,#data 2	MOV Rr,#data 3	MOV Rr,#data 4	MOV Rr,#data 5	MOV Rr,#data 6	MOV Rr,#data 7
C	DEC @Rr 0	DEC @Rr 1			JMP page 6	SEL RB0	JZ addr	MOV A,PSW	DEC Rr 0	DEC Rr 1	DEC Rr 2	DEC Rr 3	DEC Rr 4	DEC Rr 5	DEC Rr 6	DEC Rr 7
D	XRL A, @Rr 0	XRL A, @Rr 1	JB6 addr	XRL A,#data	CALL page 6	SEL RB1		MOV PSW,A	XRL A,Rr 0	XRL A,Rr 1	XRL A,Rr 2	XRL A,Rr 3	XRL A,Rr 4	XRL A,Rr 5	XRL A,Rr 6	XRL A,Rr 7
E	DJNZ @ Rr,addr 0	DJNZ @ Rr,addr 1			JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr,addr 0	DJNZ Rr,addr 1	DJNZ Rr,addr 2	DJNZ Rr,addr 3	DJNZ Rr,addr 4	DJNZ Rr,addr 5	DJNZ Rr,addr 6	DJNZ Rr,addr 7
F	MOV A, @Rr 0	MOV A, @Rr 1	JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr 0	MOV A,Rr 1	MOV A,Rr 2	MOV A,Rr 3	MOV A,Rr 4	MOV A,Rr 5	MOV A,Rr 6	MOV A,Rr 7

MBA281

Fig.23 PCF84CXXX instruction map.

Table 8 PCF84CXXX family instruction set.

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION		NOTES
ACCUMULATOR						
ADD A, Rr	6<8 + r>	1/1	Add register contents to A	(A) ← (A) + (Rr)	r = 0 to 7	1
ADD A, @Rr	6r	1/1	Add RAM data, addressed by Rr, to A	(A) ← (A) + ((Rr))	r = 0, 1	1
ADD A, #data	03 data	2/2	Add immediate data to A	(A) ← (A) + data		1
ADDC A, Rr	7<8 + r>	1/1	Add carry and register contents to A	(A) ← (A) + (Rr) + (C)	r = 0 to 7	1
ADDC A, @Rr	7r	1/1	Add carry and RAM data, addressed by Rr, to A	(A) ← (A) + ((Rr)) + (C)	r = 0, 1	1
ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A) ← (A) + data + (C)		1
ANL A, Rr	5<8 + r>	1/1	'AND' Rr with A	(A) ← (A) AND (Rr)	r = 0 to 7	
ANL A, @Rr	5r	1/1	'AND' RAM data, addressed by Rr, with A	(A) ← (A) AND ((Rr))	r = 0, 1	
ANL A, #data	53 data	2/2	'AND' immediate data with A	(A) ← (A) AND data		
ORL A, Rr	4<8 + r>	1/1	'OR' Rr with A	(A) ← (A) OR (Rr)	r = 0 to 7	
ORL A, @Rr	4r	1/1	'OR' RAM data, addressed by Rr, with A	(A) ← (A) OR ((Rr))	r = 0, 1	
ORL A, #data	43 data	2/2	'OR' immediate data with A	(A) ← (A) OR data		
XRL A, Rr	D<8 + r>	1/1	'XOR' Rr with A	(A) ← (A) XOR (Rr)	r = 0 to 7	
XRL A, @Rr	Dr	1/1	'XOR' RAM data, addressed by Rr, with A	(A) ← (A) XOR ((Rr))	r = 0, 1	
XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A) ← (A) XOR data		
INC A	17	1/1	Increment A by 1	(A) ← (A) + 1		
DEC A	07	1/1	Decrement A by 1	(A) ← (A) − 1		
CLR A	27	1/1	Clear A to zero	(A) ← 0		
CPL A	37	1/1	One's complement A	(A) ← NOT(A)		
RL A	E7	1/1	Rotate A left	$(A_{n+1}) \leftarrow (A_n)$ $(A_0) \leftarrow (A_7)$	n = 0 to 6	
RLC A	F7	1/1	Rotate A left through carry	$(A_{n+1}) \leftarrow A_n$ $(A_0) \leftarrow (C), (C) \leftarrow (A_7)$	n = 0 to 6	2
RR A	77	1/1	Rotate A right	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (A_0)$	n = 0 to 6	
RRC A	67	1/1	Rotate A right through carry	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (C), (C) \leftarrow (A_0)$	n = 0 to 6	2
DA A	57	1/1	Decimal adjust A	(A) ← (A) + 06H if AC = 1 or $(A_{0-3}) > 9$; (A) ← (A) + 60H if $(A_{4-7}) > 9$		2
SWAP A	47	1/1	Swap nibbles of A	$(A_{4-7}) \leftrightarrow (A_{0-3})$		2

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION		NOTES
DATA MOVES						
MOV A, Rr	F<8 + r>	1/1	Move register contents to A	(A) ← (Rr)	r = 0 to 7	
MOV A, @Rr	Fr	1/1	Move RAM data, addressed by Rr, to A	(A) ← ((Rr))	r = 0, 1	
MOV A, #data	23 data	2/2	Move immediate data to A	(A) ← data		
MOV Rr, A	A<8 + r>	1/1	Move accumulator contents to register	(Rr) ← (A)	r = 0 to 7	
MOV @Rr, A	Ar	1/1	Move accumulator contents to RAM location addressed by Rr	((Rr)) ← (A)	r = 0, 1	
MOV Rr, #data	B<8 + r> data	2/2	Move immediate data to Rr	(Rr) ← data	r = 0 to 7	
MOV @Rr, #data	Br data	2/2	Move immediate data to RAM location addressed by Rr	((R0)) ← data	r = 0, 1	
XCH A, Rr	2<8 + r>	1/1	Exchange accumulator contents with Rr	(A) ↔ (Rr)	r = 0 to 7	
XCH A, @Rr	2r	1/1	Exchange accumulator contents with RAM data addressed by Rr	(A) ↔ ((Rr))	r = 0, 1	
XCHD A, @Rr	3r	1/1	Exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3}) \leftrightarrow ((Rr_{0-3}))$	r = 0, 1	
MOV A, PSW	C7	1/1	Move PSW contents to accumulator	(A) ← (PSW)		
MOV PSW, A	D7	1/1	Move accumulator bit 3 to PSW_3 (PS)	(PS) ← (A_3)		3
MOVP A, @A	A3	1/2	Move indirectly addressed data in current page to A	(PC_{0-7}) ← (A), (A) ← ((PC))		
CARRY FLAG						
CLR C	97	1/1	Clear carry bit	(C) ← 0		2
CPL C	A7	1/1	Complement carry bit	(C) ← NOT(C)		2
REGISTER						
INC Rr	1<8 + r>	1/1	Increment register by 1	(Rr) ← (Rr) + 1	r = 0 to 7	
INC @Rr	1r	1/1	Increment RAM data, addressed by Rr, by 1	((Rr)) ← ((Rr)) + 1	r = 0, 1	
DEC Rr	C<8 + r>	1/1	Decrement register by 1	(Rr) ← (Rr) – 1	r = 0 to 7	
DEC @Rr	Cr	1/1	Decrement RAM data, addressed by Rr, by 1	((Rr)) ← ((Rr)) – 1	r = 0, 1	

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION		NOTES
BRANCH						
JMP addr	<2n>4 addr	2/2	Unconditional jump within a 2 K bank	(PC_{8-10}) ← n (PC_{0-7}) ← addr (PC_{11-12}) ← (MBFF 0-1)	n = 0 to 7	
JMPP @A	B3	1/2	Indirect jump within a page	(PC_{0-7}) ← ((A))		
DJZN Rr, addr	E<8 + r> addr	2/2	Decrement Rr by 1 and jump if not zero to addr	(Rr) ← (Rr) – 1; if (Rr) not zero, then (PC_{0-7}) ← addr	r = 0 to 7	
DJNZ @Rr, addr	Er	2/2	Decrement RAM data, addressed by Rr, by 1 and jump if not zero to addr	((Rr)) ← ((Rr)) – 1; if ((Rr)) not zero, then (PC_{0-7}) ← addr	r = 0, 1	
JBb addr	<2b + 1>2 addr	2/2	Jump to addr if Accumulator bit b = 1	If (A_b) = 1, then (PC_{0-7}) ← addr	b = 0 to 7	
JC addr	F6 addr	2/2	Jump to addr if C = 1	If (C) = 1, then (PC_{0-7}) ← addr		
JNC addr	E6 addr	2/2	Jump to addr if C = 0	If (C) = 0, then (PC_{0-7}) ← addr		
JZ addr	C6 addr	2/2	Jump to addr if A = 0	If (A) = 0, then (PC_{0-7}) ← addr		
JNZ addr	96 addr	2/2	Jump to addr if A is NOT zero	If (A) ≠ 0, then (PC_{0-7}) ← addr		
JTO addr	36 addr	2/2	Jump to addr if T0 = 1	If T0 = 1, then (PC_{0-7}) ← addr		
JNT0 addr	26 addr	2/2	Jump to addr if T0 = 0	If T0 = 0: (PC_{0-7}) ← addr		
JT1 addr	56 addr	2/2	Jump to addr if T1 = 1	If T1 = 1: (PC_{0-7}) ← addr		
JNT1 addr	46 addr	2/2	Jump to addr if T1 = 0	If T1 = 0: (PC_{0-7}) ← addr		
JTF addr	16 addr	2/2	Jump to addr if Timer Flag = 1	If TF = 1: (PC_{0-7}) ← addr		4
JNTF addr	06 addr	2/2	Jump to addr if Timer Flag = 0	If TF = 0: (PC_{0-7}) ← addr		4
TIMER/EVENT COUNTER						
MOV A, T	42	1/1	Move timer/event counter contents to accumulator	(A) ← (T)		
MOV T, A	62	1/1	Move accumulator contents to timer/event counter	(T) ← (A)		
STRT CNT	45	1/1	Start event counter			
STRT T	55	1/1	Start timer			
STOP TCNT	65	1/1	Stop timer/event counter			
EN TCNTI	25	1/1	Enable timer/event counter interrupt			
DIS TCNTI	35	1/1	Disable timer/event counter interrupt			
CONTROL						
EN I	05	1/1	Enable external interrupt			
DIS I	15	1/1	Disable external interrupt			
SEL RB0	C5	1/1	Select register bank 0	(RBS) ← 0		5
SEL RB1	D5	1/1	Select register bank 1	(RBS) ← 1		5
SEL MB0	E5	1/1	Select program memory bank 0	(MBFF0) ← 0, (MBFF1) ← 0		10
SEL MB1	F5	1/1	Select program memory bank 1	(MBFF0) ← 1, (MBFF1) ← 0		10
SEL MB2	A5	1/1	Select program memory bank 2	(MBFF0) ← 0, (MBFF1) ← 1		10
SEL MB3	B5	1/1	Select program memory bank 3	(MBFF0) ← 1, (MBFF1) ← 1		10
STOP	22	1/1	Enter Stop mode			
IDLE	01	1/1	Enter Idle mode			

MNEMONIC	OPCODE (HEX)	BYTES/ CYCLES	DESCRIPTION	FUNCTION		NOTES
SUBROUTINE						
CALL addr	<2n + 1>4 addr	2/2	Jump to subroutine	((SP)) ← (PC), ($PSW_{4, 6, 7}$) (SP) ← (SP) + 1 (PC_{8-10}) ← n (PC_{0-7}) ← addr (PC_{11-12}) ← (MBFF0-1)	n = 0 to 7	6
RET	83	1/2	Return from subroutine	(SP) ← (SP) - 1 (PC) ← ((SP))		6
RETR	93	1/2	Return from interrupt and restore bits 4, 6, 7 of PSW	(SP) ← (SP) - 1 ($PSW_{4, 6, 7}$) + (PC) ← ((SP))		6
PARALLEL INPUT/OUTPUT						
IN A, Pp	08 09 0A	1/2	Input port p data to accumulator	(A) ← (P0) (A) ← (P1) (A) ← (P2)		7
OUTL Pp, A	38 39 3A	1/2	Output accumulator data to port p	(P0) ← (A) (P1) ← (A) (P2) ← (A)		
ANL Pp, #data	98 data 99 data 9A data	2/2	AND port p with immediate data	(P0) ← (P0) AND data (P1) ← (P1) AND data (P2) ← (P2) AND data		
ORL Pp, #data	88 data 89 data 8A data	2/2	OR port p data with immediate data	(P0) ← (P0) OR data (P1) ← (P1) OR data (P2) ← (P2) OR data		
DERIVATIVE INPUT/OUTPUT						
MOV A, Dx	8C direct	2/2	Move derivative register contents to accumulator	(A) ← (Dx)	x = 0 to 255	8
MOV Dx, A	8D direct	2/2	Move accumulator contents to derivative register	(Dx) ← (A)	x = 0 to 255	8
ANL Dx, A	8E direct	2/2	AND derivative register with accumulator	(Dx) ← (Dx) AND (A)	x = 0 to 255	8
ORL Dx, A	8F direct	2/2	OR derivative register with accumulator	(Dx) ← (Dx) OR (A)	x = 0 to 255	8
SERIAL INPUT/OUTPUT						
MOV A, S_n	0C 0D	1/2	Move serial I/O register contents to accumulator	(A) ← (S0) (A) ← (S1)	n = 0, 1	
MOV S_n, A	3C 3D 3E	1/2	Move accumulator contents to serial I/O register	(S0) ← (A) (S1) ← (A) (S2) ← (A)	n = 0, 1, 2	
MOV S_n, #data	9C data 9D data 9E data	2/2	Move immediate data to serial I/O register	(S0) ← data (S1) ← data (S2) ← data	n = 0, 1, 2	
EN SI	85	1/1	Enable serial I/O interrupt			
DIS SI	95	1/1	Disable serial I/O interrupt			
NOP	00	1/1	No operation	(PC_{0-10}) ← (PC_{0-10}) + 1		

Notes

1. PSW CY, AC affected.
2. PSW CY affected.
3. PSW PS affected.
4. Execution of a JTF or JNTF instruction resets the Timer Flag (TF).
5. PSW RBS affected.
6. PSW SP_0, SP_1, SP_2 affected.
7. (A) = 0000, P2.3, P2.2, P2.1, P2.0
8. For more information on the derivative input/output instructions of a particular microcontroller, consult the specific microcontroller data sheet.
9. (S1) has a different meaning for read and write operations. See section 4.11.4.
10. SEL MB instructions may not be used within interrupt routines.

6 LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Supply voltage range	−0.8	8.0	V
V_I	All input voltages	−0.5	V_{DD} + 0.5	V
I_I, I_O	DC current into any input or output	-	10	mA
P_{tot}	Total power dissipation	-	125	mW
T_{stg}	Storage temperature range	−65	150	°C
T_{amb}	Operating ambient temperature range (if $P_{tot} \leq 100$ mW)	−40	70	°C
T_{amb}	Operating ambient temperature range (if $P_{tot} \leq 30$ mW)	−40	85	°C
T_j	Operating junction temperature	-	90	°C

7 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

8 DC CHARACTERISTICS

V_{DD} = 2.5 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to 85 °C; all voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	Operating supply voltage range	See Fig.24.	2.5	-	5.5	V
I_{DD}	Operating supply current	See Fig.26, Fig.27, and note 1; at V_{DD} = 5 V; f_{XTAL} = 10 MHz at V_{DD} = 5 V; f_{XTAL} = 6 MHz at V_{DD} = 3 V; f_{XTAL} = 3.58 MHz	- - -	1.6 1.0 0.3	3.2 2.0 0.8	mA mA mA
I_{DD}	Idle mode supply current	See Fig.28, Fig.29, and note 1; at V_{DD} = 5 V; f_{XTAL} = 10 MHz at V_{DD} = 5 V; f_{XTAL} = 6 MHz at V_{DD} = 3 V; f_{XTAL} = 3.58 MHz	- - -	0.8 0.5 0.15	1.6 1.0 0.4	mA mA mA
IDD	Stop mode supply current	See Fig.25, note 1, and note 2; at V_{DD} = 2.5 V; T_{amb} = 25 °C at V_{DD} = 2.5 V; T_{amb} = 85 °C	- -	1.2 -	2.5 10.0	µA µA
Inputs						
V_{IL}	Input voltage LOW		0	-	$0.3V_{DD}$	V
V_{IH}	Input voltage HIGH		$0.7V_{DD}$	-	V_{DD}	V
$\pm I_{IL}$	Input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	-	-	1	µA
Outputs						
I_{OL}	Output sink current	All outputs except SCL, P2.3/SDA; see Fig.30. at V_{DD} = 5 V ± 10%; V_O = 0.4 V	1.6	3.0	-	mA
I_{OL}	Output sink current	SCL, P2.3/SDA; see Fig.31. at V_{DD} = 5 V ± 10%; V_O = 0.4 V	3.0	5.5	-	mA
$-I_{OH}$	Output source current	See Fig.32. at V_{DD} = 5 V ± 10%; V_O = $0.7V_{DD}$ at V_{DD} = 5 V ± 10%; V_O = V_{SS}	40 -	- -	- 400	µA µA
$-I_{OH}$	Output source current	See Fig.33. at V_{DD} = 5 V ± 10%; V_O = V_{DD} − 0.4 V	1.6	3.0	-	mA

9 AC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to 85 °C. All voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	Rise time all outputs	See note 3.	-	30	-	ns
t_f	Fall time all outputs	See note 3.	-	30	-	ns
f_{XTAL}	Clock frequency	See Fig.24.	0.45	-	10.0	MHz

10 SERIAL I/O INTERFACE CHARACTERISTICS

See Fig.34, Fig.35 and note 4.

SYMBOL	PARAMETER	CONDITIONS	SCL INPUT	SCL OUTPUT
$t_{HD;STA}$	START condition hold time		$\geq 14/f_{XTAL}$	$(DF+9)/(2f_{XTAL})$
t_{LOW}	SCL LOW time	Note 5.	$\geq 17/f_{XTAL}$	$(DF-3)/(2f_{XTAL})$
t_{HIGH}	SCL HIGH time	Note 5.	$\geq 17/f_{XTAL}$	$(DF+3)/(2f_{XTAL})$
t_{RC}	SCL rise time	Note 6.	≤ 1 µs	≤ 1 µs
t_{FC}	SCL fall time	Note 7.	≤ 0.3 µs	≤ 0.1 µs
SYMBOL	**PARAMETER**	**CONDITIONS**	**P2.3/SDA INPUT**	**P2.3/SDA OUTPUT**
t_{BUF}	Bus free time	Note 8.	$\geq 14/f_{XTAL}$	≥ 4.7 µs
$t_{SU;DAT}$	Data set-up time	Note 9.	≥ 250 ns	$\geq 15/f_{XTAL}$
$t_{HD,DAT}$	Data hold time		> 0	$\geq 9/f_{XTAL}$
t_{RD}	SDA rise time	Note 6.	≤ 1 µs	≤ 1 µs
t_{FD}	SDA fall time	Note 7.	≤ 0.3 µs	≤ 0.1 µs
$t_{SU;STO}$	Stop condition set-up time		$\geq 14/f_{XTAL}$	$(DF-3)/(2f_{XTAL})$

Notes

1. $V_{IL} = 0$; $V_{IH} = V_{DD}$; open drain outputs connected to V_{SS}; all other outputs open.
2. Crystal connected between XTAL1 and XTAL2; pin T1 at V_{SS}; pin $\overline{INT}$/T0 at V_{DD}.
3. $V_{DD} = 5$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF.
4. DF is the f_{XTAL} divisor (see Table 2).
5. Values given for ASC = 0; for ASC = 1, $t_{LOW} = (DF-3)/4f_{XTAL}$, $t_{HIGH} = 3(DF+1)/4f_{XTAL}$.
6. Determined by the I^2C-bus capacitance (C_b) and the external pull-up resistor.
7. At maximum allowed I^2C-bus capacitance $C_b = 400$ pF.
8. Determined by program.
9. Independently of ASC, if $t_{LOW} \leq 24/f_{XTAL}$, $t_{SU;DAT} \geq t_{LOW} - 9/f_{XTAL}$.

11 CHARACTERISTIC CURVES

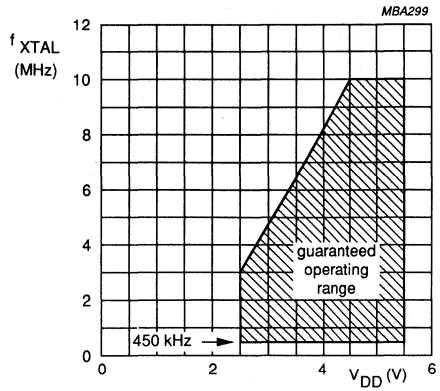
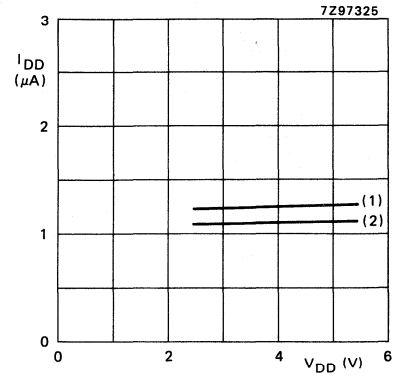
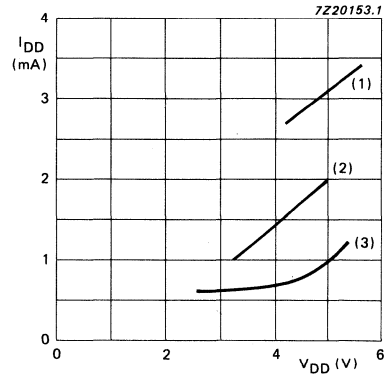


Fig.24 Maximum clock frequency (f_{XTAL}) as a function of supply voltage (V_{DD}).



(1) T_{amb} = 85 °C
(2) T_{amb} = 25 °C

Fig.25 Typical supply current (I_{DD}) in Stop mode as a function of supply voltage (V_{DD}).



(1) f_{XTAL} = 10.0 MHz
(2) f_{XTAL} = 6.0 MHz
(3) f_{XTAL} = 3.58 MHz

Fig.26 Maximum operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).

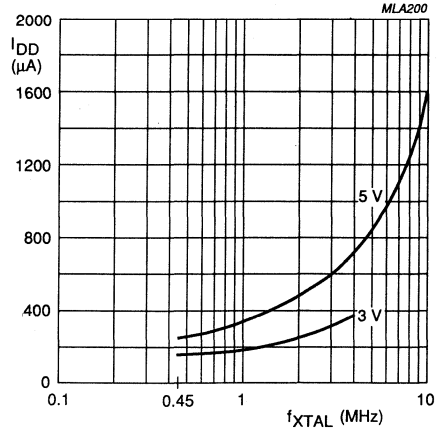
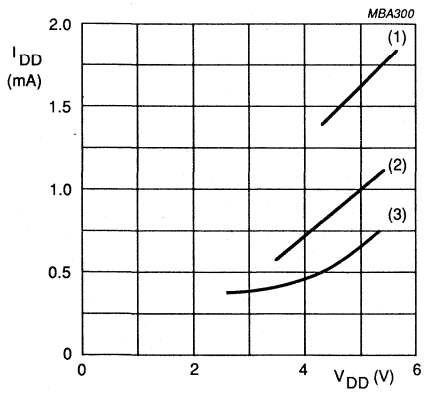


Fig.27 Typical operating supply current (I_{DD}) as a function of frequency at V_{DD} = 3 V and V_{DD} = 5 V.



(1) f_{XTAL} = 10.0 MHz
(2) f_{XTAL} = 6.0 MHz
(3) f_{XTAL} = 3.58 MHz

Fig.28 Maximum supply current (I_{DD}) in Idle mode as a function of supply voltage (V_{DD}).

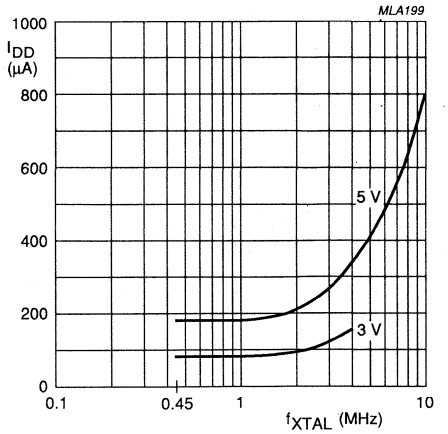


Fig.29 Typical supply current (I_{DD}) in Idle mode as a function of frequency at V_{DD} = 3 V and V_{DD} = 5 V.

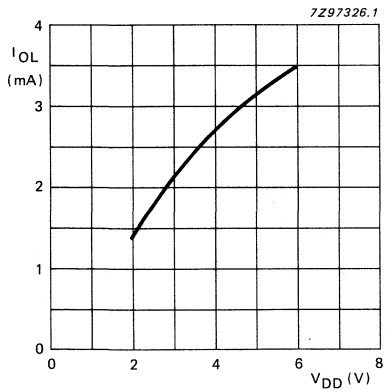


Fig.30 Typical output sink current (I_{OL}) as a function of supply voltage (V_{DD}); V_O = 0.4 V.

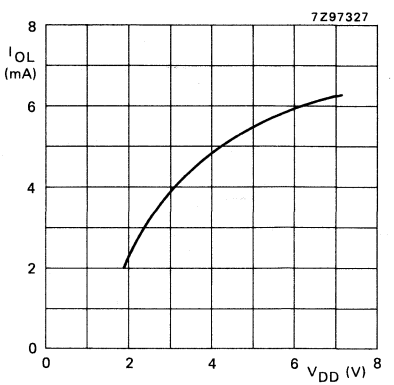
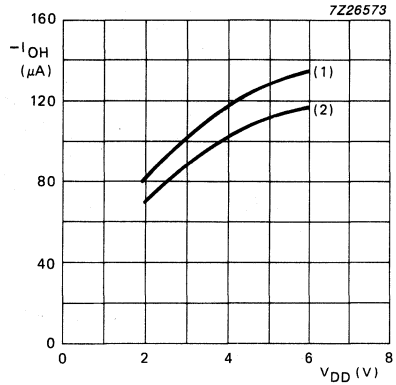


Fig.31 Typical output sink current (I_{OL}), outputs P2.3/SDA and SCL as a function of supply voltage (V_{DD}); V_O = 0.4 V.



(1) $V_O = V_{SS}$
(2) $V_O = 0.7V_{DD}$

Fig.32 Typical output source current ($-I_{OH}$) as a function of supply voltage (V_{DD}).

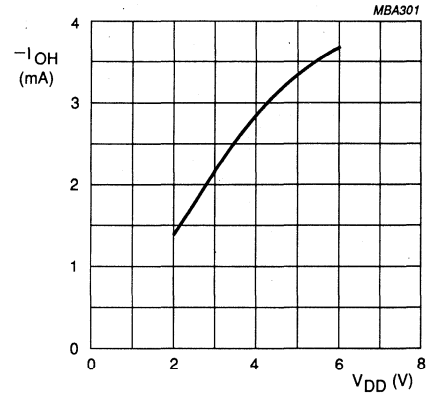


Fig.33 Typical push-pull output source current ($-I_{OH}$) as a function of supply voltage (V_{DD}); $V_O = V_{DD} - 0.4$ V.

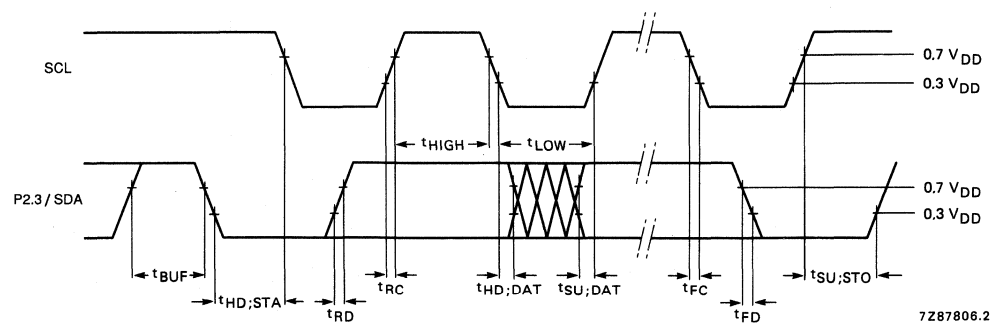


Fig.34 Slave SCL and receiver P2.3/SDA timing (SCL and P2.3/SDA input).

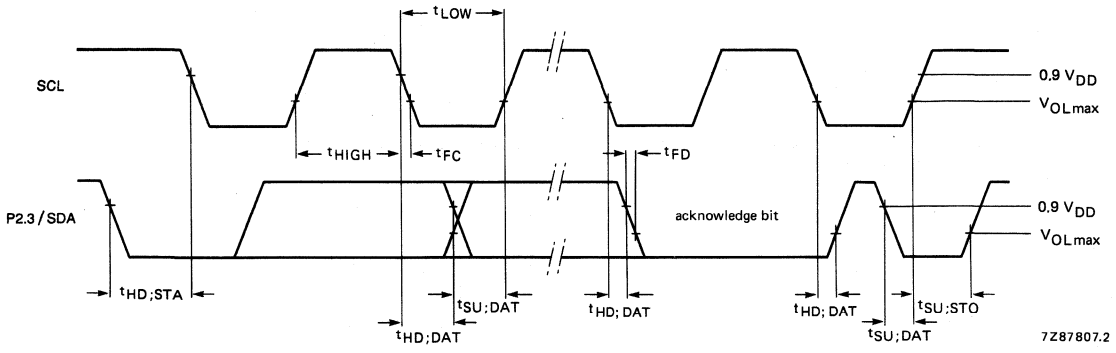


Fig.35 Master SCL and transmitter P2.3/SDA timing (SCL and P2.3/SDA output).

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLERS WITH I²C-BUS INTERFACE

DESCRIPTION

An advanced CMOS process is used to manufacture the PCF84C00, PCF84C21/C, PCF84C41/C and PCF84C81/C microcontrollers. The PCF84C21C, PCF84C41C and PCF84C81C operate at a higher clock frequency. Each device has 20 quasi-bidirectional I/O port lines, a serial I/O interface, a single-level vectored interrupt structure, an 8-bit timer/event counter and on-chip clock oscillator and clock circuits. On-chip RAM and ROM content is as follows:

- PCF84C00 – 256 x 8 RAM, external program memory
- PCF84C21 – 64 x 8 RAM, 2 K x 8 ROM
- PCF84C41 – 128 x 8 RAM, 4 K x 8 ROM
- PCF84C81 – 256 x 8 RAM, 8 K x 8 ROM

These efficient controllers also perform well as arithmetic processors. They have facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set is similar to that of the MAB8048.

These microcontrollers are members of the 84CXXX family. For detailed information, consult the 84CXXX family specification.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 2K, 4 K or 8 K x ROM; also a ROM-less version
- 64, 128 or 256 x 8 RAM
- 20 quasi-bidirectional I/O port lines
- Two test inputs, one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter and serial I/O
- I²C hardware interface for serial data transfer on two lines (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency range: 100 kHz to 10 MHz ; C versions: 1 MHz to 12 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage (2,5 to 5,5 V)
- STOP and IDLE modes
- Power-on reset circuit
- Operating temperature range: −40 to +85 °C
- High current on Port 1: I_{OL} = 10 mA at V_{OL} = 1,2 V (all versions except the PCF84C00).

For following sections see 84CXXX family specification

Program memory
Data memory
Program counter stack
IDLE and STOP modes
I/O facilities
Serial I/O
Interrupts
Oscillator
Timer/event counter
Program status word

Program counter
Central processing unit
Conditional branch logic
Test input T1

Power-on reset
Instruction set

PACKAGE OUTLINES

PCF84C21/41/81P: 28-lead DIL; plastic (SOT117).
PCF84C21/41/81T: 28-lead mini-pack; plastic (SO28; SOT136A).
PCF84C00B : 28-lead 'piggy-back' package (supports up to 28-pin EPROM).
PCF84C00T : 56-lead mini-pack; plastic (VSO56; SOT190).

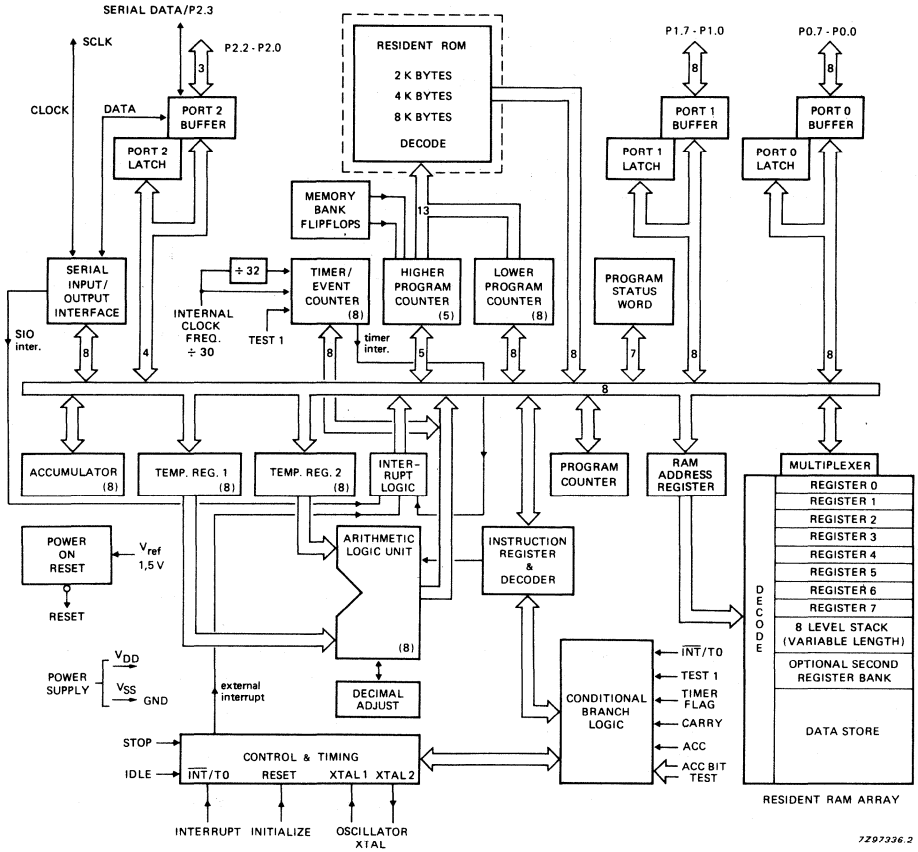


Fig. 1 Block diagram.

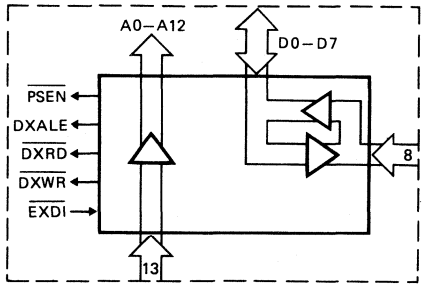


Fig. 1a Replacement of dotted section in Fig. 1, for the PCF84C00T ROM-less version.

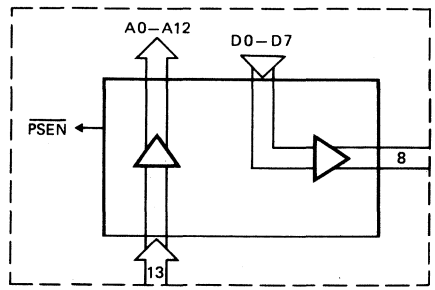


Fig. 1b Replacement of dotted section in Fig. 1, for the PCF84C00B 'piggy-back' version.

PINNING

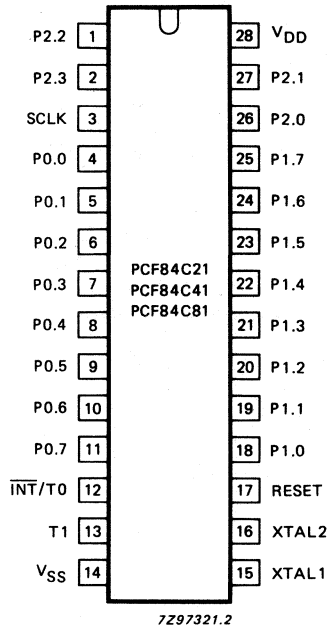


Fig. 2 Pinning diagram.

PIN DESIGNATION

Pin	*Symbol*	*Type*	*Function*
3	SCLK	I/O	**Clock:** bidirectional clock for serial I/O.
4-11	P0.0-P0.7	I/O	**Port 0:** 8-bit quasi-bidirectional I/O port.
12	$\overline{\text{INT}}$/T0	I	**Interrupt/Test 0:** external interrupt input (negative edge triggered)/ test input pin; when used as a test input, this pin is directly tested by conditional branch instructions JT0 and JNT0.
13	T1	I	**Test 1:** test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 may also be selected as an input to the 8-bit timer/event counter via the STRT CNT instruction.
14	V_{SS}	I	**Ground:** circuit earth potential.
15	XTAL 1	I	**Oscillator input:** input from a crystal which determines the internal oscillator frequency or an external clock generator.
16	XTAL 2	I/O	**Oscillator output:** output of the inverting amplifier.
17	RESET	I/O	**Reset input:** used to initialize the microcontroller (active HIGH); also output of power-on-reset circuit.
18-25	P1.0-P1.7	I/O	**Port 1:** 8-bit quasi-bidirectional I/O port.
26, 27, 1, 2	P2.0-P2.3	I/O	**Port 2:** 4-bit quasi-bidirectional I/O port. P2.3 is the serial data input/output in serial I/O mode.
28	V_{DD}	I	**Power supply:** 2,5 V to 5,5 V.

PINNING (continued)

Pin diagram of the PCF84C00B 'piggy-back' version

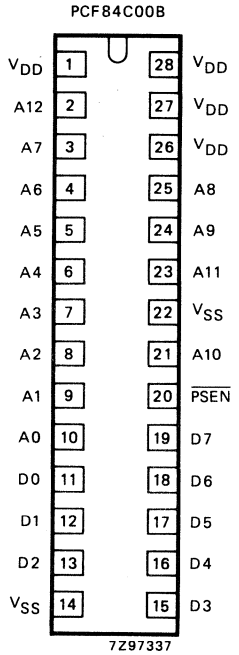


Fig. 3(a) Pinning diagram (top pins) of the PCF84C00B 'piggy-back' version.

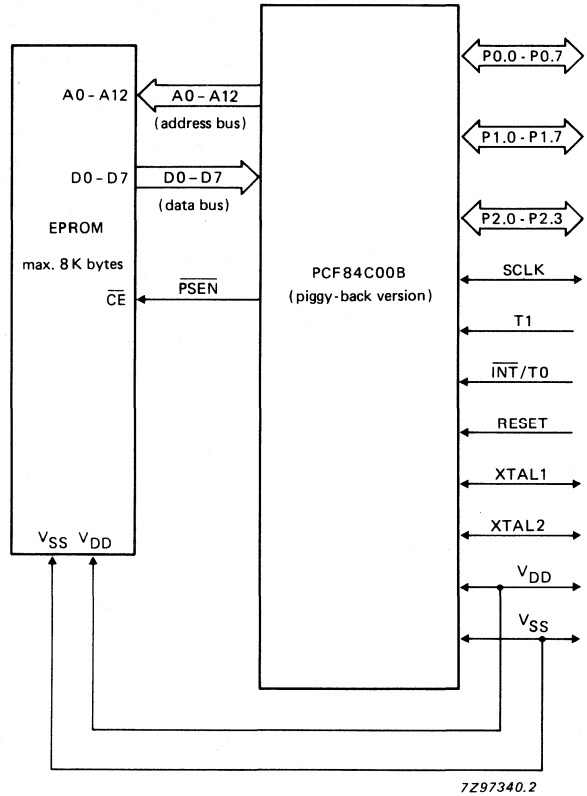


Fig. 3(b) Connection of EPROM to the PCF84C00B 'piggy-back' version.

The PCF84C00B is mainly used for prototyping and for low volume production applications. This device is packaged in a 'piggy-back' package. i.e. a 4 K or 8 K byte EPROM (2732 or 2764) may be mounted in the 24/28 pin socket on top of the package.

Notes

1. The PCF84C00B has 256 bytes of on-chip RAM.
2. Access time for ROMS/EPROMS must be less than 7 x $1/f_{XTAL}$.
3. Bottom pinning is identical to that of Fig. 2.

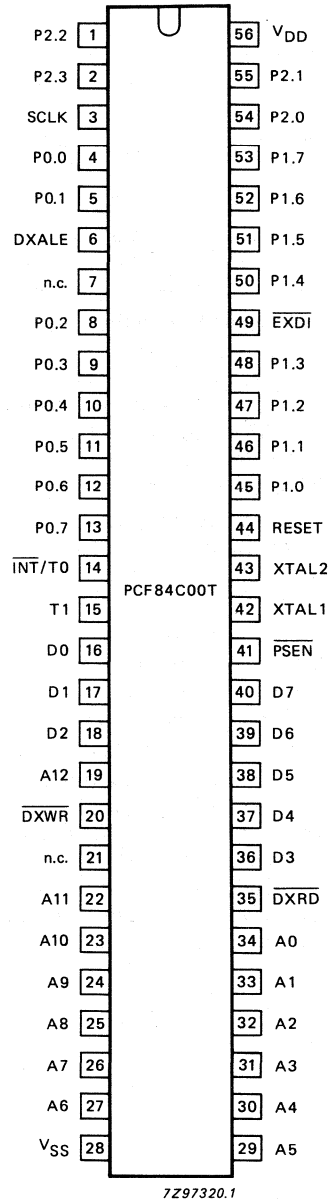


Fig. 4 Pinning diagram; ROM-less version PCF84C00T.

The PCF84C00T may be used for prototyping future derivatives of the PCF84CXX family or for low volume production applications. This device is packaged in a 56-lead VSO outline. Additional signals are available (see pinning information following) to control external program memory and derivative functions.

PIN FUNCTION (continued)

Pin	*Symbol*	*Type*	*Function*
34-29, 27-22, 19	A00-A12	O	**Address bus.** For external memory and pheripherals.
16-18, 36-40	D0-D7	I/O	**Data bus.** For external memory and pheripherals. The specified STOP mode supply current is valid only if external pull-ups are connected to all data lines.
41	$\overline{\text{PSEN}}$	O	**Program store enable** (active LOW). $\overline{\text{PSEN}}$ is used to enable external program memory and is active during TS9 and TS10 of each machine cycle and TS1 of each following cycle. $\overline{\text{PSEN}}$ is HIGH during the STOP mode.
6	DXALE	O	**Address latch enable.** On the falling edge of DXALE, the Dx address can be latched in an external latch. This signal occurs only during execution of the MOV Dx,A, MOV A,Dx, ANL Dx,A and ORL Dx,A instructions, with x = 0 to 255. It is active during TS10 of cycle 1 and the first half of TS1 of cycle 2.
35	$\overline{\text{DXRD}}$	O	**Read strobe** (active LOW). When this signal is active, external registers emulating Dx registers can be read by the data bus. This signal occurs only during execution of MOV A,Dx, ANL Dx,A and ORL Dx,A instructions, with x = 0 to 255. It is active during TS3 and TS4 of cycle 2.
20	$\overline{\text{DXWR}}$	O	**Write strobe** (active LOW). On the rising edge, data on D0-D7 may be written to external registers. This signal occurs only during MOV Dx,A, ANL Dx,A and ORL Dx,A instructions, with x = 0 to 255. It is active during TS7 of cycle 2.
49	$\overline{\text{EXDI}}$	I	**External derivative interrupt** (active LOW). $\overline{\text{EXDI}}$ is 'OR-ed' with the internal serial interrupt and can be used to initiate an interrupt from external hardware emulating derivative functions. $\overline{\text{EXDI}}$ is pulled HIGH internally. The derivative interrupt is polled during time slot TS6*, and is only accepted if an EN SI instruction has been executed and the device is not already executing an interrupt routine. Derivative interrupts are not latched in the PCF84C00.

* The interrupt signal must remain active until the vector address (05 H) is present on the address bus.

FUNCTIONAL DESCRIPTION

ROM-less version PCF84C00T

The PCF84C00T microcontroller contains no on-chip ROM, but has all address and data lines brought out to access an external ROM or EPROM. This version has more pins than the PCF84CXXX with on-chip ROM (see Fig. 1a). The PCF84C00T can address up to 8 K bytes of external program memory, and has 256 bytes of internal data RAM.

'Piggy-back' version PCF84C00B

The PCF84C00B package has standard pinning on the bottom to facilitate insertion as a mask-programmed device. An EPROM can be mounted on top in an additional socket. The total package height is greater than the height of a standard DIL package. The PCF84C00B can address up to 8 K bytes of external ROM/RAM, and has 256 bytes of internal data RAM.

Program memory

The program memory consists of 2, 4 or 8 K bytes of read-only memory (ROM). Each location is directly addressable by the program counter. The ROM is mask-programmed at the factory.

Data memory

Data memory consists of 64, 128 or 256 bytes of random-access memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer.

I/O facilities

Each device has 23 I/O lines arranged as follows:

- Port 0 8-bit parallel port (P0.0-P0.7)
- Port 1 8-bit parallel port (P1.0-P1.7)
- Port 2 4-bit parallel port (P2.0-P2.3)
- SCLK serial I/O clock line
- $\overline{\text{INT}}$/T0 external interrupt and test input. When used as a test input, it can be directly tested by conditional branch instructions JT0 and JNT0
- T1 test input which can alter program sequences when tested by conditional jump instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter

Reset

A positive-going signal on the RESET input/output:

- Sets the program counter to zero
- Selects location 0 of memory bank 0 and register bank 0
- Sets the stack pointer to zero (000); pointing to RAM address 8
- Disables the interrupts (external, timer and serial I/O)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to divide by 32
- Resets the timer flag
- Sets all ports except P2.3 to input mode
- Sets the serial I/O to slave receiver mode and disables the serial I/O
- Cancels IDLE and STOP mode

A negative-going signal on the RESET input/output:

- Sets P2.3/SDA and SCLK to HIGH after a maximum of 30 clock pulses
- Sets the serial I/O to slave receiver mode and disables the serial I/O after a maximum of 30 clock pulses
- Starts program execution after 1866 clock pulses

AC CHARACTERISTICS

V_{DD} = 2,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C. All voltages with respect to V_{SS} unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Rise time all outputs (note 1)	t_R	–	30	–	ns
Fall time all outputs (note 1)	t_F	–	30	–	ns
Cycle time (= 30 CP; note 2)	t_{CY}	3	–	30	μs
PCF84C00/non-standard pins:					
Control pulse width	t_{CC}	–	9	–	CP
Address to $\overline{PSEN}$ set-up	t_{AS}	–	1,5	–	CP
Data to $\overline{PSEN}$ set-up	t_{DS}	–	2	–	CP
Data hold time	t_{DR}	0	–	–	ns
Data out to $\overline{DWXR}$ set-up	t_{SDO}	–	2	–	CP
Data out to $\overline{DXWR}$ hold	t_{HDO}	–	1	–	CP
Time from DXALE to $\overline{PSEN}$	t_{SLPH}	–	1,5	–	CP
Data-in to $\overline{DXRD}$ set-up	t_{DS1}	–	2,5	–	CP
Data-in to $\overline{DXRD}$ hold	t_{DR1}	0	–	–	ns
HIGH time of DXALE	t_{DXALE}	–	4,5	–	CP
LOW time of $\overline{DXRD}$	t_{DXRD}	–	6	–	CP
LOW time of $\overline{DXWR}$	t_{DXWR}	–	3	–	CP

Notes:

1. At V_{DD} = 5 V; T_{amb} = + 25 °C; C_L = 50 pF.
2. 1 Time slot (TS) = 3 CP, 1 clock pulse (CP) = $1/f_{XTAL}$.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLERS

DESCRIPTION

An advanced CMOS process is used to manufacture the PCF84C12, PCF84C22 and PCF84C42 microcontrollers. Each device has 13 quasi-bidirectional I/O port lines, a single-level vectored interrupt structure, an 8-bit timer and on-chip clock oscillator and clock circuits. On-chip RAM and ROM content is as follows:

- PCF84C12 – 64 x 8 RAM, 1 K x 8 ROM
- PCF84C22 – 64 x 8 RAM, 2 K x 8 ROM
- PCF84C42 – 64 x 8 RAM, 4 K x 8 ROM

These efficient microcontrollers also perform well as arithmetic processors. The instruction set is similar to that of the MAB8048. They have bit handling abilities and facilities for both binary and BCD arithmetic.

These microcontrollers are members of the 84CXXX family. For detailed information, consult the 84CXXX family specification.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 20-lead DIL or SO package
- 1 K, 2 K or 4 K x 8 ROM
- 64 x 8 RAM
- 2 timers (8-bit programmable)
- 13 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input
- Single-level, vectored interrupts: external and timer/event counter
- 8-bit programmable timer/event counter
- Clock frequency range: 100 kHz to 10 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage (2.5 V to 5.5 V)
- STOP and IDLE modes
- Power-on-reset circuit
- Operating temperature range: −40 to + 85 °C

PACKAGE OUTLINES

PCF84C12/22/42P: 20-lead DIL; plastic (SOT146).
PCF84C12/22/42T: 20-lead mini-pack; plastic (SO20, SOT163A).

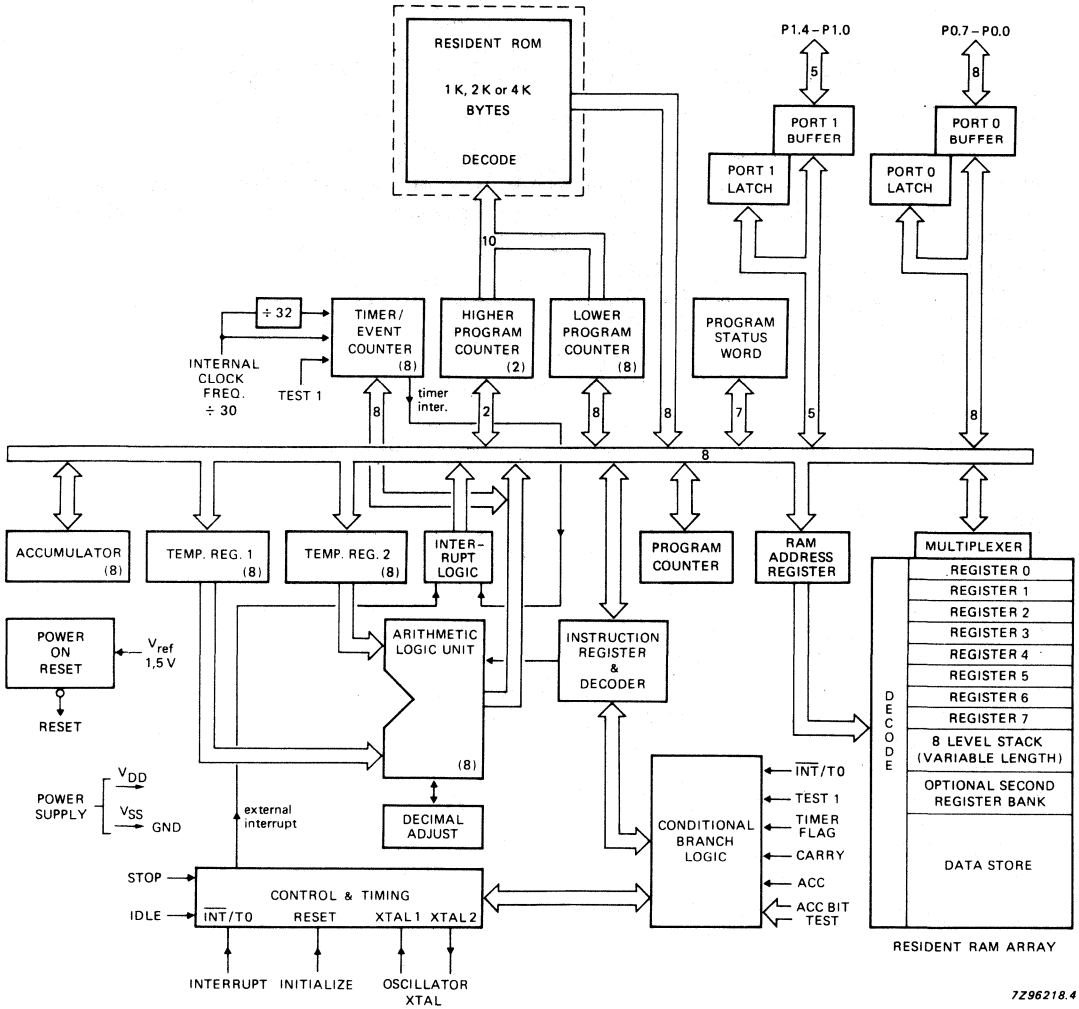


Fig. 1 Block diagram.

PINNING

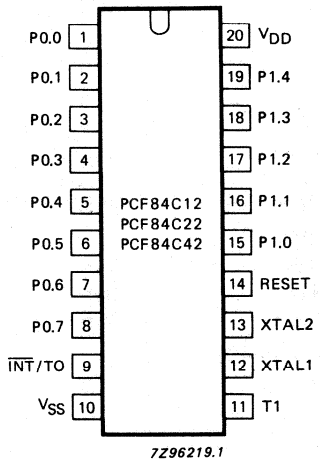


Fig. 2 Pinning diagram.

PIN DESIGNATION

1-8	P0.0-P0.7	**Port 0:** 8-bit quasi-bidirectional I/O port.
9	$\overline{INT}$/T0	**Interrupt/Test 0**: external interrupt input (negative edge triggered)/test input pin; when used as a test input, this pin is directly tested by conditional branch instructions JT0 and JNT0.
10	V_{SS}	**Ground:** circuit earth potential.
11	T1	**Test 1:** test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 may also be selected as an input to the 8-bit timer/event counter via the STRT CNT instruction.
12	XTAL 1	**Oscillator input:** input from a crystal which determines the internal oscillator frequency, or an external clock generator.
13	XTAL 2	**Oscillator output:** output of the inverting amplifier.
14	RESET	**Reset input:** used to initialize the microcontroller (active HIGH); also output of power-on-reset circuit.
15-19	P1.0-P1.4	**Port 1:** 8-bit quasi-bidirectional I/O port.
20	V_{DD}	**Power supply:** 2.5 V to 5.5 V.

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; all voltages with respect to V_{SS}; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating (see Fig. 3)	V_{DD}	2.5	–	5.5	V
Supply current					
operating (see Fig. 4 and note 2)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	1.6	3.2	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz	I_{DD}	–	1	2	mA
at V_{DD} = 3 V; f_{XTAL} = 3.58 MHz	I_{DD}	–	0.3	0.6	mA
IDLE mode (see Fig. 5 and note 2)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	0.8	1.6	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz	I_{DD}	–	0.5	1	mA
at V_{DD} = 3 V; f_{XTAL} = 3.58 MHz	I_{DD}	–	0.15	0.4	mA
STOP mode (see Fig. 8, note 1 and note 2)					
at V_{DD} = 2.5 V; T_{amb} = 25 °C	I_{DD}	–	1.2	2.5	μA
at V_{DD} = 2.5 V; T_{amb} = 85 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0.3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input leakage current					
as $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output sink current LOW					
at V_{DD} = 5 V ± 10%; V_O = 0.4 V	I_{OL}	1.6	3	–	mA
Pull-up output source current HIGH					
at V_{DD} = 5 V ± 10%; V_O = 0.7 V_{DD}	$-I_{OH}$	40	–	–	μA
at V_{DD} = 5 V ± 10%; V_O = V_{SS}	$-I_{OH}$	–	–	400	μA
Push-pull output source current HIGH					
at V_{DD} = 5 V ± 10%; V_O = V_{DD}−0.4 V	$-I_{OH}$	1.6	3	–	mA

Notes to the DC characteristics

1. Crystal connected between XTAL 1 and XTAL 2; T1 = V_{SS}; $\overline{INT}$ = V_{DD}.
2. V_{IL} = V_{SS}; V_{IH} = V_{DD}; all outputs unloaded; all open drain outputs connected to V_{SS}.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 32 I/O LINES

DESCRIPTION

The PCF84C85 microcontroller is manufactured in CMOS, and is designed to be an efficient controller as well as an arithmetic processor. The instruction set is based on that of the MAB8048 and is software compatible with the 84CXXX family. The PCF84C85 has two additional derivative ports and the microcontroller has bit handling abilities and facilities for both binary and BCD arithmetic.

For detailed information see the 84CXXX family specification.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 40-lead DIL or mini-pack package
- 8 K ROM
- 256 RAM bytes
- 32 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- I^2C hardware interface for two-line serial data transfer
  (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency 100 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2,5 V to 5,5 V
- STOP and IDLE mode
- Power-on-reset circuit
- Operating temperature range: −40 to +85 °C

PACKAGE OUTLINES

PCF84C85P: 40-lead DIL; plastic (SOT129).
PCF84C85T: 40-lead; mini-pack (VSO40; SOT158A).

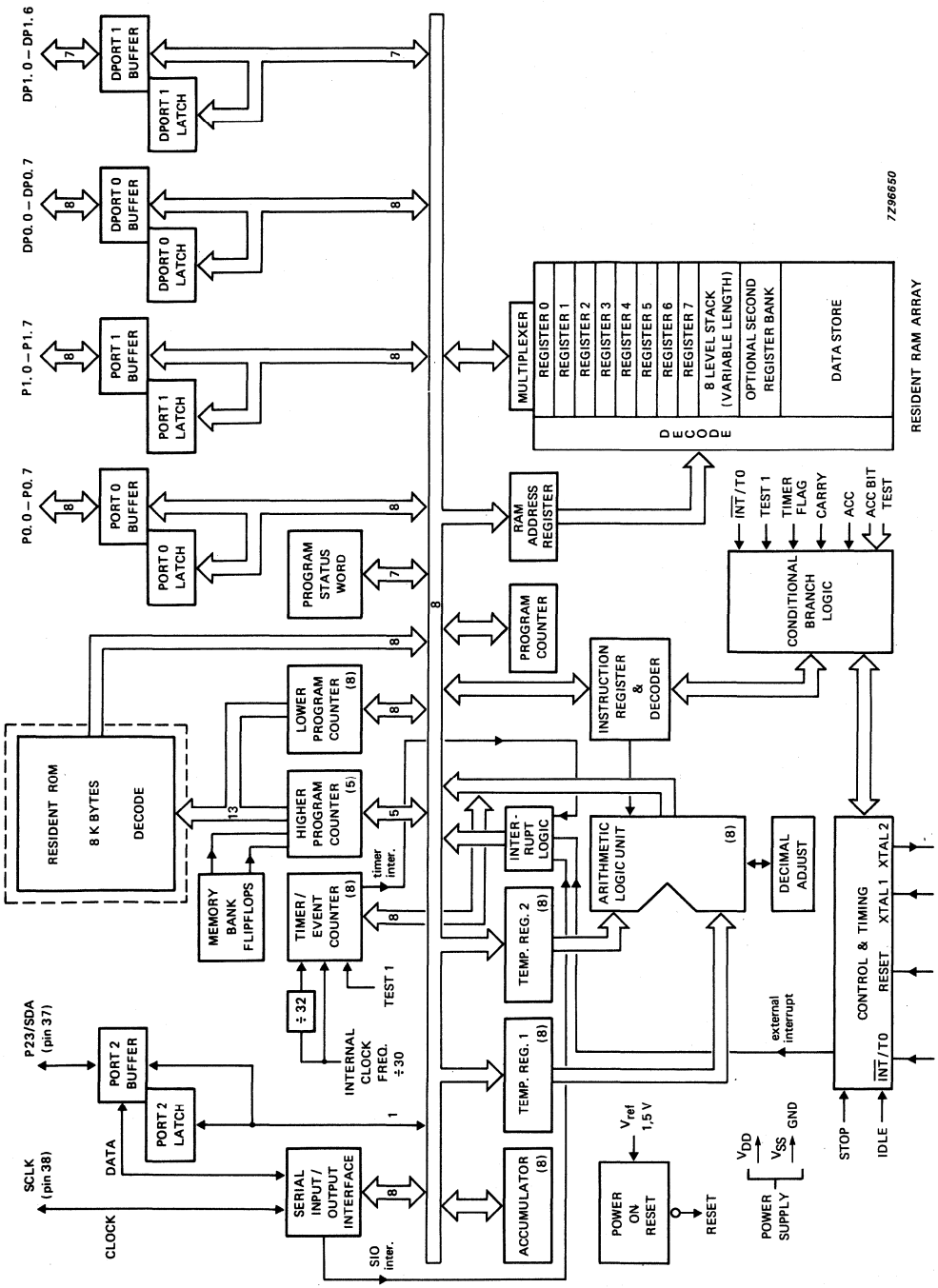


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

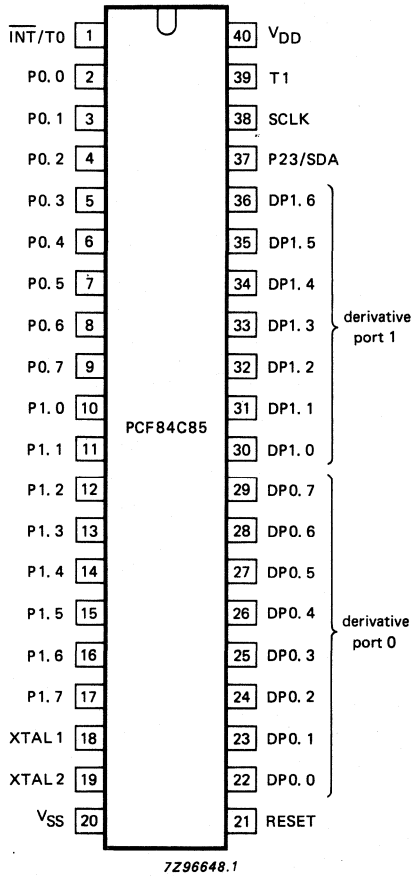


Fig. 2 Pinning diagram.

PIN DESIGNATION

38	SCLK	**Clock:** bidirectional clock for serial I/O.
1	$\overline{\text{INT}}$/T0	**Interrupt/Test 0:** external interrupt input (sensitive to negative-going edge)/test input pin; when used as a test input directly tested by conditional branch instructions JT0 and JNT0.
39	T1	**Test 1:** test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
18	XTAL 1	**Crystal input:** connection to timing component (crystal) which determines the frequency of the internal oscillator; also the input for an external clock source.
19	XTAL 2	Connection to the other side of the timing component.
21	RESET	**Reset input:** used to initialize the processor (active HIGH), or output of power-on-reset circuit.

PIN DESIGNATION (continued)

2-9	P0.0-P0.7	**Port 0:** 8-bit quasi-bidirectional I/O port.
10-17	P1.0-P1.7	**Port 1:** 8-bit quasi-bidirectional I/O port.
37	P23/SDA	**Port 2:** 1-bit quasi-bidirectional I/O port or serial data input/output in serial I/O mode.
22-29	DP0.0-DP0.7	**Derivative port 0:** 8-bit quasi-bidirectional I/O port.
30-36	DP1.0-DP1.6	**Derivative port 1:** 7-bit quasi-bidirectional I/O port.
20	V_{SS}	**Ground:** circuit earth potentional.
40	V_{DD}	**Power supply:** 2,5 V to 5,5 V.

FUNCTIONAL DESCRIPTION

Program memory

The program memory consists of 8 K bytes, in a read-only memory (ROM). Each location is directly addressable by the program counter. The memory is mask-programmed at the factory. Figure 3 shows the program memory map.

Four program memory locations are of special importance:

- Location 0; contains the first instruction to be executed after the processor is initialized (RESET),
- Location 3; contains the first byte of an external interrupt service subroutine;
- Location 5; contains the first byte of a serial I/O interrupt service subroutine.
- Location 7; contains the first byte of a timer/event counter interrupt service subroutine.

Program memory is arranged in banks of 2 K bytes, which are selected by SEL MB instructions. The program memory is further divided into location 'pages', each of 256 bytes. This latter division applies only for conditional branches. Memory bank boundaries can be crossed only by using unconditional branch instructions after the appropriate memory bank has been selected. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

Data memory

Data memory consists of 256 bytes, random-access data memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 4 shows the data memory map.

Working registers

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1, designates locations 24 to 31 as working registers, instead of locations 0 to 7, and these are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service subroutines saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first locations of each bank contain the RAM pointer registers R0, R1, R0' and R1', which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{DD} = 2,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; all voltages with respect to V_{SS}; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating (see Fig. 27)	V_{DD}	2,5	–	5,5	V
Supply current					
operating (see Fig. 28)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	1,6	3,2	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz	I_{DD}	–	1	2	mA
at V_{DD} = 3 V; f_{XTAL} = 3,58 MHz	I_{DD}	–	0,5	0,6	mA
IDLE mode (see Fig. 29)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	0,8	1,6	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz	I_{DD}	–	1	1	mA
at V_{DD} = 3 V; f_{XTAL} = 3,58 MHz	I_{DD}	–	0,25	0,4	mA
STOP mode (see Fig. 35 and note 1)					
at V_{DD} = 2,5 V; T_{amb} = 25 °C	I_{DD}	–	1,2	2,5	μA
at V_{DD} = 2,5 V; T_{amb} = 70 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current					
as $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output voltage LOW					
at V_I = V_{SS} or V_{DD}; $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW					
at V_{DD} = 5 V ± 10%; V_O = 0,4 V					
except P23/SDA, SCLK (see Fig. 31)	I_{OL}	1,6	3	–	mA
P23/SDA, SCLK (see Fig. 32)	I_{OL}	3	–	–	mA
Pull-up output source current HIGH (see Fig. 33)					
at V_{DD} = 5 V ± 10%; V_O = $0{,}7V_{DD}$	$-I_{OH}$	40	–	–	μA
at V_{DD} = 5 V ± 10%; V_O = V_{SS}	$-I_{OH}$	–	–	400	μA
Push-pull output source current HIGH					
at V_{DD} = 5 V ± 10%; V_O = V_{DD}−0,4 V	$-I_{OH}$	1,6	3	–	mA

Note 1

Crystal connected between XTAL1 and XTAL2; SCL and SDA pulled to V_{DD} via 5,6 kΩ resistor; T1 at V_{SS}, $\overline{INT}$ at V_{DD}.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 8 BYTES EEPROM

DESCRIPTION

An advanced CMOS process is used to manufacture the PCF84C121. The PCF84C121 has 13 quasi-bidirectional I/O port lines, three single-level vectored interrupts (one external and two timer), 8 bytes of EEPROM, two 8-bit timer counters and on-chip clock oscillator and clock circuits.

This efficient microcontroller also performs well as an arithmetic processor. The PCF84C121 is pin- and instruction set compatible with the PCF84C12. The PCF84C121 has bit handling abilities and facilities for both binary and BCD arithmetic.

This microcontroller is a member of the 84CXXX family. For detailed information, consult the 84CXXX family specification.

Features

- 8-bit CPU, ROM, RAM, EEPROM, I/O in a single 20-lead DIL or SO package
- 1 K x 8 ROM
- 64 x 8 RAM
- 8 x 8 EEPROM, designed for 10000 erase/write cycles per byte minimum
- 2 timers (8-bit programmable)
- 13 quasi-bidirectional I/O port lines
- 3 single-level, vectored interrupts: external, Timer 1 and Timer 2
- Two test inputs: one of which is also the external interrupt input
- 8-bit programmable timer/event counter
- Clock frequency range: 450 kHz to 10 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage
- STOP and IDLE modes
- Power-on-reset circuit
- Operating temperature range: −40 to +85 °C; 0 to +55 °C for programming

LIFE SUPPORT APPLICATIONS

This product is not designed for use in life support appliances, devices, or systems where malfunction of this product can reasonably be expected to result in personal injury. Philips customers using or selling this product for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PACKAGE OUTLINES

PCF84C121P: 20-lead DIL; plastic (SOT146).
PCF84C121T: 20-lead mini-pack; plastic (SO20; SOT163A).

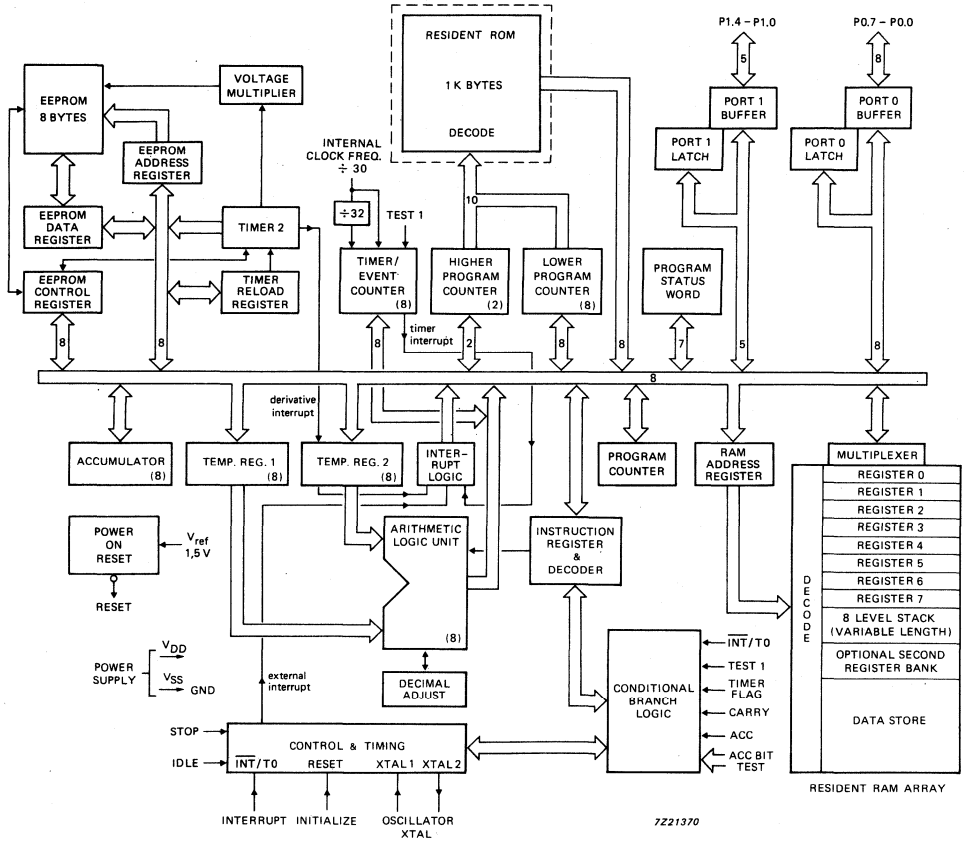


Fig. 1 Block diagram.

PINNING

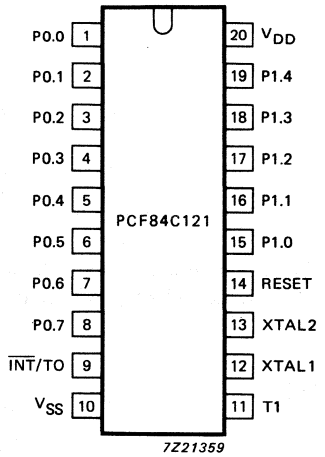


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

Pin function

Pin	*Symbol*	*Function*
1-8	P0.0-P0.7	**Port 0:** 8-bit quasi-bidirectional I/O port.
9	$\overline{\text{INT}}$/T0	**Interrupt/Test 0:** external interrupt input (negative edge triggered)/test input pin; when used as a test input, this pin is directly tested by conditional branch instructions JT0 and JNT0.
10	V_{SS}	**Ground:** circuit earth potential.
11	T1	**Test 1:** test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 may also be selected as an input to the 8-bit timer/event counter via the STRT CNT instruction.
12	XTAL 1	**Oscillator input:** input from a crystal which determines the internal oscillator frequency or an external clock generator.
13	XTAL 2	**Oscillator output**
14	RESET	**Reset input:** used to initialize the microcontroller (active HIGH); also output of power-on-reset circuit.
15-19	P1.0-P1.4	**Port 1:** 5-bit quasi-bidirectional parallel I/O port.
20	V_{DD}	**Power supply:** 2.5 to 5.5 V

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 20)	V_{DD}	−0.8 to + 8	V
All input voltages	V_I	0.8 to V_{DD} + 0.8	V
DC current into any input or output	$\pm I_I, \pm I_O$	max. 10	mA
Total power dissipation (see note 1)	P_{tot}	max. 125	mW
Power dissipation per output	P_O	max. 50	mW
Storage temperature range	T_{stg}	−65 to + 150	°C
Operating junction temperature	T_j	max. 125	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

Notes to the ratings

1. Thermal resistance (junction to ambient)

for SOT146	$R_{th\ j\text{-}a}$	max. 75	K/W
for SOT163A	$R_{th\ j\text{-}a}$	max. 135	K/W

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; all voltages with respect to V_{SS}; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating (see Fig. 4)	V_{DD}	2.5	–	5,5	V
Supply current					
operating (see Fig. 5 and note 2)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	2.0	3.5	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz	I_{DD}	–	1.2	2.4	mA
at V_{DD} = 3 V; f_{XTAL} = 3.58 MHz	I_{DD}	–	0.4	0.8	mA
IDLE mode (see Fig. 6 and note 2)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	1.0	2.0	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz	I_{DD}	–	0.7	1.4	mA
at V_{DD} = 3 V; f_{XTAL} = 3.58 MHz	I_{DD}	–	0.25	0.6	mA
STOP mode (see Fig. 9, note 1 and note 2)					
at V_{DD} = 2.5 V; T_{amb} = 85 °C	I_{DD}	–	–	10	μA
Erase/write cycle					
time	$t_{e/w}$	–	10	–	ms
data retention	Dr	10	–	–	years
Inputs					
Input voltage LOW	V_{IL}	0	–	$0.3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input leakage current					
as $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output sink current LOW					
at V_{DD} = 5 V ± 10%; V_O = 0.4 V	I_{OL}	1.6	3	–	mA
Pull-up output source current HIGH					
at V_{DD} = 5 V ± 10%; V_O = 0.7 V_{DD}	$-I_{OH}$	40	–	–	μA
at V_{DD} = 5 V ± 10%; V_O = V_{SS}	$-I_{OH}$	–	–	400	μA
Push-pull output source current HIGH					
at V_{DD} = 5 V ± 10%; V_O = V_{DD}−0.4 V	$-I_{OH}$	1.6	3	–	mA

Notes to the DC characteristics

1. Crystal connected between XTAL 1 and XTAL 2; T1 = V_{SS}; $\overline{INT}$ = V_{DD}.
2. V_{IL} = V_{SS}; V_{IH} = V_{DD}; all outputs unloaded; all open-drain outputs connected to V_{SS}.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH LCD DRIVER

GENERAL DESCRIPTION

The PCF84C230 is a single-chip 8-bit microcontroller manufactured in CMOS technology, and is a member of the 84CXXX family. For detailed information see the 84CXXX family specification.

The PCF84C230 provides 12 general purpose quasi-bidirectional I/O port lines, a line that is directly testable (T1), one external interrupt line, and an LCD driver for up to 64 graphic elements. The IC is mask-programmable and is designed for control in small systems with LCD displays.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 40-lead DIL package
- 2 K ROM bytes
- 64 RAM bytes
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- 12 quasi-bidirectional I/O port lines
- Configuration of I/O lines can be individually selected by mask (pull-up, open drain, push-pull)
- LCD drive circuit with 16 segment drivers and selectable backplane drive configuration: static or 2/3/4 multiplex, to drive up to 64 graphic elements
- LCD possible during STOP mode
- Single-level vectored interrupts: external and timer/event counter
- Power-on reset and low voltage detector
- Single supply voltage from 2.5 V to 5.5 V
- STOP and IDLE modes
- Clock frequency 100 kHz to 10 MHz
- Operating ambient temperature range: −40 to + 85 °C

PACKAGE OUTLINES

40-lead DIL; plastic (SOT129).
40-lead mini-pack; plastic (VS040; SOT158A).

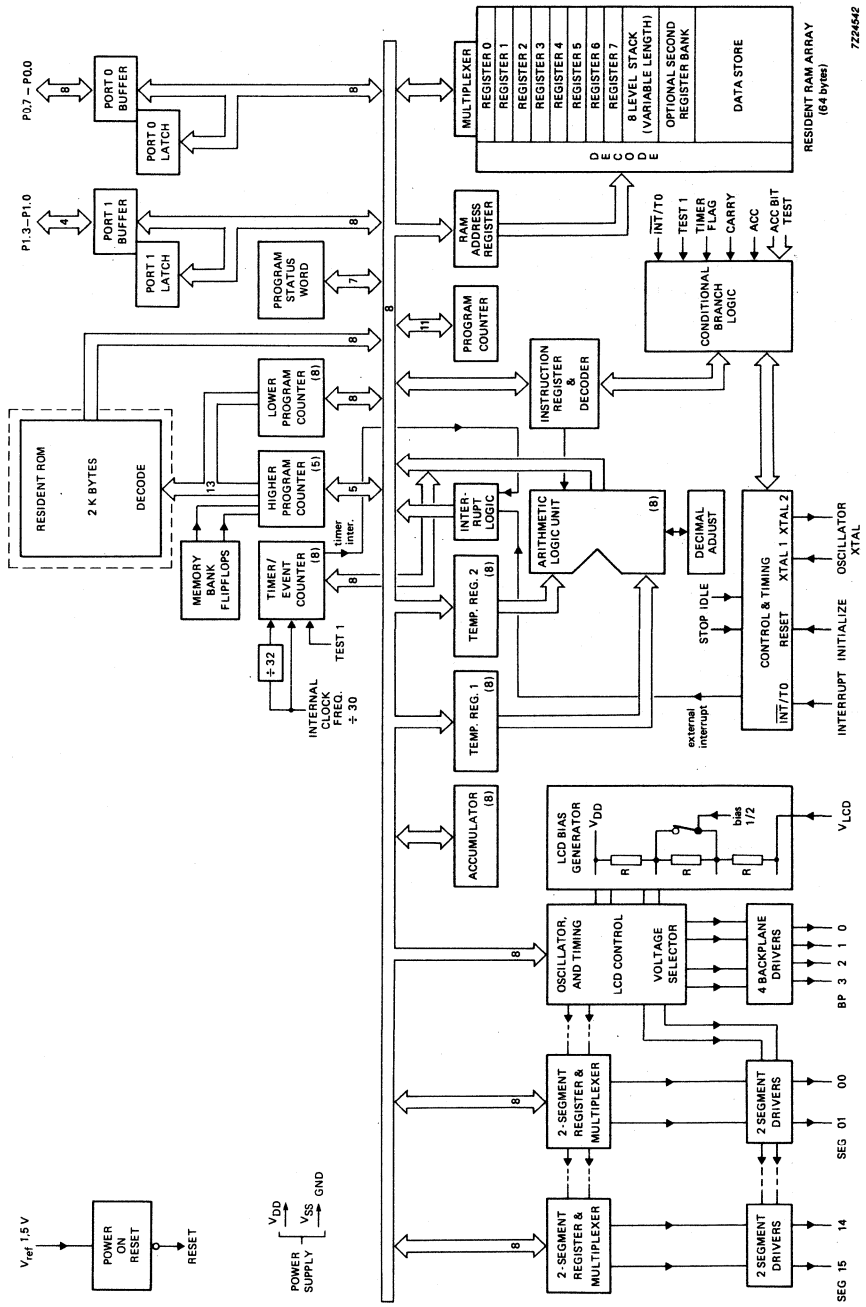


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

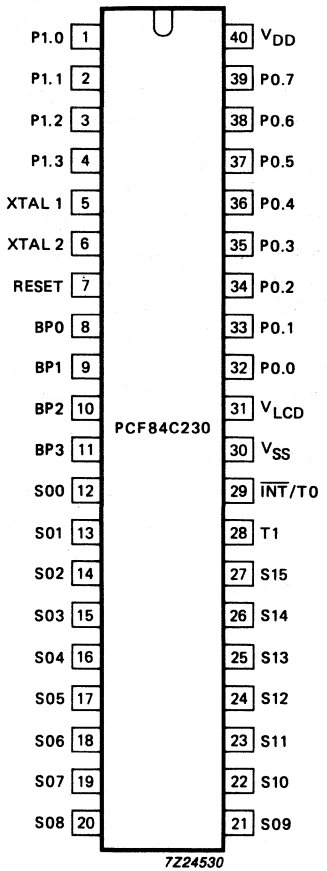


Fig.2 Pinning diagram.

Pin functions

pin no.	mnemonic	description
1 to 4	P1.0 to P1.3	**Port 1**: 4-bit quasi-bidirectional I/O port. This port can be mask programmed to either standard I/O, open drain or push-pull.
5	XTAL 1	**Crystal input**: connected to the timing component which determines the frequency of the internal oscillator; also used as an external clock source.
6	XTAL 2	Connection to the other side of the timing component.
7	RESET	**Reset**: bidirectional reset, used to initialize the processor or output of power-on reset circuit.
8 to 11	BP0 to BP3	**LCD**: backplane outputs.
12 to 27	S00 to S15	**LCD**: segment driver outputs.
28	T1	**Test 1**: test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
29	$\overline{INT}$/T0	**Interrupt/Test 0**: external interrupt input, sensitive to negative going edge. Also shared with test input 0; when used as a test input directly tested by conditional branch instructions JT0 and JNT0.
30	V_{SS}	**Ground**: circuit earth potential.
31	V_{LCD}	**LCD supply**: LCD supply voltage.
32 to 39	P0.0 to P0.7	**Port 0**: 8-bit quasi-bidirectional I/O port. This port can be mask programmed to either standard I/O, open drain or push-pull.
40	V_{DD}	**Power supply**: 2.5 V to 5.5 V.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 40)	V_{DD}	−0.8	+ 8.0	V
All input voltages	V_I	−0.8	V_{DD} + 0.8	V
DC current into any input or output	$\pm I_I, \pm I_O$	–	10	mA
Total power dissipation	P_{tot}	–	500	mW
Power dissipation per output	P_O	–	50	mW
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Operating junction temperature	T_j	–	+ 125	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DEVELOPMENT DATA

LCD DRIVER CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C. All voltages with respect to V_{SS} unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
LCD supply voltage	note 1	V_{LCD}	V_{SS}	–	V_{DD}−2	V
DC voltage component (BP0 to BP3)	V_{DD} = 5 V	$\pm V_{BP}$	0	–	20	mV
DC voltage component (S00 to S15)	V_{DD} = 5 V	$\pm V_S$	–	–	20	mV
Output impedance (BP0 to BP3)	$V_{LCD} = V_{DD}-5$ V; note 2	R_{BP}	–	2.5	5	kΩ
Output impedance (S00 to S15)	$V_{LCD} = V_{DD}-5$ V; note 2	R_S	–	4.5	7	kΩ
Driver delays with test loads	$V_{LCD} = V_{DD}-5$ V	t_{PLCD}	–	–	30	μs
LCD frame scan frequency		f_{LCD}	–	60	–	Hz

Notes to the LCD driver characteristics

1. $V_{LCD} < V_{DD}-3$ V for 1/3 bias.
2. Outputs measured one at a time in DC mode; V_{DD} = 5.5 V.

DC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; all voltages with respect to V_{SS}; f_{XTAL} = 10 MHz; R_S = 50 Ω unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	2.5	–	5.5	V
Supply current operating	note 1					
	V_{DD} = 3 V; f_{XTAL} = 3.58 MHz	I_{DD}	–	0.4	0.8	mA
	V_{DD} = 5.0 V; f_{XTAL} = 6 MHz	I_{DD}	–	1.0	2.0	mA
	V_{DD} = 5.0 V; f_{XTAL} = 10 MHz	I_{DD}	–	1.6	3.2	mA
IDLE mode						
	V_{DD} = 3 V; f_{XTAL} = 3.58 MHz	I_{DD}	–	0.15	0.4	mA
	V_{DD} = 5.0 V; f_{XTAL} = 6 MHz	I_{DD}	–	0.5	1.0	mA
	V_{DD} = 5.0 V; f_{XTAL} = 10 MHz	I_{DD}	–	0.8	1.6	mA
STOP mode						
	V_{DD} = 2.5 V; T_{amb} = 25 °C	I_{DD}	–	15	30	μA
	V_{DD} = 2.5 V; T_{amb} = 85 °C	I_{DD}	–	12	24	μA
Inputs						
Input voltage LOW		V_{IL}	0	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Input leakage current	$V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs						
Output voltage LOW	V_I = V_{SS} or V_{DD}; $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	0.05	V
Output sink current LOW	V_{DD} = 5 V ± 10%; V_O = 0.4 V	I_{OL}	1.6	3.0	–	mA
Pull-up output source current HIGH	V_{DD} = 5 V ± 10%; V_O = 0.7 V_{DD}	$-I_{OH}$	40	–	–	μA
	V_O = 0.4 V	$-I_{OH}$	–	–	400	μA
Push-pull output source current HIGH	V_{DD} = 5 V ± 10%; V_O = V_{DD}−0.4 V	$-I_{OH}$	1.6	3.0	–	mA

Notes to the DC characteristics

1. V_{IL} = V_{SS}; V_{IH} = V_{DD}; all outputs unloaded; all open drain outputs connected to V_{SS}.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH LCD DRIVERS, DERIVATIVE PORT, TIMER/CAPTURE AND TIMER/COUNTER

DESCRIPTION

The PCF84C633A is a microcontroller with 20 on-chip liquid crystal display (LCD) outputs. These can be configured for one to four backplanes and 19 to 16 segment lines, yielding a maximum of 64 display elements. In addition to the shared features of the PCF84CXX family of microcontrollers, the PCF84C633A includes a 16-bit timer with capture and compare registers, a 16-bit up/down counter/timer and two filtered control inputs. Together with additional derivative port lines, these powerful extensions make the device attractive for demanding real-time applications.

IMPORTANT

This data sheet details the specific properties of the PCF84C633A. The shared characteristics of the 84CXXX family of microcontrollers are described in 84CXXX family specification, which should be read in conjunction with this publication.

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 56-lead package
- 6 K bytes ROM
- 256 bytes RAM
- Over 80 instructions (based on MAB 8048) all of 1 or 2 cycles
- 28 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter
- 16-bit derivative timer with capture and compare registers (T2)
- 16-bit up/down counter/timer (T3)
- 2 filtered input lines coupled to T2 and T3
- 3 single-level vectored interrupts; external, 8-bit programmable timer/event counter, derivative (triggered by 4 events in T2 and T3)
- 2 test inputs of which one also serves as the external interrupt input
- 20 LCD output configurable for one to four backplanes and 19 to 16 segment lines
- Drive for up to 64 display elements
- Display memory bank switching in static and duplex drive modes
- 19 of the LCD outputs may serve as additional low-drive logic outputs with optional level-shift
- Stop and idle modes
- Logic supply V_{DD}; 2.5 V to 5.5 V
- Independent LCD supply V_{DDLC}; 2.5 V to 5.5 V
- Clock frequency: 1 MHz to 16 MHz
- Operating temperature range: −40 °C to 85 °C
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINE

PCF84C633AT: 56-lead mini-pack; plastic (VSO56; SOT190)

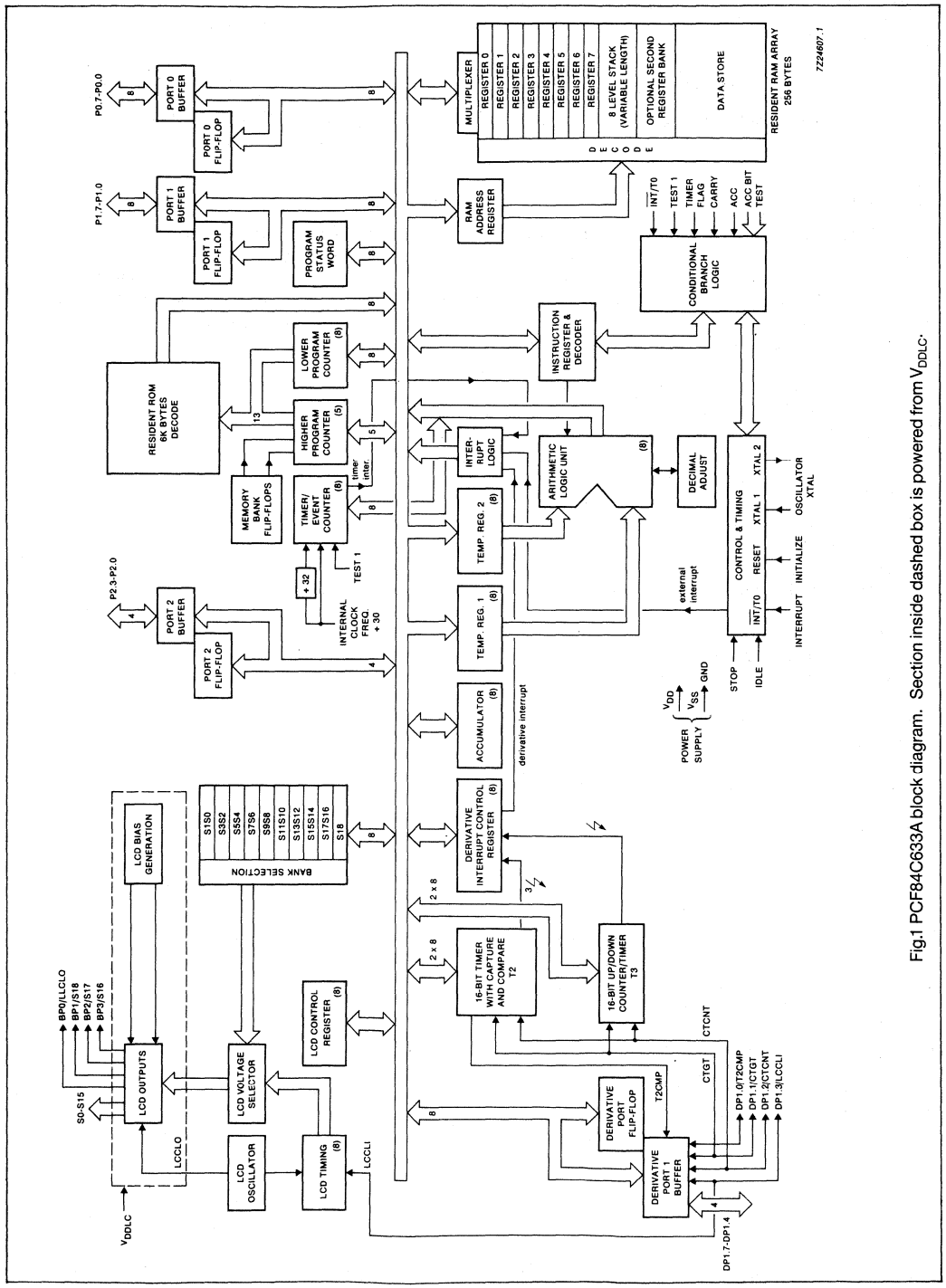


Fig.1 PCF84C633A block diagram. Section inside dashed box is powered from V_{DDLC}.

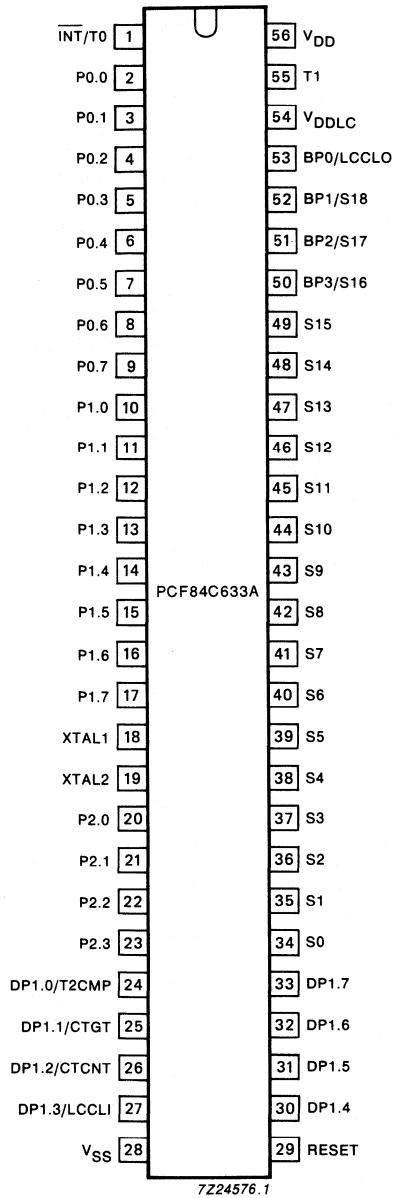


Fig.2 Pinning diagram.

Pinning

PIN	SYMBOL	TYPE	FUNCTION
1	INT/T0	I	Interrupt/Test 0
2-9	P0.0-P0.7	I/O	Port 0; 8-bit quasi-bidirectional I/O port
10-17	P1.0-P1.7	I/O	Port 1; 8-bit quasi-bidirectional I/O port
18	XTAL1	I	Crystal oscillator/external clock input
19	XTAL2	O	Crystal oscillator output
20-23	P2.0-P2.3	I/O	Port 2; 4-bit quasi-bidirectional I/O port
24	DP1.0/T2CMP	I/O	Derivative Port 1; quasi-bidirectional I/O line/compare output of T2
25	CP1.1/CTGT	I/O	Derivative Port 1; quasi-bidirectional I/O line/capture input (T2) and/or gate input (T3)
26	DP1.2/CTCNT	I/O	Derivative Port 1; quasi-bidirectional I/O line/capture input (T2) and/or count input (T3)
27	DP1.3/LCCLI	I/O	Derivative Port 1; quasi-bidirectional I/O line/LCD clock input
28	V_{SS}	P	Ground
29	RESET	I	Reset input
30-33	DP1.4-DP1.7	I/O	Derivative Port 1; quasi-bidirectional I/O port
34-49	S0-S15	O	LCD segment outputs
50-52	BP3/S16-BP1/S18	O	LCD backplane/segment outputs
53	BP0/LCCLO	O	LCD backplane/LCD oscillator output
54	V_{DDLC}	P	LCD supply voltage
55	T1	I	Test 1/count input of 8-bit timer/event counter
56	V_{DD}	P	Logic supply voltage

DC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{DDLC} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; all voltages with respect to V_{SS}; unless otherwise specified. See Figs.17 to 31.

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Logic supply voltage operating		V_{DD}	2.5	–	5.5	V
LCD supply voltage	$V_{DDLC} \geq 3V$ for 1/3 bias	V_{DDLC}	2.5	–	5.5	V
Logic supply current operating	(note 1)					
	V_{DD} = 5 V, f_{XTAL} = 16 MHz	I_{DD}	–	2.6	5.2	mA
	V_{DD} = 5 V, f_{XTAL} = 10 MHz	I_{DD}	–	1.6	3.2	mA
	V_{DD} = 3 V; f_{XTAL} = 3.58 MHz	I_{DD}	–	0.3	0.6	mA
IDLE mode	(note 1)					
	V_{DD} = 5 V; f_{XTAL} = 16 MHz	I_{DD}	–	1.3	2.6	mA
	V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	0.8	1.6	mA
	V_{DD} = 3 V; f_{XTAL} = 3.58 MHz	I_{DD}	–	0.15	0.4	mA
STOP mode	(notes 1 and 2)					
	LCD oscillator running, V_{DD} = 2.5 V	I_{DD}	–	10	30	µA
STOP mode	(notes 1, 2 and 3)					
	LCD oscillator stopped, V_{DD} = 2.5 V	I_{DD}	–	5	10	µA
LCD supply current	(note 4)	I_{DDLC}	–	10	20	µA
Inputs						
Input voltage LOW		V_{IL}	0	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	$\pm I_L$	–	–	1	µA
Port Outputs						
Output sink current LOW	V_{DD} = 5 V; V_O = 0.4 V	I_{OL}	1.6	5.5	–	mA
Pull-up output source current HIGH	V_{DD} = 5 V; $V_O = 0.7V_{DD}$	$-I_{OH}$	40	–	–	µA
	V_{DD} = 5 V; $V_O = V_{SS}$	$-I_{OH}$	–	–	400	µA
Push-pull output source current HIGH	V_{DD} = 5 V; $V_O = V_{DD}$ − 0.4 V	$-I_{OH}$	1.6	4	–	mA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
LCD Outputs						
Output sink current LOW	V_{DDLC} = 5 V; V_O = 0.4 V	I_{OL}	1	2.8	–	mA
Output source current HIGH	V_{DDLC} = 5 V; V_O = V_{DDLC} − 0.4 V	$-I_{OH}$	1	2	–	mA
Output impedance (BP3/S16 to BP0/LCCLO)	V_{DDLC} = 5 V and I_{BP} = 100 µA Outputs measured one at a time	R_{BP}	–	–	5	kΩ
Output impedance (S0 to S15)	V_{DDLC} = 5 V and I_S = 100 µA Outputs measured one at a time	R_S	–	–	7	kΩ
DC voltage component (BP3/S16 to BP0/LCCLO)	V_{DDLC} = 5 V; LCD modes	$\pm V_{BP}$	–	20	–	mV
DC voltage component (S0 to S15)	V_{DDLC} = 5 V; LCD modes	$\pm V_S$	–	20	–	mV
Oscillator transconductance						
option 'LOW' gm	V_{DD} = 5 V	gmL	0.3	0.4	–	mA/V
option 'MEDIUM' gm	V_{DD} = 5 V	gmM	0.9	1.2	–	mA/V
option 'HIGH' gm	V_{DD} = 5 V	gmH	3	4	–	mA/V
Oscillator feedback resistor		R_f	0.4	0.8	1.6	MΩ

Notes to characteristics

1. V_{IL} = 0, V_{IH} = V_{DD}; open drain outputs connected to V_{SS}; all other outputs open.
2. Crystal connected between XTAL1 and XTAL2; pin T1 at V_{SS}; pin INT/T0 at V_{DD}.
3. E0 = 0 in LCD control register; if E1 = 1, f_{LCCLI} = 1.5 kHz.
4. f_{LCCLI} = 1.5 kHz if measured in LCD drive 1 mode.

AC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C. All voltages with respect to V_{SS}; unless otherwise specified. See Fig.17.

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Rise time all outputs	V_{DD} = 5 V, T_{amb} = 25 °C, C_L = 50 pF	t_R	–	30	–	ns
Fall time all outputs	V_{DD} = 5 V, T_{amb} = 25 °C, C_L = 50 pF	t_F	–	30	–	ns
Clock frequency		f_{XTAL}	1	–	16	MHz
LCD oscillator frequency	V_{DD} = 5 V	f_{LCCLO}	0.9	1.5	2.4	kHz

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH DERIVATIVE PORTS, TIMER/CAPTURE AND TIMER/COUNTER

DESCRIPTION

The PCF84C853A is a microcontroller with 33 quasi-bidirectional I/O port lines. In addition to the shared features of the PCF84CXX family of microcontrollers, the PCF84C853 includes a 16-bit timer with capture and compare registers, a 16-bit up/down counter/timer and two filtered control inputs. Together with additional derivative port lines, these powerful extensions make the device attractive for demanding realtime applications.

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 40-lead package
- 8 K bytes ROM
- 256 bytes RAM
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- 33 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter
- 16-bit derivative timer with capture and compare registers (T2)
- 16-bit up/down counter/timer (T3)
- 2 filtered input lines coupled to T2 and T3
- 3 single-level vectored interrupt: external, 8-bit programmable timer/event counter, derivative (triggered by 4 events in T2 and T3)
- 2 test inputs of which one also serves as the external interrupt input
- Stop and Idle modes
- Supply range V_{DD}: 2.5 V to 5.5 V
- Clock frequency: 1 MHz to 16 MHz
- Operating temperature range: −40 °C to + 85 °C
- Manufactured in silicon gate CMOS process

IMPORTANT

This data sheet details the specific properties of the PCF84C853A. The shared characteristics of the 84CXXX family of microcontrollers are described in 84CXXX family specification, which should be read in conjunction with this publication.

PACKAGE OUTLINES

PCF84C853AP: 40-lead DIL; plastic (SOT129)
PCF84C853AT: 40-lead mini-pack; plastic (VSO40; SOT158A)

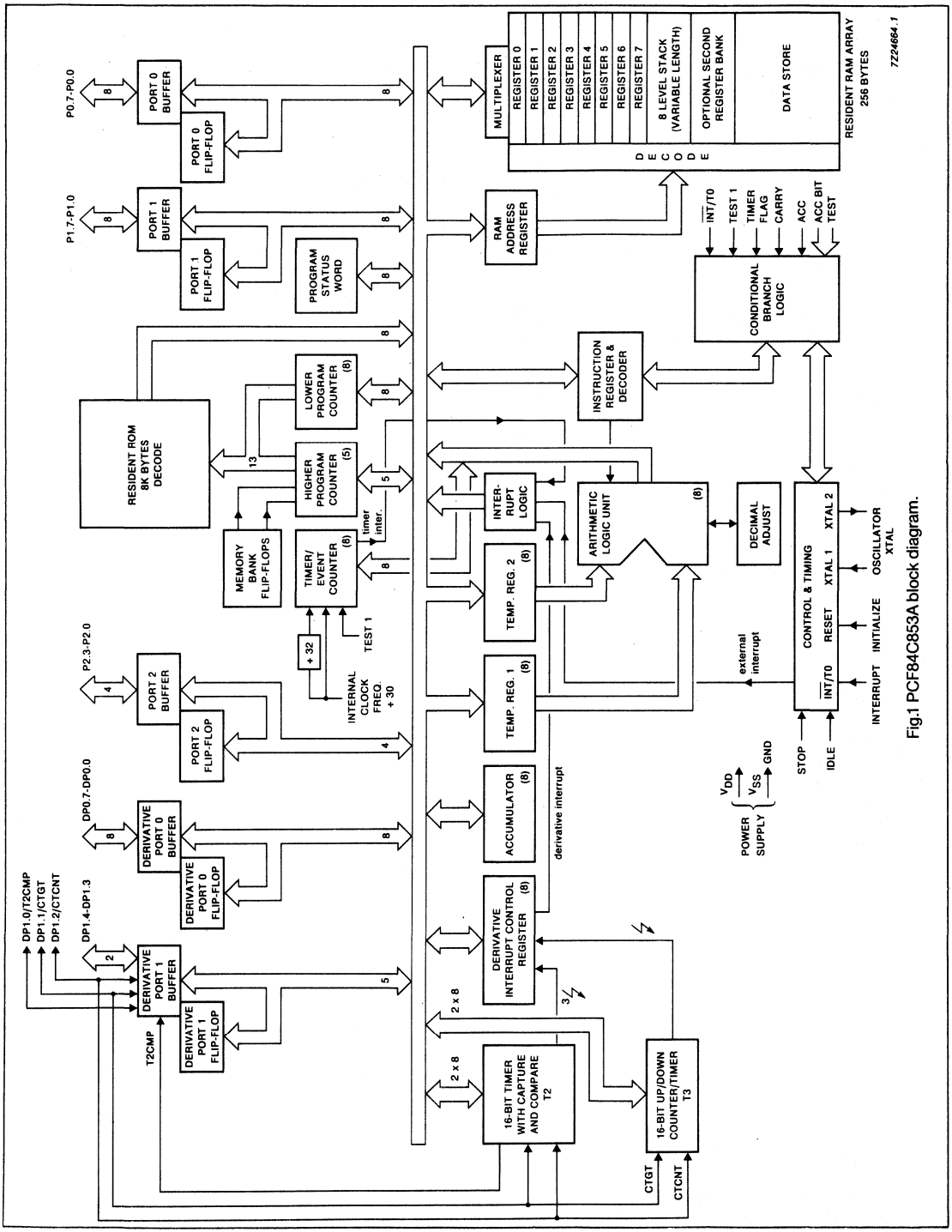


Fig.1 PCF84C853A block diagram.

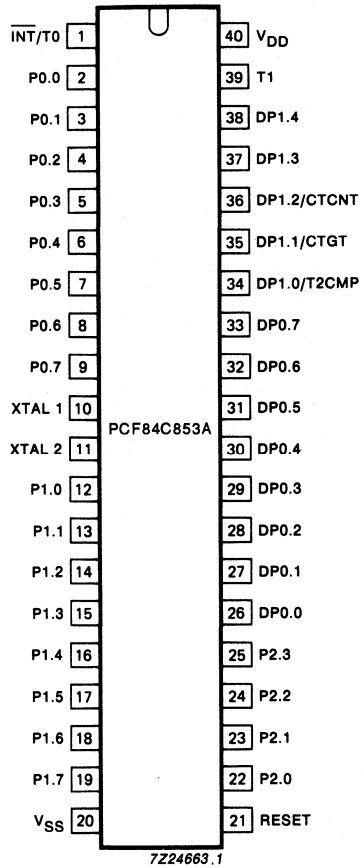


Fig.2 Pinning diagram.

Pinning

PIN	SYMBOL	TYPE	FUNCTION
1	INT/T0	I	Interrupt/Test 0
2-9	P0.0-P0.7	I/O	Port 0 : 8-bit quasi-bidirectional I/O port
10	XTAL1	I	Oscillator/external clock input
11	XTAL2	O	Oscillator output
12-19	P1.0-P1.7	I/O	Port 1: 8-bit quasi-bidirectional I/O port
20	V_{SS}	P	Ground
21	RESET	I	Reset input
22-25	P2.0-P2.3	I/O	Port 2: 4-bit quasi-bidirectional I/O port
26-33	DP0.0-DP0.7	I/O	Derivative Port 0: 8-bit quasi-bidirectional I/O port
34	DP1.0/T2CMP	I/O	Derivative Port 1: quasi-bidirectional I/O line/compare output of T2
35	DP1.1/CTGT	I/O	Derivative Port 1: quasi-bidirectional I/O line/capture input (T2) and/or gate input (T3)
36	DP1.2/CTCNT	I/O	Derivative Port 1: quasi-bidirectional I/O line/capture input (T2) and/or count input (T3)
37-38	DP1.3-DP1.4	I/O	Derivative Port 1: quasi-bidirectional I/O port
39	T1	I	Test 1/count input of 8-bit timer/event counter
40	V_{DD}	P	Supply voltage

DC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to 85 °C; all voltages with respect to V_{SS}; unless otherwise specified. See Figs.9 to 18.

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage, operating		V_{DD}	2.5	–	5.5	V
Supply current, operating	note 1					
	V_{DD} = 5 V; f_{XTAL} = 16 MHz	I_{DD}	–	2.6	5.2	mA
	V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	1.6	3.2	mA
	V_{DD} = 3 V; f_{XTAL} = 3.58 MHz	I_{DD}	–	0.3	0.6	mA
IDLE mode	note 1					
	V_{DD} = 5 V; f_{XTAL} = 16 MHz	I_{DD}	–	1.3	2.6	mA
	V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	0.8	1.6	mA
	V_{DD} = 5 V; f_{XTAL} = 3.58 MHz	I_{DD}	–	0.15	0.4	mA
STOP	notes 1 and 2					
	V_{DD} = 2.5 V; T_{amb} = 25 °C	I_{DD}	–	1.2	2.5	µA
	V_{DD} = 2.5 V; T_{amb} = 85 °C	I_{DD}	–	–	1O	µA
Inputs						
Input voltage LOW		V_{IL}	0	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	$\pm I_{IL}$	–	–	1	µA
Outputs						
Output sink current LOW	V_{DD} = 5 V; V_O = 0.4 V	IO_L	1.6	5.5	–	mA
Pull-up output source current HIGH	V_{DD} = 5 V; V_O = 0.7 V_{DD}	$-I_{OH}$	40	–	–	µA
	V_{DD} = 5 V; V_O = V_{SS}	$-I_{OH}$	–	–	400	µA
Push-pull output source current HIGH	V_{DD} = 5 V; V_O = V_{DD}−0.4 V	$-I_{OH}$	1.6	4	–	mA
Oscillator transconductance						
option LOW gm	V_{DD} = 5 V	gmL	0.3	0.4	–	mA/V
option MEDIUM gm	V_{DD} = 5 V	gmM	0.9	1.2	–	mA/V
option HIGH gm	V_{DD} = 5 V	gmH	3	4	–	mA/V
Oscillator feedback resistor		Rf	0.4	0.8	1.6	MΩ

Notes to characteristics

1. V_{IL} = 0, V_{IH} = V_{DD}; open drain outputs connected to V_{SS}; all other outputs open.
2. Crystal connected between XTAL1 and XTAL2; pin T1 and V_{SS}; pin INT/T0 at V_{DD}.

AC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to 85 °C. All voltages with respect to V_{SS}; unless otherwise specified. See Fig.9.

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Rise time all outputs	V_{DD} = 5 V, T_{amb} = 25 °C, C_L = 50 pF	t_R	–	30	–	ns
Fall time all outputs	V_{DD} = 5 V, T_{amb} = 25 °C, C_L = 50 pF	t_F	–	30	–	ns
Clock frequency		f_{XTAL}	1	–	16	MHz

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2,5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8566P: 40-lead DIL; plastic (SOT129).
PCF8566T: 40-lead mini-pack (VSO40; SOT158A).

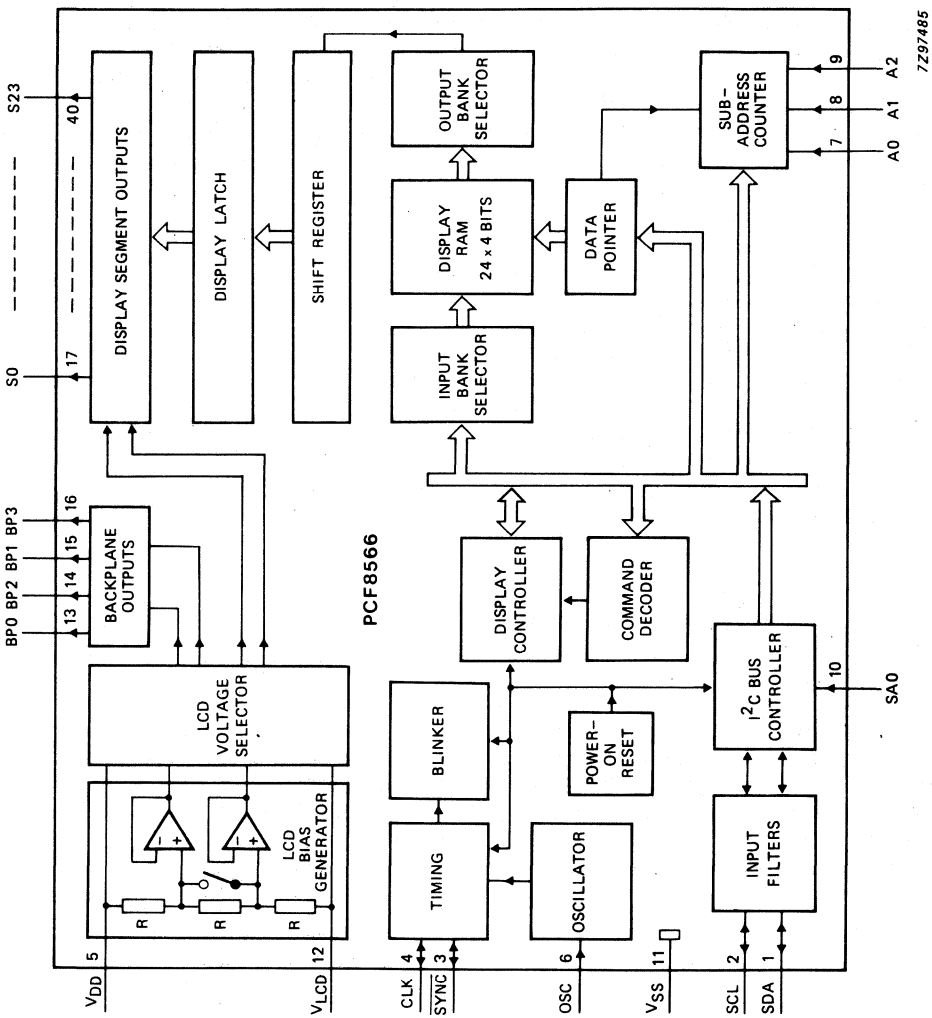


Fig. 1 Block diagram.

DEVELOPMENT DATA

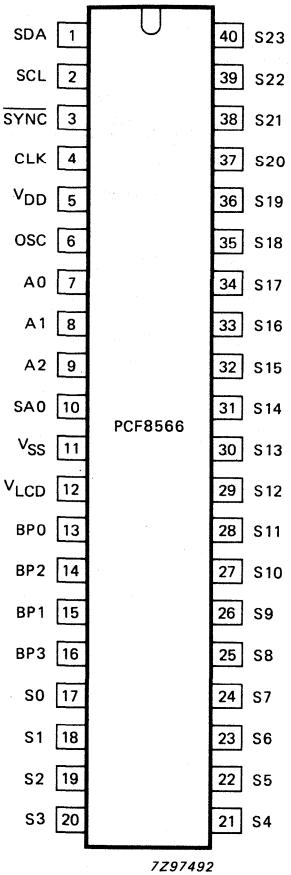


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17 to 40	S0 to S23	LCD segment outputs

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range; see note	V_{DD}		−0,5 to + 7 V
LCD supply voltage range	V_{LCD}		V_{DD} −7 to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS} −0,5 to V_{DD} + 0,5 V
Output voltage range (S0 to S23; BP0 to BP3)	V_O		V_{LCD} −0,5 to V_{DD} + 0,5 V
DC input current	$\pm I_I$	max.	20 mA
DC output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C

Note

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2,5 to 6 V; V_{LCD} = V_{DD} −2,5 to V_{DD} −6 V;

T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6	V
LCD supply voltage	V_{LCD}	V_{DD} −6	–	V_{DD} −2,5	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 1)	I_{DD}	–	30	90	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz; A0, A1 and A2 tied to V_{SS} (note 1)	I_{LP}	–	15	40	μA

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD} –0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	–1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SA0, CLK, OSC, A0, A1, A2, SCL, SDA) at $V_I = V_{SS}$ or V_{DD}	$\pm I_L$	–	–	1	μA
Pull-down current (A0; A1; A2; OSC) at V_I = 1 V and V_{DD} = 5 V	I_{pd}	15	50	150	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	15	25	60	kΩ
Power-on reset level (note 2)	V_{REF}	–	1,3	2,0	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 3)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S23) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}$ –5 V (note 4)	R_{BP}	–	1	5	kΩ
Output impedance (S0 to S23) at $V_{LCD} = V_{DD}$ –5 V (note 4)	R_S	–	3	7,0	kΩ

AC CHARACTERISTICS (note 5)

V_{SS} = 0 V; V_{DD} = 2,5 to 6 V; V_{LCD} = V_{DD} −2,5 to V_{DD} −6 V;
T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V (note 6)	f_{CLK}	125	200	315	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at V_{LCD} = V_{DD} −5 V	t_{PLCD}	–	–	30	μs
I²C bus					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_r	–	–	1	μs
Fall time	t_f	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs

Notes to characteristics

1. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C bus inactive.
2. Resets all logic when $V_{DD} < V_{REF}$.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
6. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8569 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8 or 1:16. The device has 40 outputs and can drive 16 x 40 dots in a 16 row multiplexed LCD. Up to 16 PCF8569s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8568/78/79 family of LCD row/column drivers. Together the PCF8568, PCF8578 and PCF8569 form a general LCD dot matrix driver chip set, capable of driving displays of up to 20 480 dots. The PCF8569 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

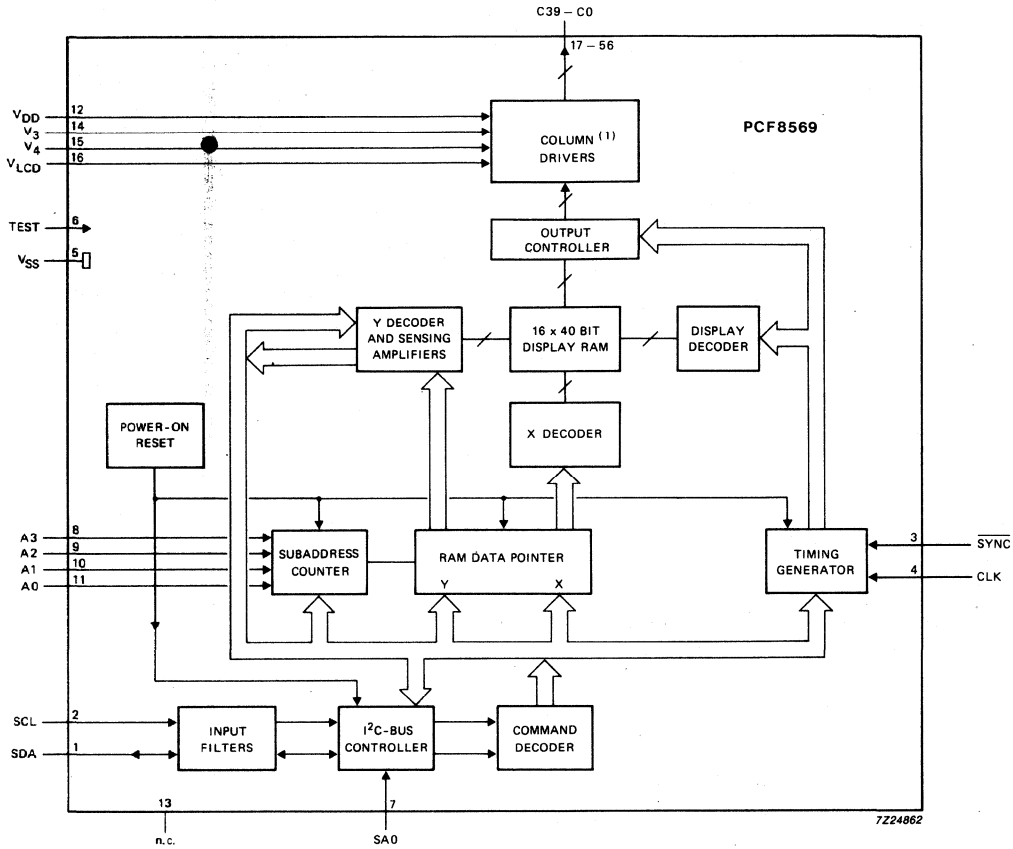
- LCD column driver
- Used in conjunction with the PCF8568 or PCF8578, this device forms part of a chip set capable of driving up to 20 480 dots.
- 40 column outputs
- Selectable multiplex rates; 1:8 or 1:16
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications
- 640-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack or 64-lead tab module

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8569T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8569V: 64-lead tape-automated-bonding (tab) module (SOT267).



(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram (pin numbers shown for VSO56; SOT190).

DEVELOPMENT DATA

PINNING

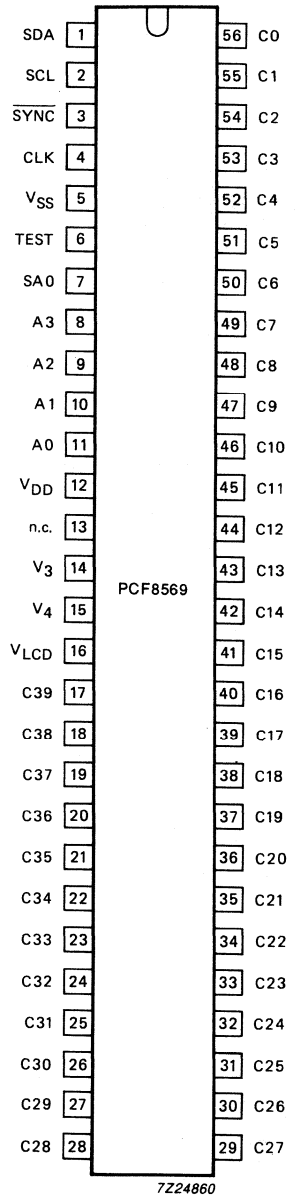
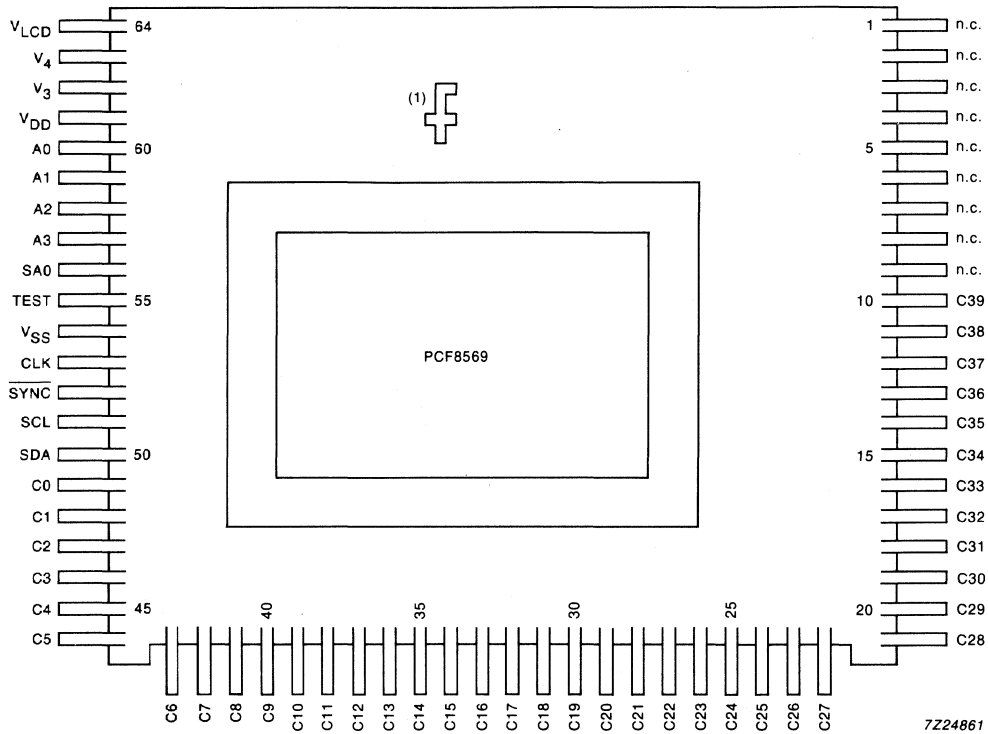


Fig.2 (a) Pinning diagram: VSO56; SOT190.

PINNING (continued)



(1) Orientation mark.

Fig.2 (b) Pinning diagram: SOT267.

mnemonic	pin number		description
	SOT190	SOT267	
SDA	1	50	I^2C-bus serial data line
SCL	2	51	I^2C-bus serial clock line
$\overline{SYNC}$	3	52	cascade synchronization input
CLK	4	53	external clock input
V_{SS}	5	54	ground (logic)
TEST	6	55	test pin (connect to V_{SS})
SA0	7	56	I^2C-bus slave address input (bit 0)
A3 to A0	8 to 11	57 to 60	I^2C-bus subaddress inputs
V_{DD}	12	61	positive supply voltage
n.c.	13 *	1 - 9	not connected
V_3 to V_4	14 to 15	62 to 63	LCD bias voltage inputs
V_{LCD}	16	64	LCD supply voltage
C39 to C0	17 to 56	10 to 49	LCD column driver outputs

DEVELOPMENT DATA

* Do not connect, this pin is reserved.

DC CHARACTERISTICS

V_{DD} = 2.5 V to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
LCD supply voltage		V_{LCD}	V_{DD} −9	–	V_{DD} −3.5	V
Supply current	note 1; f_{CLK} = 2 kHz	I_{DD1}	–	9	20	μA
Power-on reset level	note 2	V_{POR}	–	1.3	1.8	V
Logic						
Input voltage LOW		V_{IL}	V_{SS}	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Leakage current at SDA, SCL, $\overline{SYNC}$, CLK, TEST, SA0, A0, A1, A2 and A3	V_I = V_{DD} or V_{SS}	I_{L1}	−1	–	1	μA
SDA output current LOW	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL}	3	–	–	mA
Input capacitance	note 3	C_I	–	–	5	pF
LCD outputs						
Leakage current at V_3 to V_4	V_I = V_{DD} or V_{LCD}	I_{L2}	−2	–	2	μA
DC component of LCD drivers C0 to C39		± V_{DC}	–	20	–	mV
Output resistance at C0 to C39	note 4	R_{COL}	–	3	6	kΩ

DEVELOPMENT DATA

AC CHARACTERISTICS (note 5)

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Clock frequency	50% duty factor	f_{CLK}	–	*	10	kHz
Driver delays	$V_{DD} - V_{LCD}$ = 9 V; with test loads	t_{PLCD}	–	–	100	μs
I²C-bus						
SCL clock frequency		f_{SCL}	–	–	100	kHz
Tolerable spike width on bus		t_{SW}	–	–	100	ns
Bus free time		t_{BUF}	4.7	–	–	μs
Start condition set-up time	repeated start codes only	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time		$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time		t_{LOW}	4.7	–	–	μs
SCL HIGH time		t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time		t_r	–	–	1.0	μs
SCL and SDA fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop condition set-up time		$t_{SU;STO}$	4.0	–	–	μs

* Typically 0.9 to 3.3 kHz.

Notes to the characteristics

1. Outputs are open; inputs at V_{DD} or V_{SS}; I^2C-bus inactive; clock with 50% duty factor.
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled; not 100% tested.
4. Resistance measured between output terminal (C0 to C39) and bias input (V_3 to V_4, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 1):

   $V_{OP} = V_{DD} - V_{LCD} = 9$ V;

   $V_3 - V_{LCD} \geqslant 4.70$ V; $V_4 - V_{LCD} \leqslant 4.30$ V; $I_{LOAD} = 100\ \mu$A.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

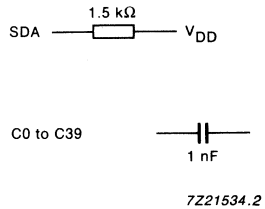


Fig.16 Test loads.

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

128 X 8-BIT/256 X 8-BIT STATIC RAMS WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8570, PCF8570C and PCF8571 are low-power static CMOS RAMs. The PCF8570 and PCF8570C are organized as 256 words by 8-bits and the PCF8571 is organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1 and A2 are used for hardware address, allowing the use of up to eight devices connected to the bus without additional hardware. For system expansion over 8 devices the PCF8570/71 can be used in conjunction with the PCF8750C which has an alternative slave address for memory extension up to 16 devices.

Features

- Operating supply voltage 2.5 V to 6 V
- Low data retention voltage min. 1.0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
- Radio and television — channel presets
- Video cassette recorder — channel presets
- General purpose — RAM expansion for the microcontroller families MAB8400, PCF84CXX and most other microcontrollers

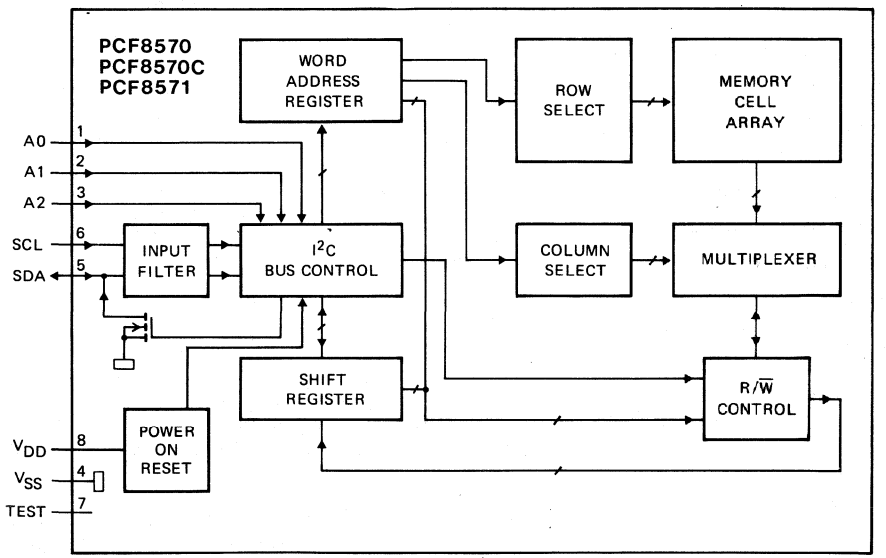


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8570/PCF8570C/PCF8571/P: 8-lead DIL; plastic (SOT97).
PCF8570/PCF8570C/PCF8571/T: 8-lead mini-pack (SO8L; SOT176C).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line (I²C-bus)
6	SCL	serial clock line (I²C-bus)
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 12 and 13)
8	V_{DD}	positive supply

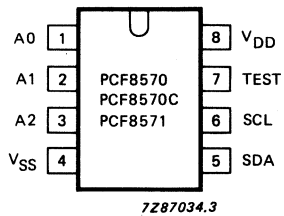


Fig.2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.8	+8.0	V
Input voltage range	V_I	−0.8	V_{DD} + 0.8	V
DC input current	$\pm I_I$	–	10	mA
DC output current	$\pm I_O$	–	10	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; $\pm I_{SS}$	–	50	mA
Total power dissipation	P_{tot}	–	300	mW
Power dissipation per output	P_O	–	50	mW
Operating ambient temperature range	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
Supply current	$V_I = V_{DD}$ or V_{SS}					
operating	f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
standby	f_{SCL} = 0 Hz	I_{DDO}	–	–	15	μA
	T_{amb} = −25 to +70 °C	I_{DDO}	–	–	5	μA
Power-on reset level	note 1	V_{POR}	1.5	1.9	2.3	V
Inputs, input/output SDA						
Input voltage LOW	note 2	V_{IL}	−0.8	–	0.3 V_{DD}	V
Input voltage HIGH	note 2	V_{IH}	0.7 V_{DD}	–	V_{DD} + 0.8	V
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_{LI}\|$	–	–	1	μA
Inputs A0 to A2; TEST						
Input leakage current	$V_I = V_{DD}$ or V_{SS}	$\pm I_{LI}$	–	–	250	nA
Inputs SCL; SDA						
Input capacitance	$V_I = V_{SS}$	C_I	–	–	7	pF
LOW V_{DD} data retention						
Supply voltage for data retention		V_{DDR}	1	–	6	V
Supply current	V_{DDR} = 1 V	I_{DDR}	–	–	5	μA
Supply current	V_{DDR} = 1 V; T_{amb} = −25 to +70 °C	I_{DDR}	–	–	2	μA
Power saving mode	see Figs 12 and 13					
Supply current	TEST = V_{DD}; T_{amb} = 25 °C					
PCF8570/PCF8570C		I_{DDR}	–	50	400	nA
PCF8571		I_{DDR}	–	50	200	nA
Recovery time		t_{HD2}	–	50	–	μs

Notes to the characteristics

1. The power-on reset circuit resets the I²C-bus logic when $V_{DD} < V_{POR}$. The status of the device after a power-on reset condition can be tested by sending the slave address and testing the acknowledge bit.
2. If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow: this current must not exceed ± 0.5 mA.

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, CMOS circuit that functions as a real time clock/calendar with an I^2C-bus interface.
The IC incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred via a serial two-line bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1.2 V nickel cadium battery. The time base is generated from a 32.768 kHz crystal-controlled oscillator.

Features

- Serial input/output I^2C-bus interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32.768 kHz)

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range					
clock (pin 16 to pin 15)	$V_{DD}-V_{SS1}$	1.1	–	6.0	V
I^2C interface (pin 16 to pin 8)	$V_{DD}-V_{SS2}$	2.5	–	6.0	V
Crystal oscillator frequency	f_{osc}	–	32.768	–	kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT38).
PCF8573T: 16-lead mini-pack; plastic (SO16L; SOT162A).

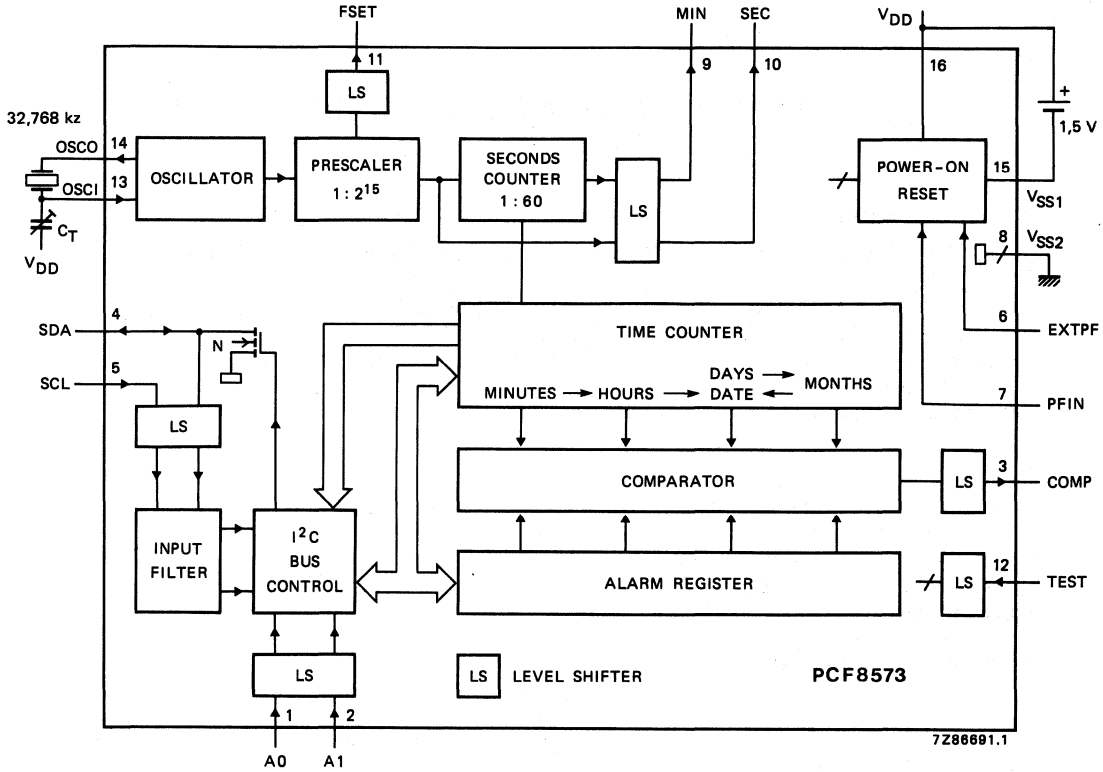


Fig.1 Block diagram.

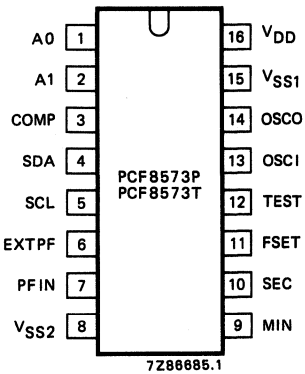


Fig.2 Pinning diagram.

PINNING

1	A0	address input
2	A1	address input
3	COMP	comparator output
4	SDA	serial data line (I^2C-bus)
5	SCL	serial clock line (I^2C-bus)
6	EXTPF	enable power fail flag input
7	PFIN	power fail flag input
8	V_{SS2}	negative supply 2 (I^2C interface)
9	MIN	one pulse per minute output
10	SEC	one pulse per second output
11	FSET	oscillator tuning output
12	TEST	test input; must be connected to V_{SS2} when not in use
13	OSCI	oscillator input
14	OSCO	oscillator input/output
15	V_{SS1}	negative supply 1 (clock)
16	V_{DD}	common positive supply

FUNCTIONAL DESCRIPTION

Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32.768 kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I²C-bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH-to-LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Table 1 Cycle length of the time counter

unit	number of bits	counting cycle	carry for following unit	content of month counter
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days	6	01 to 28	28 → 01	2 (note 1)
			or 29 → 01	2 (note 1)
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note to Table 1

1. Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I²C-bus.

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I²C-bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I²C-bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I²C-bus.

FUNCTIONAL DESCRIPTION (continued)

Power on/power fail detection

If the voltage $V_{DD}-V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with ($V_{DD}-V_{SS1}$) greater than V_{TH1}, or by an externally generated power fail signal for application with ($V_{DD}-V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF	PFIN	function
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

0 : connected to V_{SS1} (LOW)
1 : connected to V_{DD} (HIGH)

The external power fail control operates by absence of the $V_{DD}-V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of $V_{DD}-V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C-bus. A power on reset for the I^2C-bus control is generated on-chip when the supply voltage $V_{DD}-V_{SS2}$ is less than V_{TH2}.

Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD}-V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD}-V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD}-V_{SS2}$ supply voltage. If the voltage $V_{DD}-V_{SS2}$ is absent ($V_{DD} = V_{SS2}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD}-V_{SS2}$ and the $V_{DD}-V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD}-V_{SS2} = 0$.

CHARACTERISTICS OF THE I²C-BUS

The I² C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig.3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

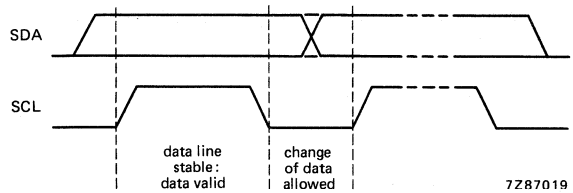


Fig.3 Bit transfer.

Start and stop conditions (see Fig. 4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

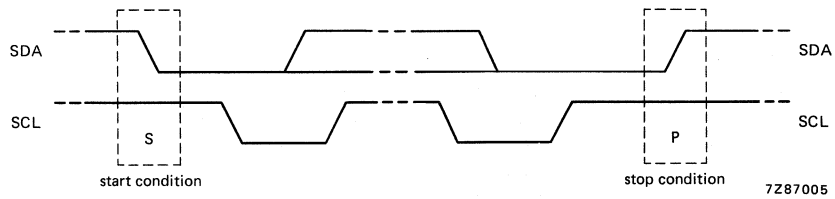


Fig.4 Definition of start and stop conditions.

System configuration (see Fig.5)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

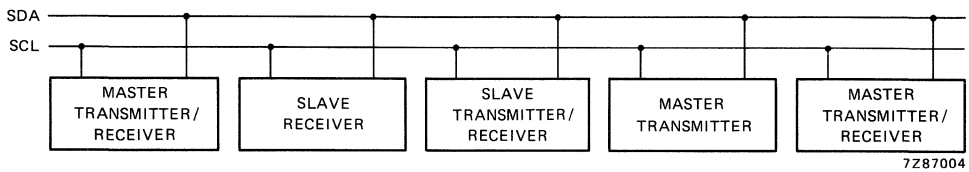


Fig.5 System configuration.

CHARACTERISTICS OF THE I²C-bus (continued)

Acknowledge (see Fig.6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. (See Fig.10 and Fig.11).

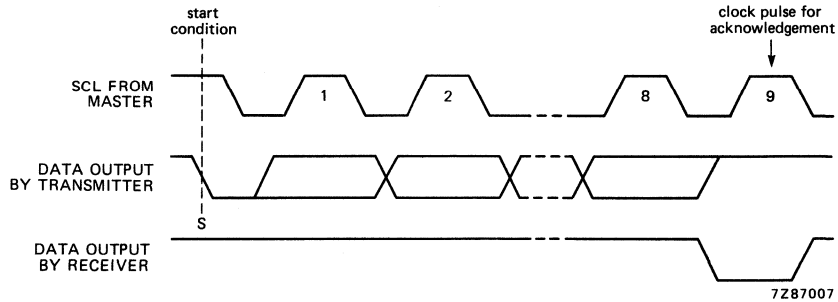


Fig.6 Acknowledgement on the I²C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

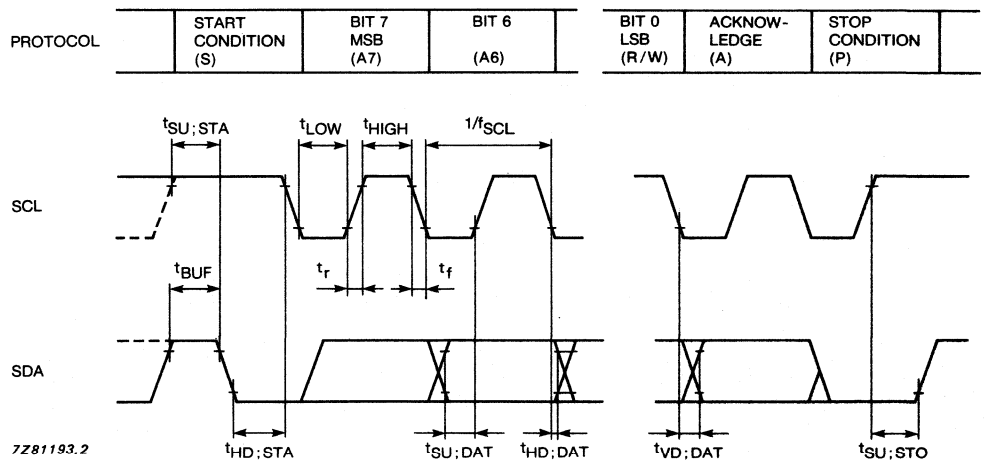


Fig.7 I²C-bus timing diagram.

ADDRESSING

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Fig.8.

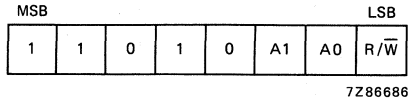


Fig.8 Slave address.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

Clock/calendar READ/WRITE cycles

The I²C-bus configuration for different clock/calendar READ and WRITE cycles is shown in Figs 9, 10 and 11.

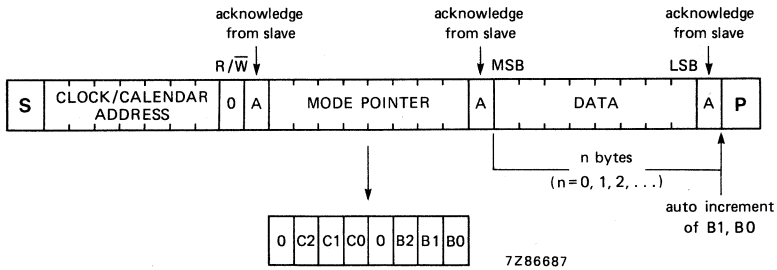


Fig.9 Master transmitter transmits to clock/calendar slave receiver.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nible is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

Table 3 CONTROL-nibble

	C2	C1	C0	function
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (see note)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 s. From the count 30 there is a carry which adjusts the time by max. + 30 s.

Table 4 ADDRESS-nibble

	B2	B1	B0	addressed to:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 5 Placement of BCD digits in the DATA byte

MSB				DATA			LSB	
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Where:

"X" is the don't care bit
"D" is the data bit
Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.

ADDRESSING (continued)

Table 6 Slave receiver acknowledgement

mode pointer								acknowledge on byte		
								address	mode pointer	data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Where:

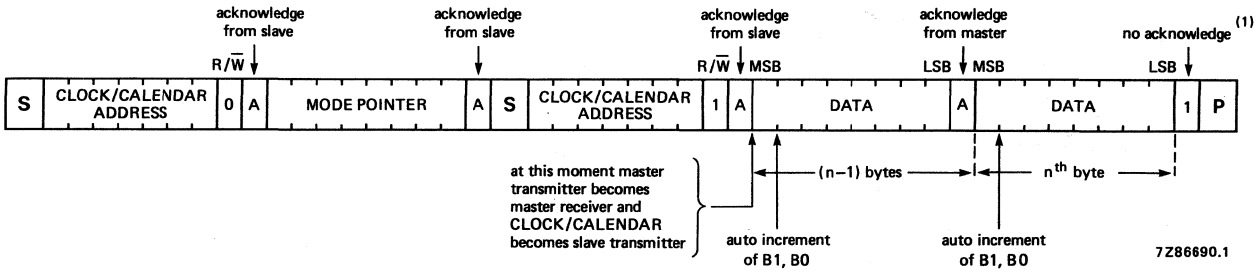
"X" is the don't care bit.

Table 7 Organization of the BCD digits in the DATA byte

MSB DATA LSB								
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	*	**	NODA	COMP	POWF	control/status flags

Where:

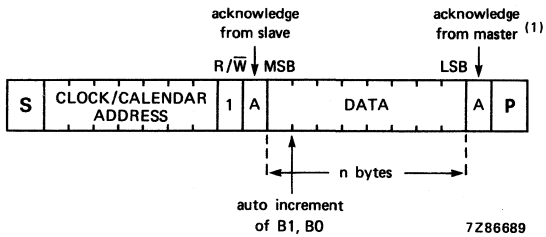
"D" is the data bit
* = minutes
** = seconds.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig.10 Master transmitter reads clock/calendar after setting mode pointer.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig.11 Master reads clock/calendar immediately after first byte.

The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER condition occurs.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	condition	symbol	min.	max.	unit
Supply voltage range					
pin 16 to pin 15		$V_{DD}-V_{SS1}$	−0.3	8.0	V
pin 16 to pin 8		$V_{DD}-V_{SS2}$	−0.3	8.0	V
Voltage input					
pins 4 and 5	note 1	V_I	$V_{SS2}-0.8$	$V_{DD}+0.8$	V
pins 6, 7, 13 and 14		V_I	$V_{SS1}-0.6$	$V_{DD}+0.6$	V
any other pin		V_I	$V_{SS2}-0.6$	$V_{DD}+0.6$	V
Input current		I_I	−	10	mA
Output current		I_O	−	10	mA
Power dissipation per output		P_O	−	100	mW
Total power dissipation		P_{tot}	−	200	mW
Operating ambient temperature range		T_{amb}	−40	+85	°C
Storage temperature range		T_{stg}	−55	+125	°C

Note to the Ratings

1. With input impedance of minimum 500 Ω.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified. Typical values at T_{amb} = +25 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage						
I^2C interface		$V_{DD}-V_{SS2}$	2.5	5.0	6.0	V
clock	$t_{HD;DAT} \geqslant$ 300 ns	$V_{DD}-V_{SS1}$	1.1	1.5	$V_{DD}-V_{SS2}$	V
Supply current						
V_{SS1} (pin 15)	$V_{DD}-V_{SS1}$ = 1.5 V	$-I_{SS1}$	–	3	10	μA
	$V_{DD}-V_{SS1}$ = 5 V	$-I_{SS1}$	–	12	50	μA
V_{SS2} (pin 8)	$V_{DD}-V_{SS2}$ = 5 V; I_O = 0 all outputs	$-I_{SS2}$	–	–	50	μA
Input SCL; input/output SDA						
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Leakage current	$V_I = V_{SS2}$ or V_{DD}	$\|I_L\|$	–	–	1	μA
Input capacitance		C_I	–	–	7	pF
Inputs A0, A1, TEST						
Input voltage LOW		V_{IL}	–	–	0.2 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Input leakage current	$V_I = V_{SS2}$ or V_{DD}	$\pm I_{LI}$	–	–	250	nA
Inputs EXTPF, PFIN						
Input voltage LOW		V_{IL}	0	–	0.2 $V_{DD}-V_{SS1}$	V
Input voltage HIGH		V_{IH}	0.7 $V_{DD}-V_{SS1}$	–	–	V
Input leakage current	$V_I = V_{SS1}$ to V_{DD} T_{amb} = 25 °C;	$\pm I_{LI}$	–	–	1.0	μA
	$V_I = V_{SS1}$ to V_{DD}	$\pm I_{LI}$	–	–	0.1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output SDA						
(n channel open drain)						
Output "ON"	I_O = 3 mA; $V_{DD}-V_{SS2}$ = 2.5 to to 6 V	V_{OL}	–	–	0.4	V
Leakage current	$V_{DD}-V_{SS2}$ = 6 V; V_O = 6 V	$\|I_L\|$	–	–	1	μA
Outputs						
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)						
Output voltage LOW	$V_{DD}-V_{SS2}$ = 2.5 V; I_O = 0.3 mA	V_{OL}	–	–	0.4	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; I_O = 1.6 mA	V_{OL}	–	–	0.4	V
Output voltage HIGH	$V_{DD}-V_{SS2}$ = 2.5 V; $-I_O$ = 0.1 mA	V_{OH}	$V_{DD}-0.4$	–	–	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; $-I_O$ = 0.5 mA	V_{OH}	$V_{DD}-0.4$	–	–	V
Internal threshold voltage						
Power failure detection		V_{TH1}	1	1.2	1.4	V
Power "ON" reset		V_{TH2}	1.5	2.0	2.5	V
Rise and fall times of input signals						
Input EXTPF		t_r, t_f	–	–	1	μs
Input PFIN		t_r, t_f	–	–	∞	μs
Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels						
rise time		t_r	–	–	1	μs
fall time		t_f	–	–	0.3	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Integrated oscillator capacitance		C_{OUT}	–	40	–	pF
Oscillator feedback resistance		R_f	–	3	–	MΩ
Oscillator stability	$\Delta(V_{DD}-V_{SS1})$ = 100 mV; at $V_{DD}-V_{SS1}$ = 1.55 V; T_{amb} = 25 °C	f/f_{osc}	–	2×10^{-7}	–	–
Quartz crystal parameters	f = 32.768 kHz					
Series resistance		R_S	–	–	40	kΩ
Parallel capacitance		C_L	–	10	–	pF
Trimmer capacitance		C_T	5	–	25	pF

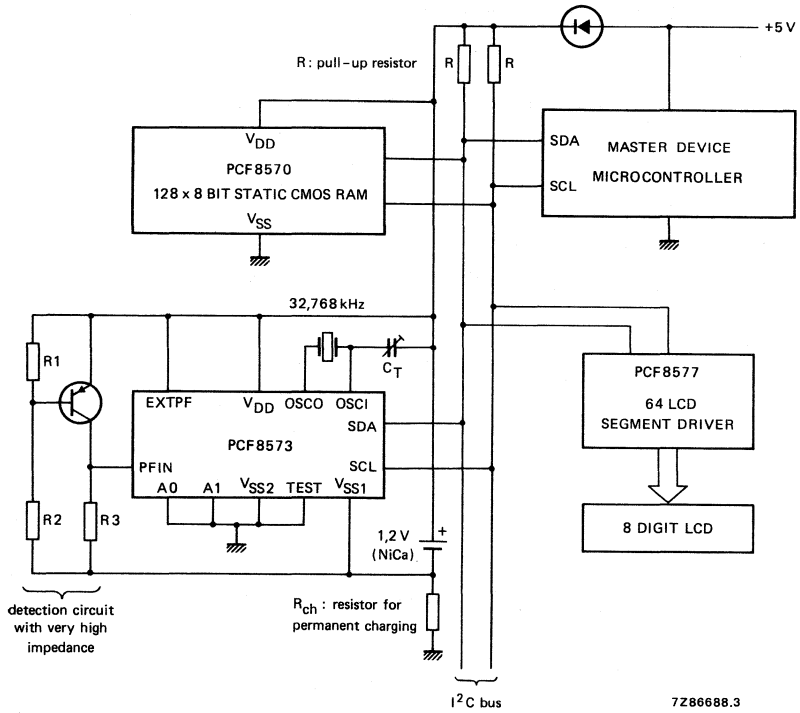


Fig.12 Application example of the PCF8573 clock/calendar.

APPLICATION INFORMATION

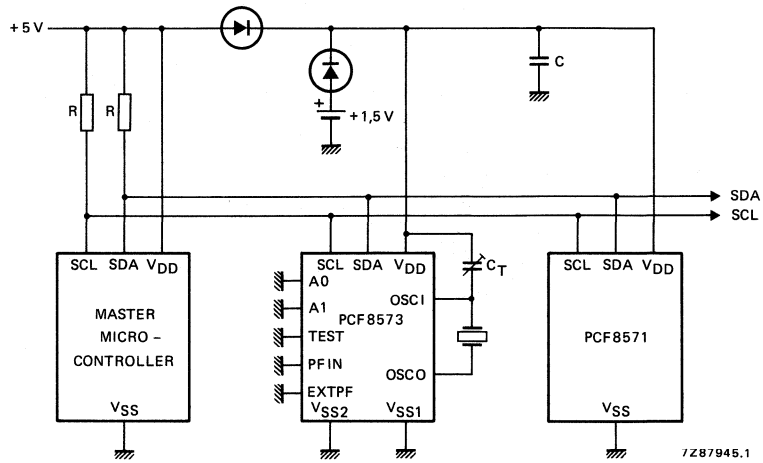


Fig.13 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

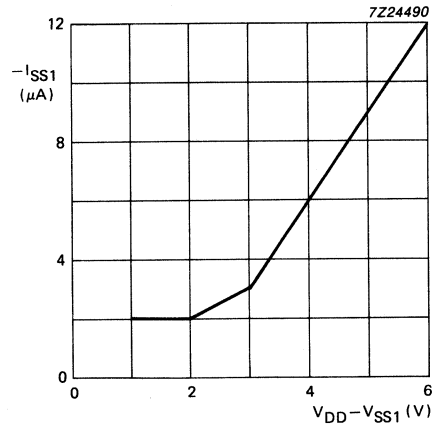


Fig.14 Typical supply current ($-I_{SS1}$) as a function of clock supply voltage ($V_{DD}-V_{SS1}$) at T_{amb} = −40 to +85 °C.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

REMOTE 8-BIT I/O EXPANDER FOR I²C-BUS

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF84CXX microcontroller families via the two-line serial bidirectional bus (I^2C).
It can also interface microcomputers without a serial interface to the I^2C-bus (as a slave function only).
The device consists of an 8-bit quasi-bidirectional port and an I^2C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I^2C-bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I^2C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and the PCF8574A versions differ only in their slave address as shown in Fig.9.

Features

- Operating supply voltage — 2.5 V to 6 V
- Low stand-by current consumption — max. 10 μA
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I^2C-bus
- Peripheral for the MAB8400 and PCF84CXX microcontroller families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)

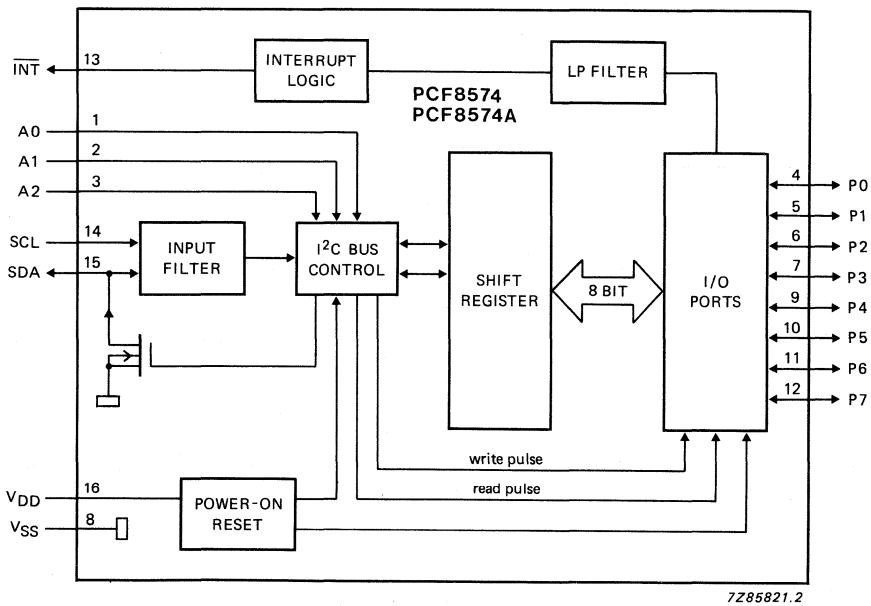


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8574P, PCF8574AP: 16-lead DIL; plastic (SOT38).
PCF8574T, PCF8574AT: 16-lead mini-pack; plastic (SO16L; SOT162A).

PINNING

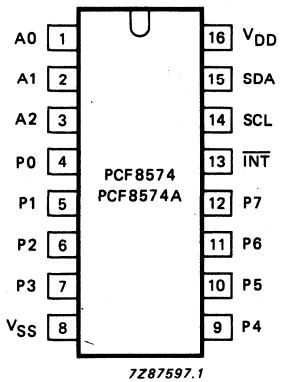


Fig.2 Pinning diagram.

1 to 3	A0 to A2	address inputs
4 to 7 9 to 12	P0 to P3 P4 to P7	8-bit quasi-bidirectional I/O port
8	V_{SS}	negative supply
13	$\overline{INT}$	interrupt output
14	SCL	serial clock line
15	SDA	serial data line
16	V_{DD}	positive supply

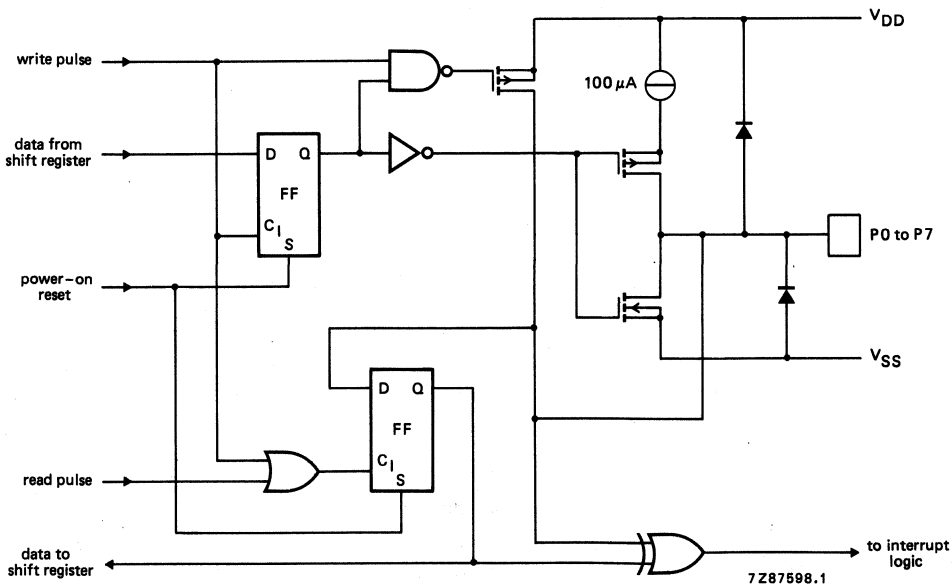


Fig.3 Simplified schematic diagram of each port.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

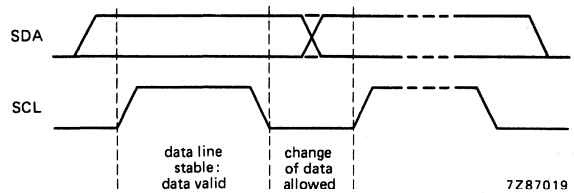


Fig.4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

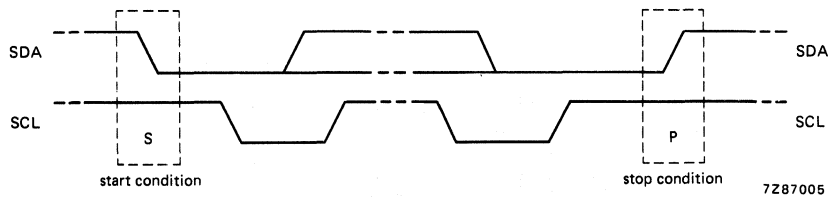


Fig.5 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

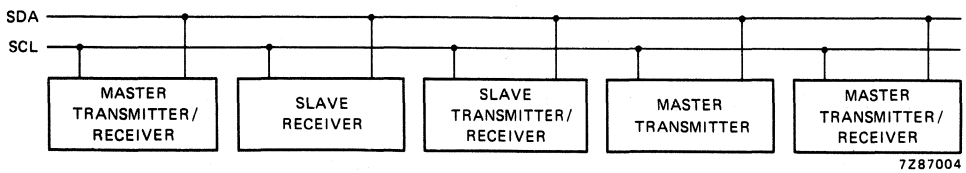


Fig.6 System configuration.

CHARACTERISTICS OF THE I²C-BUS (continued)

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

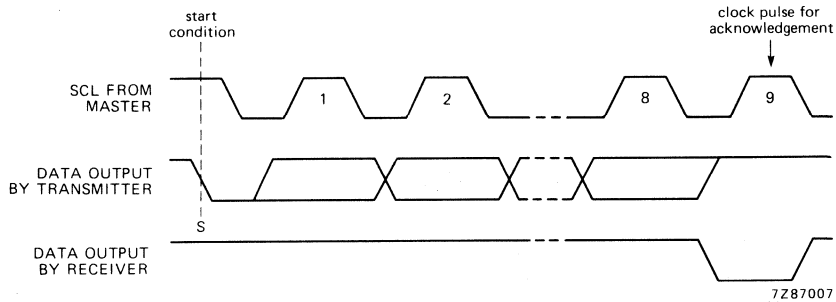


Fig.7 Acknowledgement on the I²C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

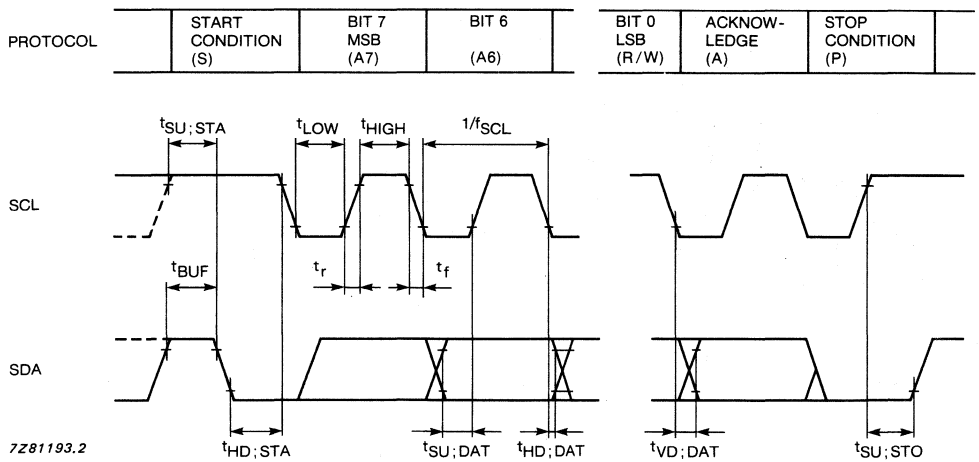
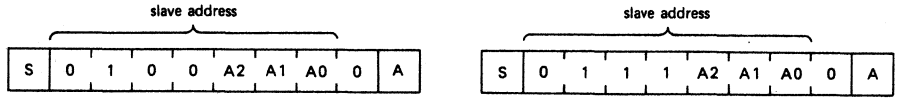


Fig.8 I²C-bus timing diagram.

FUNCTIONAL DESCRIPTION

Addressing (see Figs 9, 10 and 11)



(a) PCF8574. (b) PCF8574A.

Fig.9 PCF8574 and PCF8574A slave addresses.

Each bit of the PCF8574 I/O port can be independently used as an input or an output. Input data is transferred from the port to the microcomputer by the READ mode. Output data is transmitted to the port by the WRITE mode.

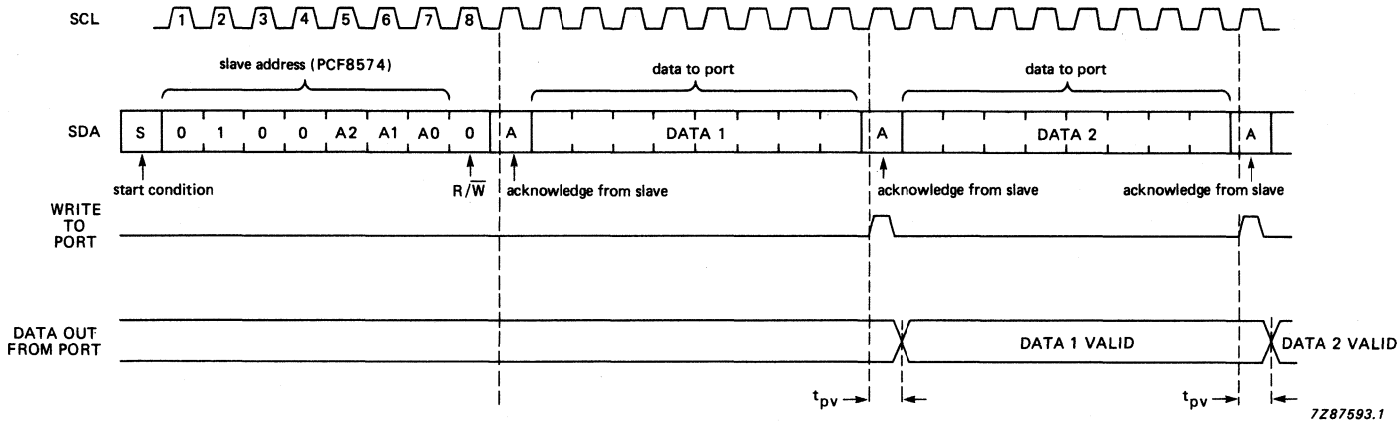


Fig.10 WRITE mode (output port).

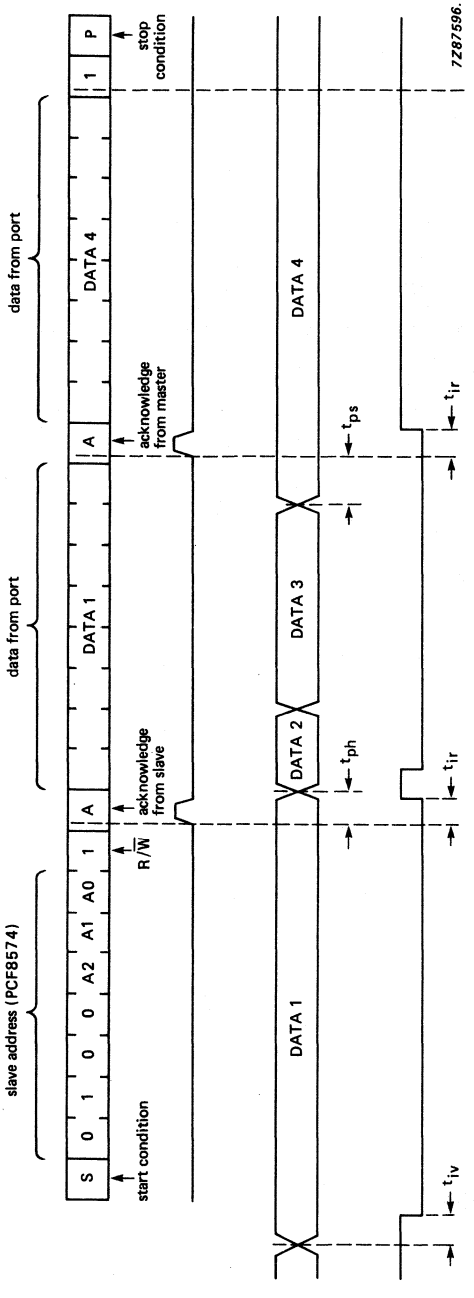


Fig.11 READ mode (input port).

Note

A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Interrupt (see Figs 12 and 13)

The PCF8574/PCF8574A provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcomputer. This gives these chips a type of master function which can initiate an action elsewhere in the system.

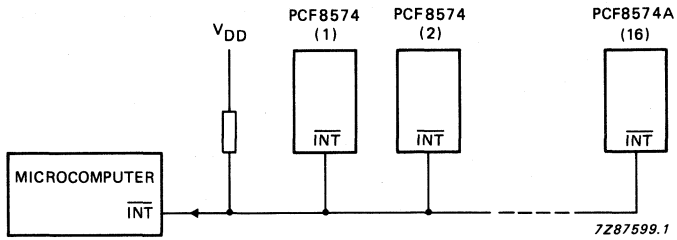


Fig.12 Application of multiple PCF8574s with interrupt.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.
Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt.
Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH-to-LOW transition of the SCL signal.

Each change of the ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$.
Reading from or writing to another device does not affect the interrupt circuit.

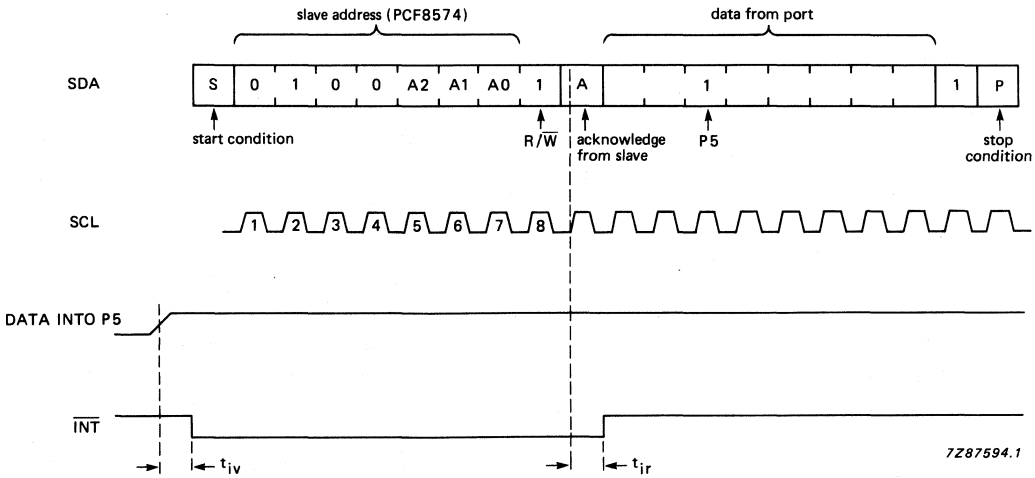


Fig.13 Interrupt generated by a change of input to port P5.

FUNCTIONAL DESCRIPTION (continued)

Quasi-bidirectional I/O ports (see Fig.14)

A quasi-bidirectional port can be used as an input or output without the use of a control signal for data direction. At power-on the ports are HIGH. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The ports should be HIGH before being used as inputs.

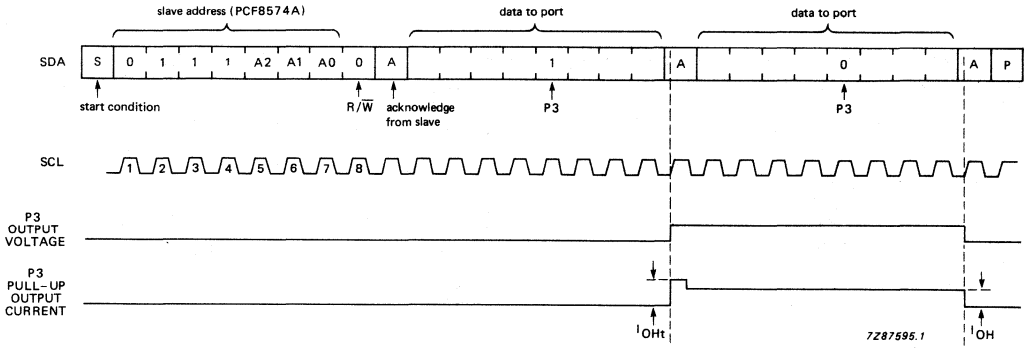


Fig.14 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+ 7.0	V
Input voltage range	V_I	V_{SS} −0.5	V_{DD} + 0.5	V
DC input current	$\pm I_I$	–	20	mA
DC output current	$\pm I_O$	–	25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; $\pm I_{SS}$	–	100	mA
Total power dissipation	P_{tot}	–	400	mW
Power dissipation per output	P_O	–	100	mW
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
Supply current	V_{DD} = 6 V; no load; $V_I = V_{DD}$ or V_{SS}					
operating	f_{SCL} = 100 kHz	I_{DD}	–	40	100	μA
standby		I_{DDO}	–	2.5	10	μA
Power-on reset level	note 1	V_{POR}	–	1.3	2.4	V
Input SCL; input/output SDA						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.5	V
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
Input capacitance (SCL, SDA)	$V_I = V_{SS}$	C_I	–	–	7	pF
I/O ports						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.5	V
Maximum allowed input current through protection diode	$V_I \geqslant V_{DD}$ or $\leqslant V_{SS}$	$\pm I_{IHL}$	–	–	400	μA
Output current LOW	V_{OL} = 1 V; V_{DD} = 5 V	I_{OL}	10	25	–	mA
Output current HIGH	$V_{OH} = V_{SS}$	I_{OH}	30	–	300	μA
Transient pull-up current HIGH during acknowledge (see Fig.14)	$V_{OH} = V_{SS}$; V_{DD} = 2.5 V	$-I_{OHt}$	–	1	–	mA
Input/Output capacitance		$C_{I/O}$	–	–	10	pF
Port timing (see Figs 10 and 11)	$C_L \leqslant$ 100 pF					
Output data valid		t_{pv}	–	–	4	μs
Input data set-up		t_{ps}	0	–	–	μs
Input data hold		t_{ph}	4	–	–	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Interrupt $\overline{INT}$						
Output current LOW	V_{OL} = 0.4 V	I_{OL}	1.6	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
$\overline{INT}$ timing (see Figs 11 and 13)	$C_L \leqslant 100$ pF					
Input data valid		t_{iv}	–	–	4	μs
Reset delay		t_{ir}	–	–	4	μs
Select inputs A0, A1, A2						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.5	V
Input leakage current	pin at V_{DD} or V_{SS}	$\|I_L\|$	–	–	250	nA

Note to the characteristics

1. The power-on reset circuit resets the I²C-bus logic with $V_{DD} < V_{POR}$ and sets all ports to logic 1 (with current source to V_{DD}).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with the 24-segment LCD driver PCF8566
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO56) or 64-lead tape-automated-bonding (TAB) module (SOT267A)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8576U: uncased chip in tray.
PCF8576U/10: chip-on-film frame carrier (FFC).
PCF8576V: 64-lead tape-automated-bonding module (SOT267A).

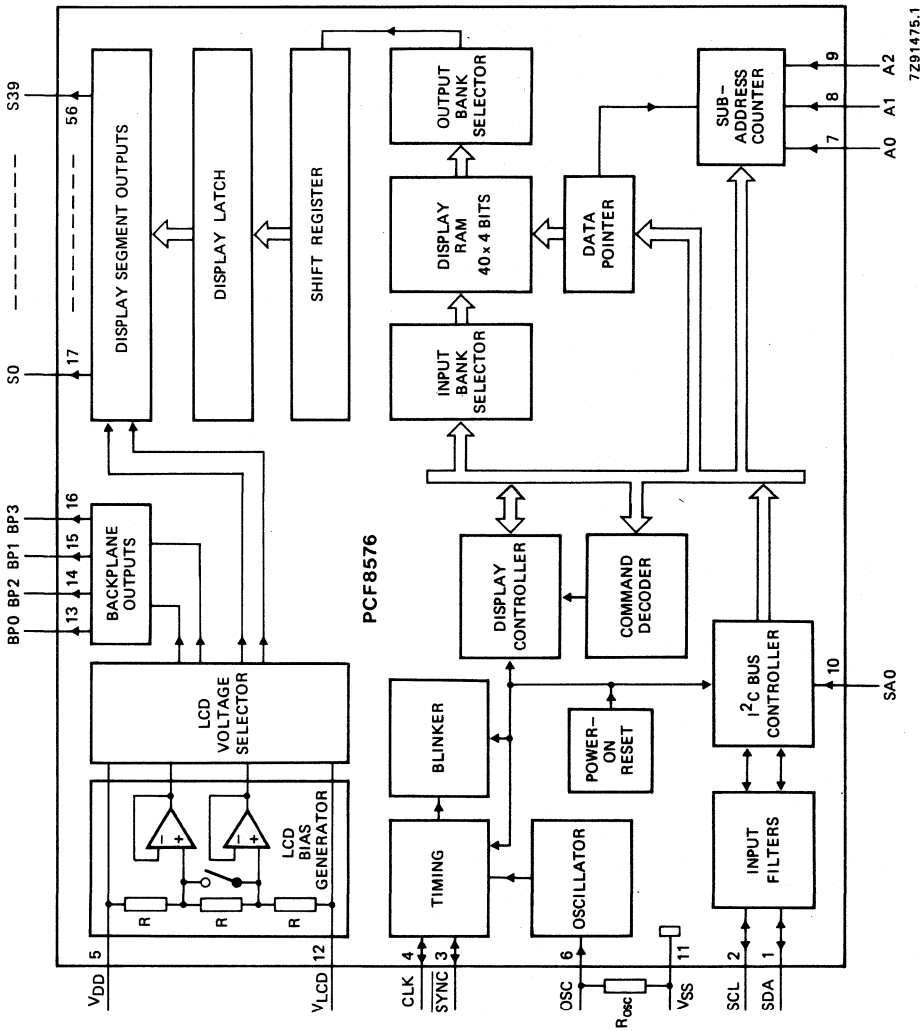


Fig.1 Block diagram; VSO56; SOT190.

PINNING

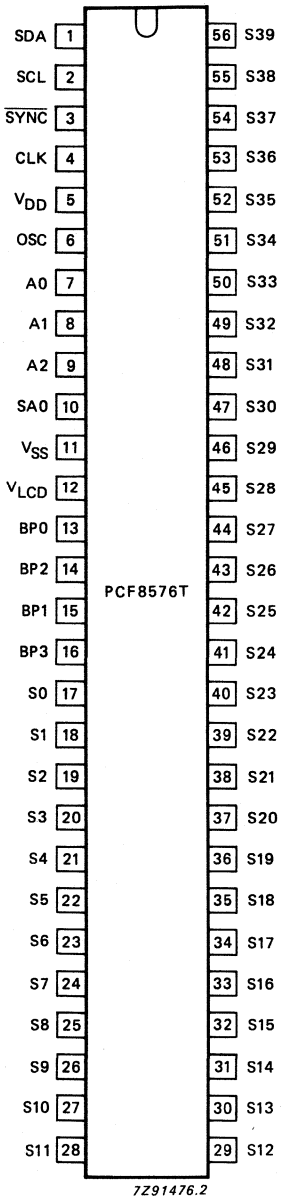
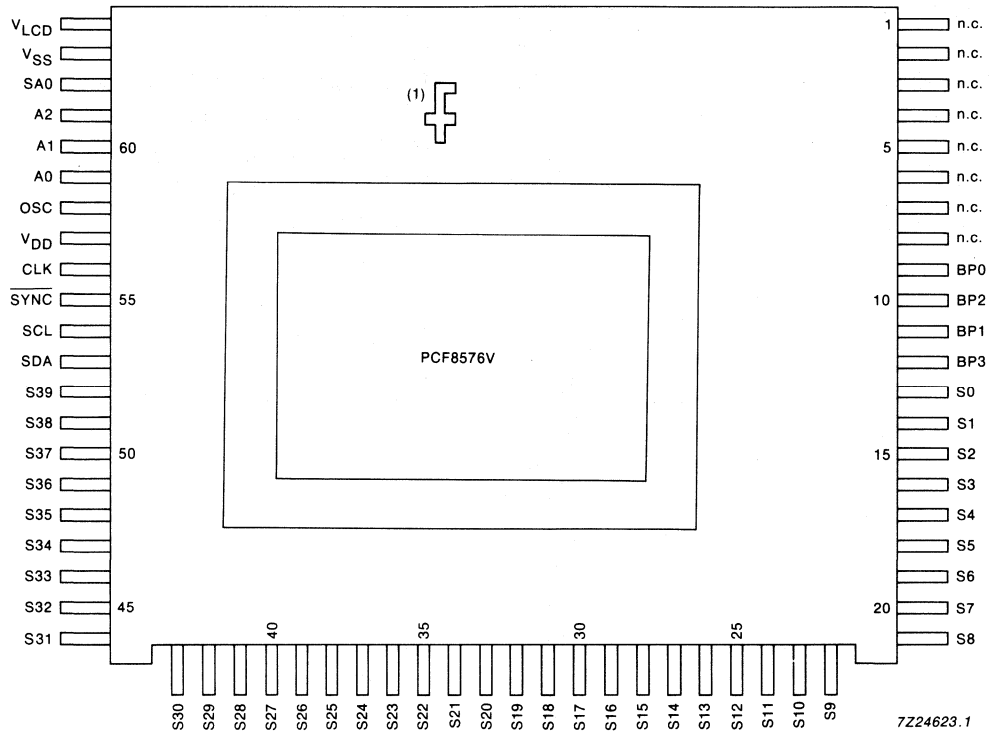


Fig.2(a) Pinning diagram: VSO56; SOT190.

PINNING (continued)



(1) Orientation mark.

Fig.2(b) Pinning diagram; SOT267A.

mnemonic	pin no.		description
	SOT190	SOT267A	
SDA	1	53	I^2C-bus serial data line
SCL	2	54	I^2C-bus serial clock line
$\overline{SYNC}$	3	55	cascade synchronization input
CLK	4	56	external clock input
V_{DD}	5	57	positive supply voltage
OSC	6	58	oscillator input
A0 to A2	7 - 9	59 - 61	I^2C-bus subaddress inputs
SA0	10	62	I^2C-bus slave address input (bit 0)
V_{SS}	11	63	ground (logic)
V_{LCD}	12	64	LCD supply voltage
n.c.		1 - 8	not connected
BP0 to BP3	13 - 16	9 - 12	LCD backplane outputs
S0 to S39	17 - 56	13 - 52	LCD segment outputs

DC CHARACTERISTICS

V_{DD} = 2 V to 9 V; V_{SS} = 0 V; V_{LCD} = V_{DD}−2 V to V_{DD}−9 V; T_{amb} = −40 °C to + 85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2	–	9	V
LCD supply voltage	note 1	V_{LCD}	V_{DD}−9	–	V_{DD}−2	V
Supply current	note 2;					
normal mode power-saving mode	f_{CLK} = 200 kHz V_{DD} = 3.5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz	I_{DD} I_{LP}	– –	– –	180 60	μA μA
Logic						
Input voltage LOW		V_{IL}	V_{SS}	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Output voltage LOW	I_O = 0 mA	V_{OL}	–	–	0.05	V
Output voltage HIGH	I_O = 0 mA	V_{OH}	V_{DD}−0.05	–	–	V
Output current LOW CLK; $\overline{SYNC}$	V_{OL} = 1 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH CLK	V_{OH} = 4 V; V_{DD} = 5 V	$-I_{OH}$	1	–	–	mA
Output current LOW SDA; SCL	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current SA0; A0 to A2; CLK; SDA; SCL OSC	 V_I = V_{SS} or V_{DD} V_I = V_{DD}	 $\pm I_{L1}$ $\pm I_{L2}$	 – –	 – –	 1 1	 μA μA
Pull-up resistor ($\overline{SYNC}$)		R_{SYNC}	20	50	150	kΩ
Power-on reset level	note 3	V_{POR}	–	1.0	1.6	V
Tolerable spike width on bus		t_{SW}	–	–	100	ns
Input capacitance	note 4	C_I	–	–	7	pF
LCD outputs						
DC voltage component BP0 to BP3 S0 to S39	 C_{BP} = 35 nF C_S = 5 nF	 $\pm V_{BP}$ $\pm V_S$	 – –	 20 20	 – –	 mV mV
Output impedance BP0 to BP3 S0 to S39	note 5 V_{LCD} = V_{DD}−5 V V_{LCD} = V_{DD}−5 V	 R_{BP} R_S	 – –	 – –	 5 7.5	 kΩ kΩ

AC CHARACTERISTICS (note 6)

V_{DD} = 2 V to 9 V; V_{SS} = 0 V; V_{LCD} = V_{DD}−2 V to V_{DD}−9 V; T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator frequency						
normal mode	V_{DD} = 5 V; note 7 R_{OSC} = 180 kΩ	f_{CLK}	125	185	288	kHz
power-saving mode	V_{DD} = 3.5 V; R_{OSC} = 1.2 MΩ	f_{CLKLP}	21	31	48	kHz
CLK HIGH time		t_{CLKH}	1	–	–	μs
CLK LOW time		t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay		t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time		t_{SYNCL}	1	–	–	μs
Driver delays with test loads	V_{LCD} = V_{DD}−5 V	t_{PLCD}	–	–	30	μs
I²C-bus						
Bus free time		t_{BUF}	4.7	–	–	μs
Start condition hold time		$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time		t_{LOW}	4.7	–	–	μs
SCL HIGH time		t_{HIGH}	4.0	–	–	μs
Start condition set-up time (repeated start code only)		$t_{SU;STA}$	4.7	–	–	μs
Data hold time		$t_{HD;DAT}$	0	–	–	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Rise time		t_r	–	–	1	μs
Fall time		t_f	–	–	300	ns
Stop condition set-up time		$t_{SU;STO}$	4.0	–	–	μs

Notes to the characteristics

1. $V_{LCD} \leqslant V_{DD}$−3 V for 1/3 bias.
2. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C-bus inactive.
3. Resets all logic when $V_{DD} < V_{POR}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.
6. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
7. At $f_{CLK} < 125$ kHz, I²C-bus maximum transmission speed is derated.

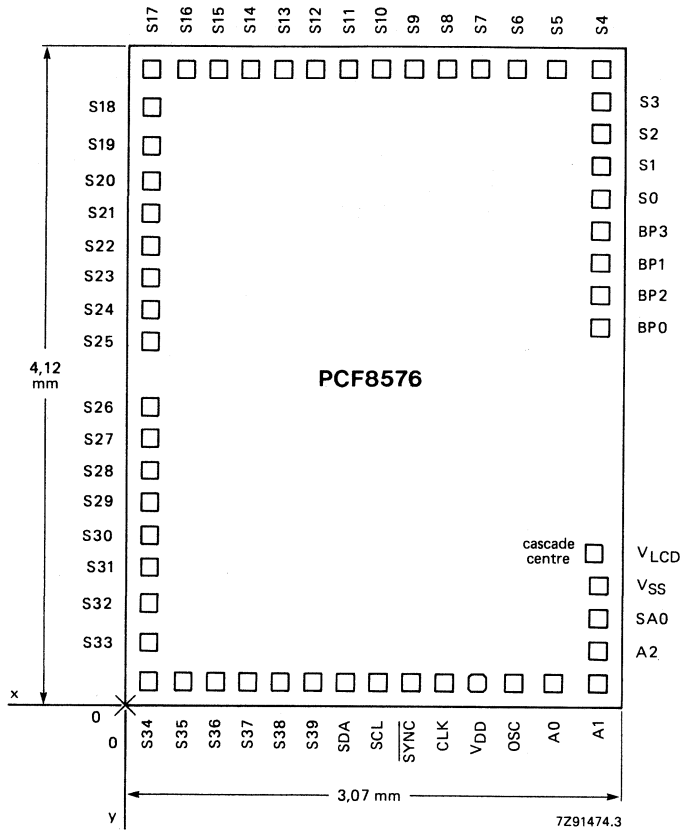


Fig.27 PCF8576 bonding pad locations.

APPLICATION INFORMATION

Bonding pad locations

All x/y coordinates are referenced to left-hand bottom corner (0/0, Fig.27).

Dimensions in μm

pad	x	y	
S34	160	160	bottom
S35	380		
S36	580		
S37	780		
S38	980		
S39	1180		
SDA	1380		
SCL	1580		
$\overline{SYNC}$	1780		
CLK	1980		
V_{DD}	2180		
OSC	2400		
A0	2640		
A1	2910	160	bottom
S17	160	3960	top
S16	380		
S15	580		
S14	780		
S13	980		
S12	1180		
S11	1380		
S10	1580		
S9	1780		
S8	1980		
S7	2180		
S6	2400		
S5	2640		
S4	2910	3960	top

pad	x	y	
S33	160	400	left
S32		640	
S31		860	
S30		1060	
S29		1260	
S28		1460	
S27		1660	
S26		1860	
S25		2260	
S24		2460	
S23		2660	
S22		2860	
S21		3060	
S20		3260	
S19		3480	
S18	160	3720	left
A2	2910	360	right
SA0		560	
V_{SS}	2910	760	
V_{LCD}	2880	960	
BP0	2910	2360	
BP2		2560	
BP1		2760	
BP3		2960	
S0		3160	
S1		3360	
S2		3560	
S3	2910	3760	right

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

LCD DIRECT / DUPLEX DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).
The PCF8577 and PCF8577C differ from the PCF8577A and PCF8577CA only in their slave addresses.
The PCF8577C/77CA is a low-voltage version of the PCF8577/77A.

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Opering supply voltage:
  PCF8577/77A: 2.5 to 9 V
  PCF8577C/77CA: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments (512 segments with PCF8577A/CA)
- Power-on reset blanks display

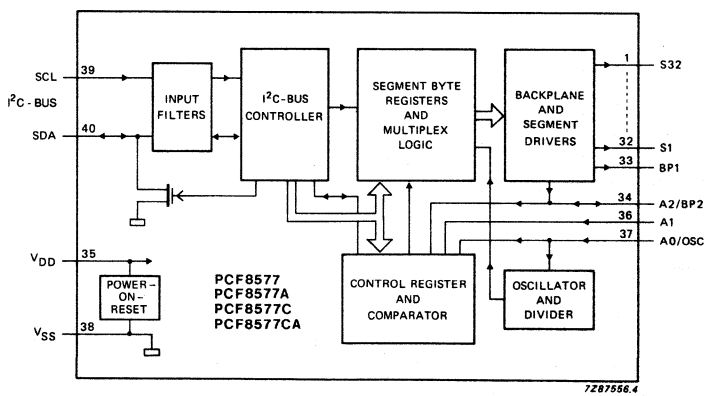


Fig.1 Block diagram.

PAKCAGE OUTLINES

PCF8577P, PCF8577AP PCF8577CP, PCF8577CAP	:	40-lead DIL; plastic (SOT129).
PCF8577T, PCF8577AT PCF8577CT, PCF8577CAT	:	40-lead mini-pack; plastic (VSO40; SOT158A).
PCF8577T, PCF8577AT PCF8577CT, PCF8577CAT	:	in blister tape.
PCF8577U/5 PCF8577CU/5	:	wafer unsawn.
PCF8577U/10 PCF8577CU/10	:	chip on film-frame-carrier (FFC).

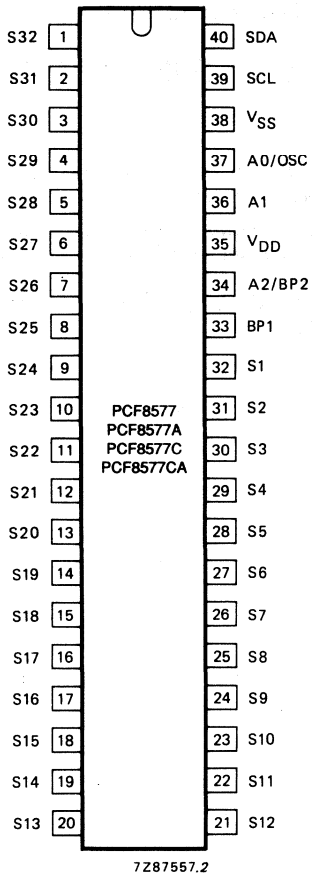


Fig.2 Pinning diagram.

PINNING

Supply

35	V_{DD}	positive supply
38	V_{SS}	negative supply

I^2C-bus

40	SDA	I^2C-bus data line
39	SCL	I^2C-bus clock line

Inputs

36	A1	hardware address line
37	A0/OSC	hardware address line/oscillator pin

Outputs

1 – 32	S32 – S1	segment outputs

Input – Output

34	A2/BP2	harware address line/cascade sync input/backplane output
33	BP1	cascade sync input/backplane output

FUNCTIONAL DESCRIPTION

Hardware subaddress A0, A1, A2

The hardware subaddress lines A0, A1, A2 are used to program the device subaddress for each PCF8577 on the bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

A0/OSC Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.

A1 Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.

A2/BP2 In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.

In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{DD} = 2.5 to 9.0 V (PCF8577/77A) or 2.5 to 6.0 V (PCF8577C/77CA); V_{SS} = 0 V;
T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.*	max.	unit
Supply						
Supply voltage						
PCF8577/77A		V_{DD}	2.5	–	9.0	V
PCF8577C/77CA		V_{DD}	2.5	–	6.0	V
Supply current	non specified inputs at V_{DD} or V_{SS}					
at f_{SCL} = 100 kHz	no load; R_{OSC} = 1 MΩ; C_{OSC} = 680 pF					
PCF8577/77A		I_{DD1}	–	80	250	μA
PCF8577C/77CA		I_{DD1}	–	50	125	μA
at f_{SCL} = 0	no load; R_{OSC} = 1 MΩ; C_{OSC} = 680 pF					
PCF8577/77A		I_{DD2}	–	25	150	μA
PCF8577C/77CA		I_{DD2}	–	25	75	μA
at f_{SCL} = 0	no load; R_{OSC} = 1 MΩ; C_{OSC} = 680 pF; V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD3}	–	25	40	μA
at f_{SCL} = 0	no load; direct mode; A0/OSC = V_{DD}; V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD4}	–	10	20	μA
Power-on reset level	note 1	V_{POR}	–	1.1	2.0	V
Input A0						
Input voltage LOW		V_{IL1}	0	–	0.05	V
Input voltage HIGH		V_{IH1}	V_{DD}−0.05	–	V_{DD}	V
Input A1						
Input voltage LOW		V_{IL2}	0	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH2}	0.7 V_{DD}	–	V_{DD}	V
Input A2						
Input voltage LOW		V_{IL3}	0	–	0.10	V
Input voltage HIGH		V_{IH3}	V_{DD}−0.10	–	V_{DD}	V

* Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.

DC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.*	max.	unit
Inputs SCL; SDA						
Input voltage LOW		V_{IL4}	0	–	0.8	V
Input voltage HIGH						
PCF8577/77A		V_{IH4}	2.0	–	9.0	V
PCF8577C/77CA		V_{IH4}	2.0	–	6.0	V
Input capacitance	note 2	C_I	–	–	7	pF
Output SDA						
Output current LOW	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL}	3.0	–	–	mA
A1; SCL; SDA						
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\pm I_{L1}$	–	–	1	μA
A2/BP2; BP1						
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\pm I_{L2}$	–	–	5	μA
A2/BP2						
Pull-down current	$V_I = V_{DD}$	$-I_{L2}$	–	1.5	5	μA
A0/OSC						
Leakage current	$V_I = V_{DD}$	$-I_{L3}$	–	–	1	μA
Oscillator						
Start-up current	$V_I = V_{SS}$	I_{OSC}	–	1.2	5	μA
LCD outputs						
DC component of LCD driver		$\pm V_{BP}$	–	20	–	mV
Segment output current	V_{DD} = 5 V; note 6					
PCF8577/77A	V_{OL} = 0.4 V	I_{OL1}	0.3	–	–	mA
PCF8577C/77CA	V_{OL} = 0.8 V	I_{OL1}	0.3	–	–	mA
PCF8577/77A	$V_{OH} = V_{DD}-0.4$ V	$-I_{OH1}$	0.3	–	–	mA
PCF8577C/77CA	$V_{OH} = V_{DD}-0.8$ V	$-I_{OH1}$	0.3	–	–	mA
Backplane output resistance (BP1; BP2)	$V_O = V_{SS}$, V_{DD}, $(V_{SS}+V_{DD})/2$; note 3	R_{BP}	–	0.4	5	kΩ

* Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.

AC CHARACTERISTICS (note 4)

V_{DD} = 2.5 to 9.0 V (PCF8577/77A) or 2.5 to 6.0 V (PCF8577C/77CA);
T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.*	max.	unit
Display frequency	C_{OSC} = 680 pF; R_{OSC} = 1 MΩ	f_{LCD}	65	90	120	Hz
Driver delays with test loads	V_{DD} = 5 V	t_{BS}	–	20	100	μs
I²C-bus						
SCL clock frequency		f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	note 5	t_{SW}	–	–	100	ns
Bus free time		t_{BUF}	4.7	–	–	μs
Start condition set-up time		$t_{SU;STA}$	4.0	–	–	μs
Start condition hold time		$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time		t_{LOW}	4.7	–	–	μs
SCL HIGH time		t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time		t_r	–	–	1.0	μs
SCL and SDA fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop condition set-up time		$t_{SU;STO}$	4.0	–	–	μs

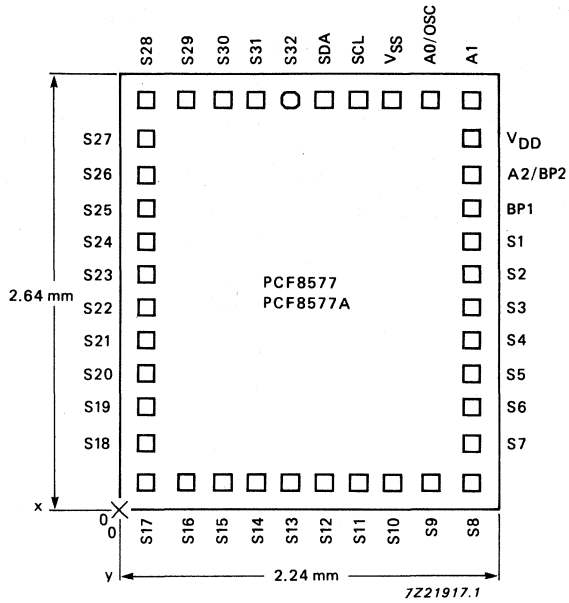
DEVELOPMENT DATA

Notes to the characteristics

1. Resets all logic when $V_{DD} < V_{POR}$.
2. Periodically sampled, not 100% tested.
3. Outputs measured one at a time; V_{DD} = 5 V; I_{load} = 100 μA.
4. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
5. PCF8577C/CA 25 °C only.
6. Outputs measured one at a time.

* Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS PCF8577/77A



Chip area: 5.91 mm^2

Bonding pad dimensions: 120 μm x 120 μm

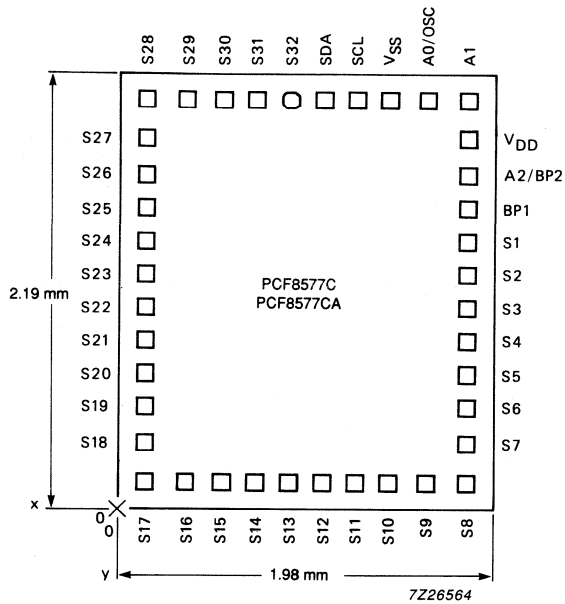
Fig.18 Bonding pad locations; PCF8577/PCF8577A.

Table 3 Bonding pad locations; PCF8577/77A (dimensions in μm)

All x/y coordinates are referenced to bottom left corner, see Fig.18.

pad	X	Y	pad	X	Y
S32	1020	2480	S12	1220	160
S31	820	2480	S11	1420	160
S30	620	2480	S10	1620	160
S29	400	2480	S9	1840	160
S28	160	2480	S8	2080	160
S27	160	2240	S7	2080	400
S26	160	2020	S6	2080	620
S25	160	1820	S5	2080	820
S24	160	1620	S4	2080	1020
S23	160	1420	S3	2080	1220
S22	160	1220	S2	2080	1420
S21	160	1020	S1	2080	1620
S20	160	820	BP1	2080	1820
S19	160	620	A2/BP2	2080	2020
S18	160	400	V_{DD}	2080	2240
S17	160	160	A1	2080	2480
S16	400	160	A0/OSC	1840	2480
S15	620	160	V_{SS}	1620	2480
S14	820	160	SCL	1420	2480
S13	1020	160	SDA	1220	2480

CHIP DIMENSIONS AND BONDING PAD LOCATIONS PCF8577C/77CA



Chip area: 4.34 mm²

Bonding pad dimensions: 110 μm x 110 μm

Fig.19 Bonding pad locations; PCF8577C/77CA.

Table 4 Bonding pad locations; PCF8577C/77CA (dimensions in μm)

All x/y coordinates are referenced to bottom left corner, see Fig.19.

pad	X	Y	pad	X	Y
S32	904	2036	S12	1075	154
S31	733	2036	S11	1246	154
S30	562	2036	S10	1417	154
S29	391	2036	S9	1588	154
S28	154	2036	S8	1826	154
S27	154	1864	S7	1826	325
S26	154	1693	S6	1826	496
S25	154	1522	S5	1826	667
S24	154	1351	S4	1826	838
S23	154	1180	S3	1826	1009
S22	154	1009	S2	1826	1180
S21	154	838	S1	1826	1351
S20	154	667	BP1	1826	1522
S19	154	496	A2/BP2	1826	1693
S18	154	325	V_{DD}	1826	1846
S17	154	154	A1	1826	2036
S16	391	154	A0/OSC	1588	2036
S15	562	154	V_{SS}	1417	2036
S14	733	154	SCL	1246	2036
S13	904	154	SDA	1075	2036

DEVELOPMENT DATA

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

LCD ROW/COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs, of which 24 are programmable, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40,960 dots possible)
- 40 driver outputs, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8578T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8578V: 64-lead tape-automated-bonding module (SOT267A).
PCF8578U: chip with bumps on-tape.

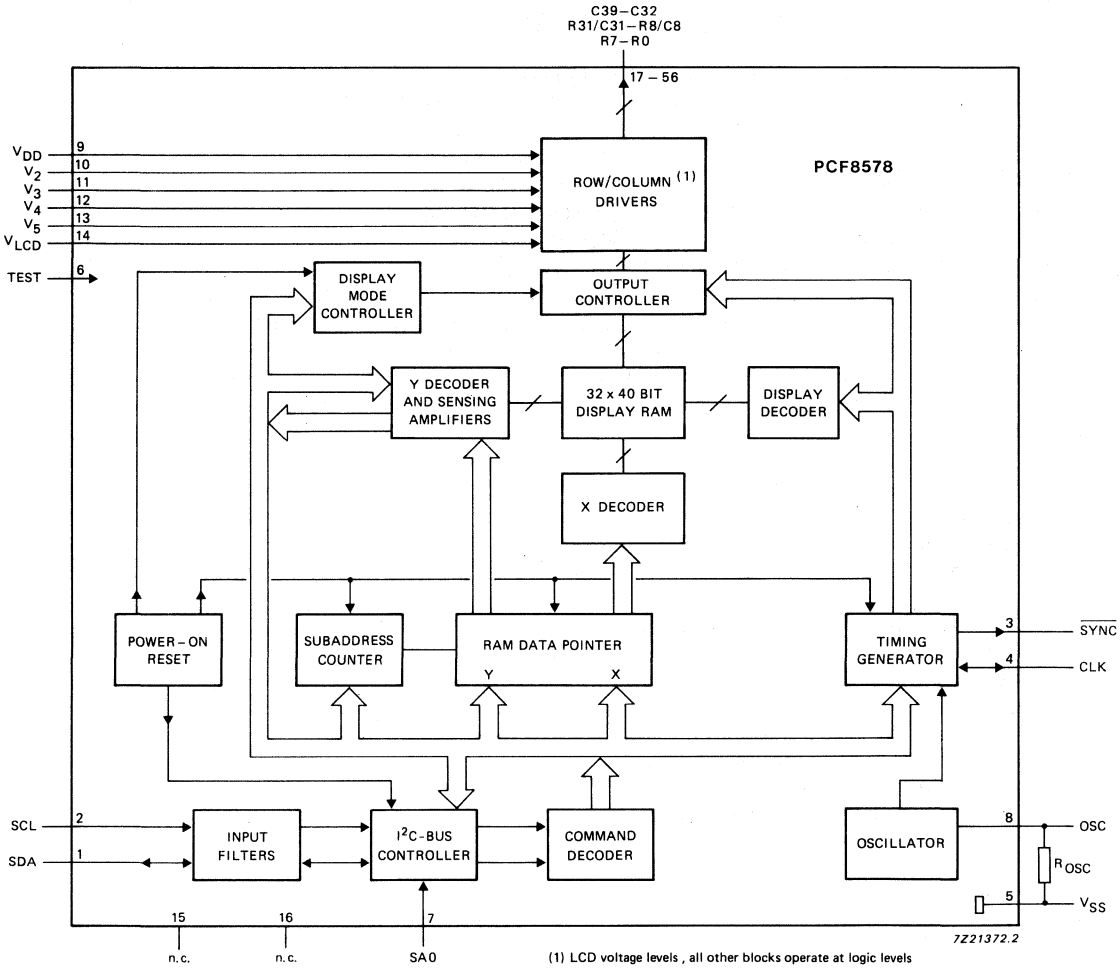


Fig.1 Block diagram.

PINNING

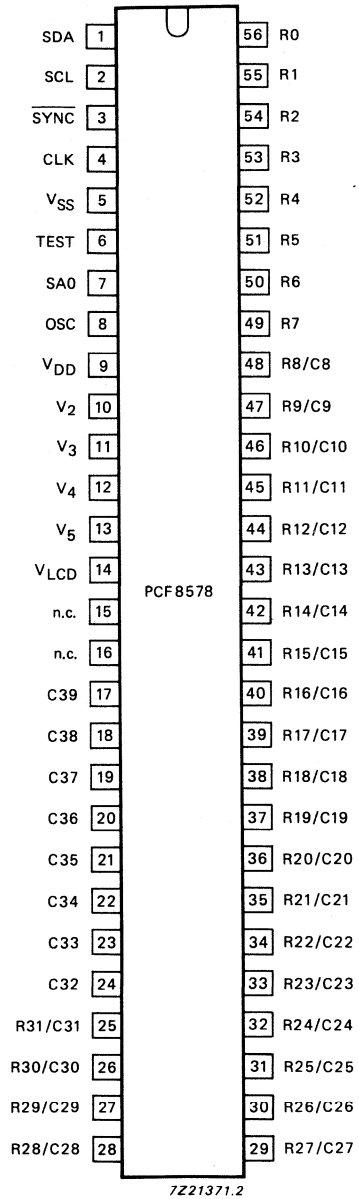
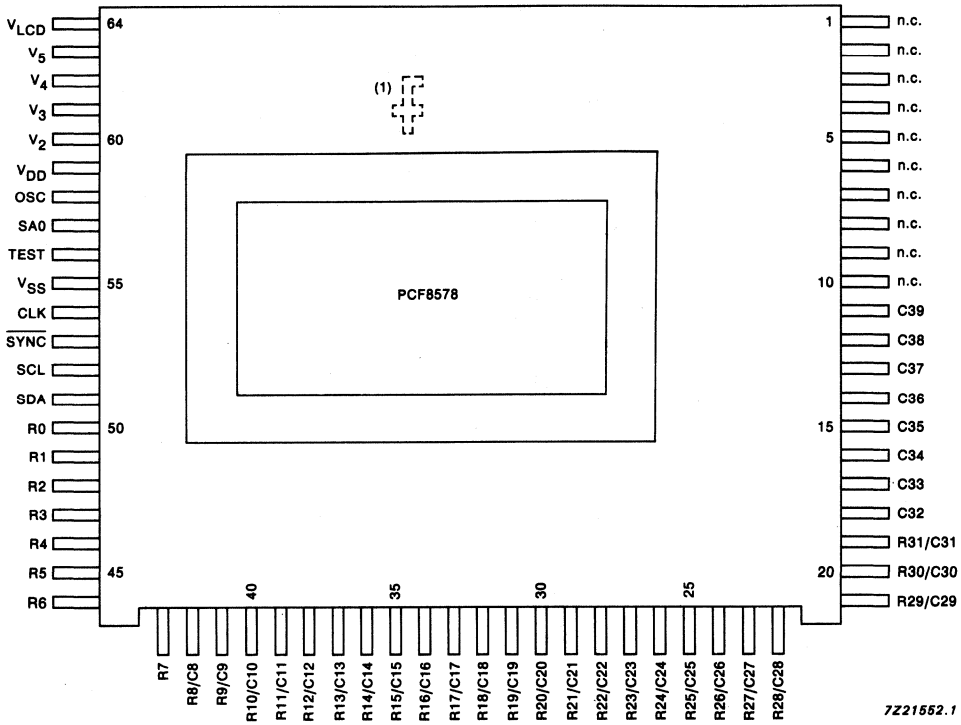


Fig.2 (a) Pinning diagram: VSO56; SOT190.

DEVELOPMENT DATA

PINNING (continued)



(1) Orientation mark.

Fig.2 (b) Pinning diagram; SO121.

mnemonic	pin no.		description
	SOT190	SO121	
SDA	1	51	I^2C-bus serial data line
SCL	2	52	I^2C-bus serial clock line
$\overline{SYNC}$	3	53	cascade synchronization output
CLK	4	54	external clock input/output
V_{SS}	5	55	ground (logic)
TEST	6	56	test pin (connect to V_{SS})
SA0	7	57	I^2C-bus slave address input (bit 0)
OSC	8	58	oscillator input
V_{DD}	9	59	positive supply voltage
V_2 to V_5	10 - 13	60 - 63	LCD bias voltage inputs
V_{LCD}	14	64	LCD supply voltage
n.c.	15 - 16	1 - 10	not connected
C39 to C32	17 - 24	11 - 18	LCD column driver outputs
R31/C31 to R8/C8	25 - 48	19 - 42	LCD row/column driver outputs
R7 to R0	49 - 56	43 - 50	LCD row driver outputs

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{DD} = 2.5 V to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
LCD supply voltage		V_{LCD}	V_{DD} −9	–	V_{DD} −3.5	V
Supply current	note 1;					
external clock	f_{CLK} = 2 kHz	I_{DD1}	–	6	15	μA
internal clock	R_{OSC} = 330 kΩ	I_{DD2}	–	20	50	μA
Power-on reset level	note 2	V_{POR}	0.8	1.3	1.8	V
Logic						
Input voltage LOW		V_{IL}	V_{SS}	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Output current LOW at $\overline{SYNC}$ and CLK	V_{OL} = 1.0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH at $\overline{SYNC}$ and CLK	V_{OH} = 4.0 V; V_{DD} = 5 V	I_{OH1}	–	–	−1	mA
SDA output current LOW	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL2}	3.0	–	–	mA
Leakage current at SDA, SCL, $\overline{SYNC}$, CLK, TEST and SA0	V_I = V_{DD} or V_{SS}	I_{L1}	−1	–	1	μA
Leakage current at OSC	V_I = V_{DD}	I_{L2}	−1	–	1	μA
Input capacitance at SCL and SDA	note 3	C_I	–	–	5	pF
LCD outputs						
Leakage current at V_2 to V_5	V_I = V_{DD} or V_{LCD}	I_{L3}	−2	–	2	μA
DC component of LCD drivers R0 to R7, R8/C8 to R31/C31, and C32 to C39		± V_{DC}	–	20	–	mV
Output resistance at R0 to R7 and R8/C8 to R31/C31	note 4					
	row mode	R_{ROW}	–	1.5	3.0	kΩ
R8/C8 to R31/C31 and C32 to C39	column mode	R_{COL}	–	3	6	kΩ

AC CHARACTERISTICS (note 5)

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = − 40 to + 85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Clock frequency at multiplex rates of 1:8, 1:16 and 1:32	R_{OSC} = 330 kΩ; V_{DD} = 6 V	f_{CLK1}	1.2	2.1	3.3	kHz
1:24		f_{CLK2}	0.9	1.6	2.5	kHz
$\overline{SYNC}$ propagation delay		t_{PSYNC}	–	–	500	ns
Driver delays	V_{DD} − V_{LCD} = 9 V; with test loads	t_{PLCD}	–	–	100	μs
I²C-bus						
SCL clock frequency		f_{SCL}	–	–	100	kHz
Tolerable spike width on bus		t_{SW}	–	–	100	ns
Bus free time		t_{BUF}	4.7	–	–	μs
Start condition set-up time	repeated start codes only	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time		$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time		t_{LOW}	4.7	–	–	μs
SCL HIGH time		t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time		t_r	–	–	1.0	μs
SCL and SDA fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop condition set-up time		$t_{SU;STO}$	4.0	–	–	μs

DEVELOPMENT DATA

Notes to the characteristics

1. Outputs are open; inputs at V_{DD} or V_{SS}; I^2C-bus inactive; external clock with 50% duty factor, (I_{DD1} only).
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled; not 100% tested.
4. Resistance measured between output terminal (R0 to R7, R8/C8 to R31/C31 and C32 to C39) and bias input (V_2 to V_5, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 2):

   $V_{OP} = V_{DD} - V_{LCD} = 9$ V;

   row mode, R0 to R7 and R8/C8 to R31/C31 (row mode):
   $V_2 - V_{LCD} \geqslant 6.65$ V; $V_5 - V_{LCD} \leqslant 2.35$ V; $I_{LOAD} = 150\ \mu A$

   column mode, R8/C8 to R31/C31 (column mode) and C32 to C39:
   $V_3 - V_{LCD} \geqslant 4.70$ V; $V_4 - V_{LCD} \leqslant 4.30$ V; $I_{LOAD} = 100\ \mu A$.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

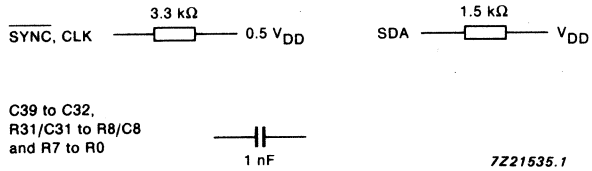
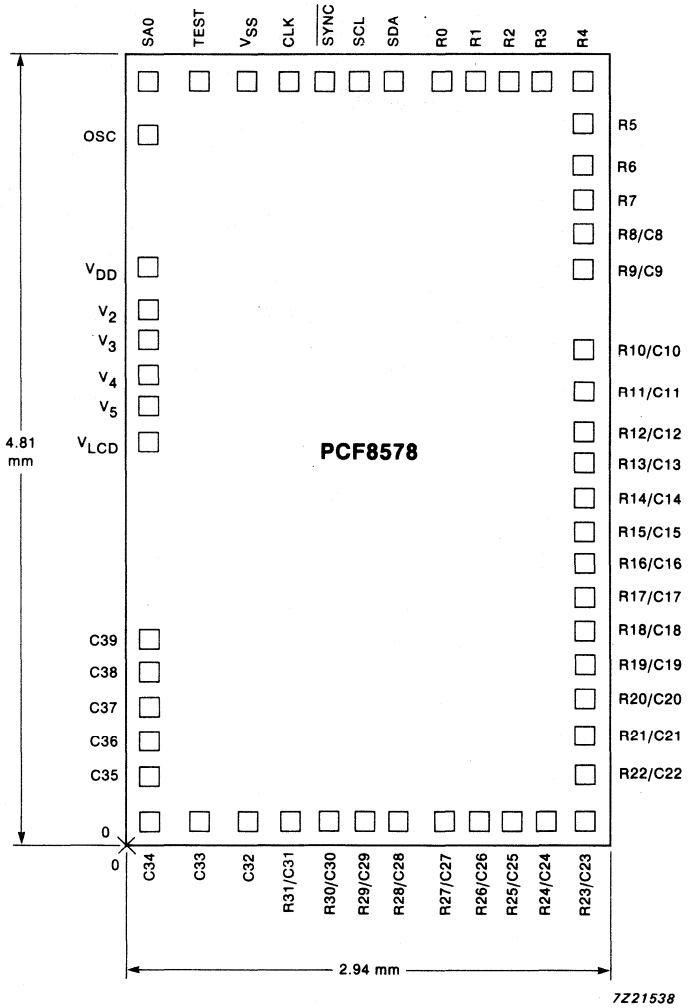


Fig.18 Test loads.

DEVELOPMENT DATA

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 14.14 mm^2
Bonding pad dimensions: 120 μm x 120 μm.

Fig.26 Bonding pad locations.

Table 6 Bonding pad locations (dimensions in μm)

All x/y co-ordinates are referenced to the bottom left corner, see Fig.26.

pad	X	Y	pad	X	Y
SDA	1642	4642	R27/C27	1936	160
SCL	1438	4642	R26/C26	2140	160
$\overline{SYNC}$	1234	4642	R25/C25	2344	160
CLK	1000	4642	R24/C24	2548	160
V_{SS}	742	4642	R23/C23	2776	160
TEST	454	4642	R22/C22	2776	424
SA0	160	4642	R21/C21	2776	670
OSC	160	4318	R20/C20	2776	886
V_{DD}	160	3514	R19/C19	2776	1096
V_2	160	3274	R18/C18	2776	1300
V_3	160	3064	R17/C17	2776	1504
V_4	160	2860	R16/C16	2776	1708
V_5	160	2656	R15/C15	2776	1912
V_{LCD}	160	2452	R14/C14	2776	2116
n.c.	—	—	R13/C13	2776	2320
n.c.	—	—	R12/C12	2776	2524
C39	160	1252	R11/C11	2776	2752
C38	160	1048	R10/C10	2776	3004
C37	160	844	R9/C9	2776	3502
C36	160	628	R8/C8	2776	3706
C35	160	406	R7	2776	3916
C34	160	160	R6	2776	4132
C33	454	160	R5	2776	4378
C32	742	160	R4	2776	4642
R31/C31	1000	160	R3	2548	4642
R30/C30	1234	160	R2	2344	4642
R29/C29	1438	160	R1	2140	4642
R28/C28	1642	160	R0	1936	4642

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs and can drive 32 x 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40,960 dots
- 40 column outputs
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8579T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8579V: 64-lead tape-automated-bonding module (SOT267A).
PCF8579U: chip with bumps on-tape.

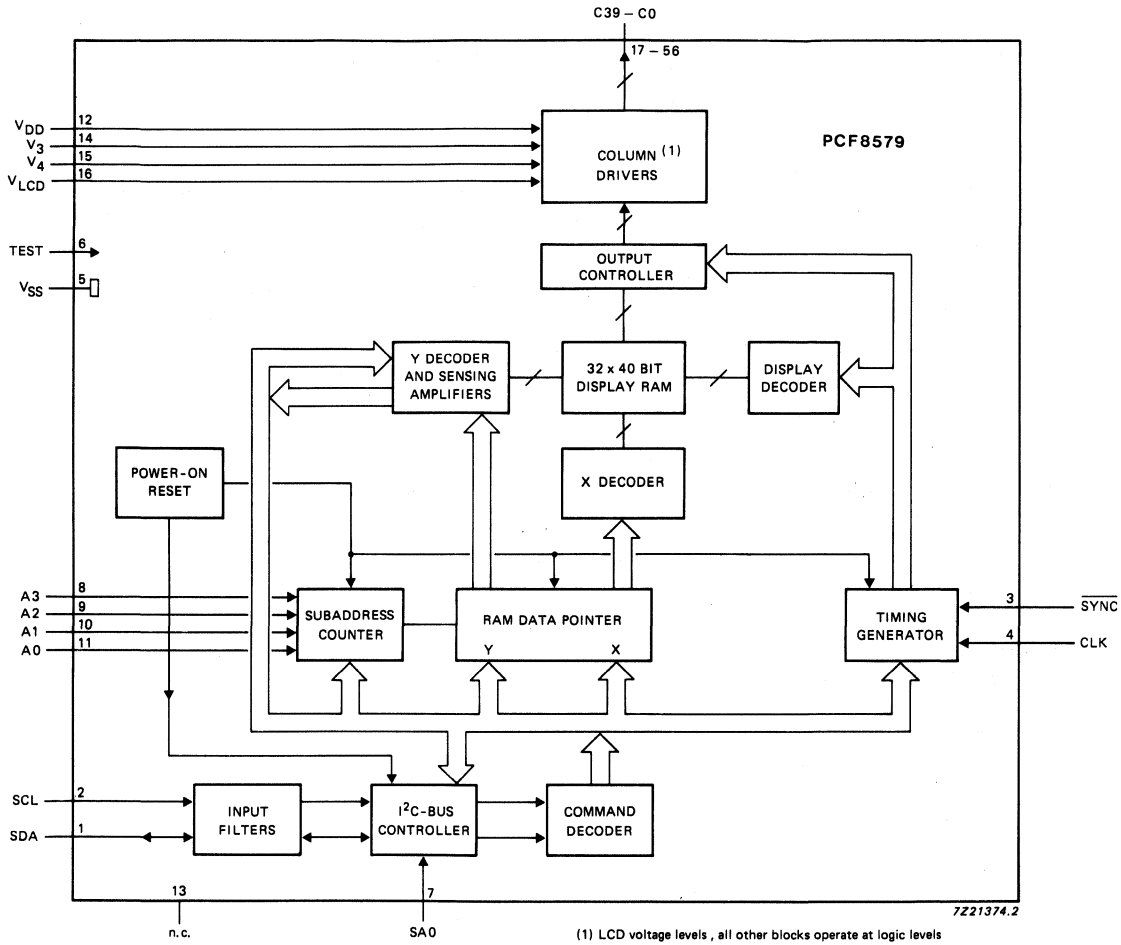


Fig.1 Block diagram.

PINNING

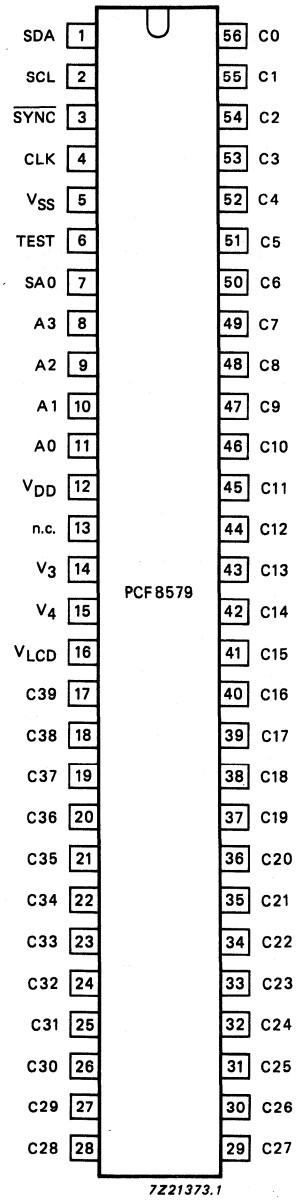
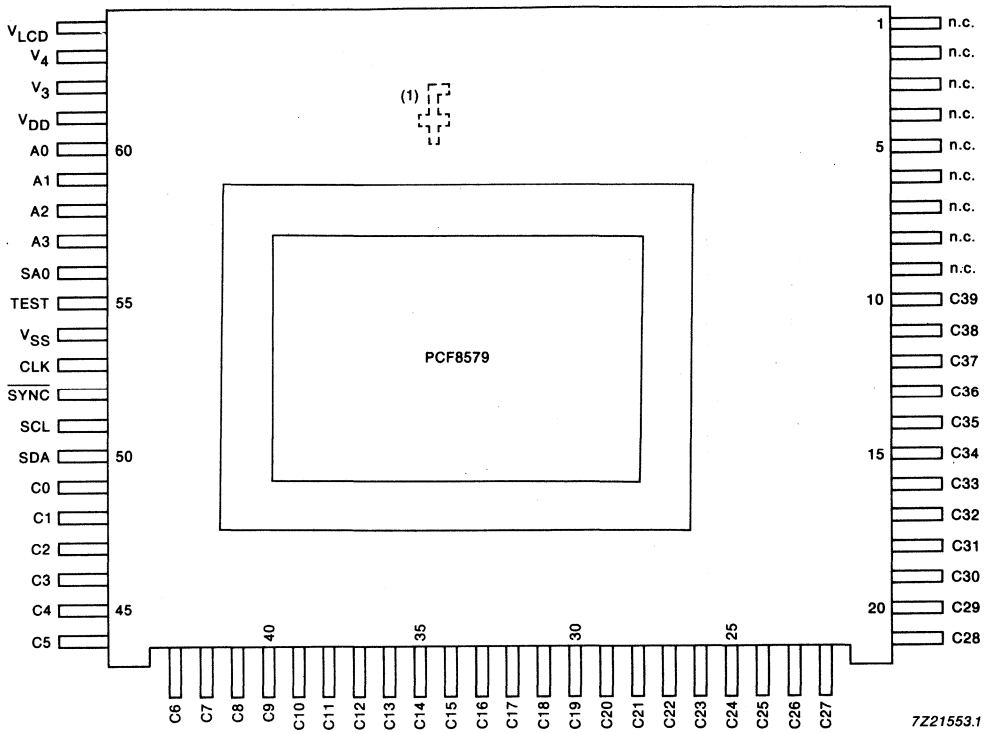


Fig.2 (a) Pinning diagram: VSO56; SOT190.

DEVELOPMENT DATA

PINNING (continued)



(1) Orientation mark.

Fig.2 (b) Pinning diagram: SOT267A.

mnemonic	pin no.		description
	SOT190	SO122	
SDA	1	50	I^2C-bus serial data line
SCL	2	51	I^2C-bus serial clock line
$\overline{SYNC}$	3	52	cascade synchronization input
CLK	4	53	external clock input
V_{SS}	5	54	ground (logic)
TEST	6	55	test pin (connect to V_{SS})
SA0	7	56	I^2C-bus slave address input (bit 0)
A3 to A0	8 - 11	57 - 60	I^2C-bus subaddress inputs
V_{DD}	12	61	positive supply voltage
n.c.	13 *	1 - 9	not connected
V_3 to V_4	14 - 15	62 - 63	LCD bias voltage inputs
V_{LCD}	16	64	LCD supply voltage
C39 to C0	17 - 56	10 - 49	LCD column driver outputs

DEVELOPMENT DATA

* Do not connect, this pin is reserved.

DC CHARACTERISTICS

V_{DD} = 2.5 V to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
LCD supply voltage		V_{LCD}	V_{DD} −9	–	V_{DD} −3.5	V
Supply current	note 1; f_{CLK} = 2 kHz	I_{DD1}	–	9	20	μA
Power-on reset level	note 2	V_{POR}	–	1.3	1.8	V
Logic						
Input voltage LOW		V_{IL}	V_{SS}	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Leakage current at SDA, SCL, $\overline{SYNC}$, CLK, TEST, SA0, A0, A1, A2 and A3	V_I = V_{DD} or V_{SS}	I_{L1}	−1	–	1	μA
SDA output current LOW	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL}	3	–	–	mA
Input capacitance	note 3	C_I	–	–	5	pF
LCD outputs						
Leakage current at V_3 to V_4	V_I = V_{DD} or V_{LCD}	I_{L2}	−2	–	2	μA
DC component of LCD drivers C0 to C39		± V_{DC}	–	20	–	mV
Output resistance at C0 to C39	note 4	R_{COL}	–	3	6	kΩ

AC CHARACTERISTICS (note 5)

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Clock frequency	50% duty factor	f_{CLK}	–	*	10	kHz
Driver delays	$V_{DD} - V_{LCD}$ = 9 V; with test loads	t_{PLCD}	–	–	100	µs
I²C-bus						
SCL clock frequency		f_{SCL}	–	–	100	kHz
Tolerable spike width on bus		t_{SW}	–	–	100	ns
Bus free time		t_{BUF}	4.7	–	–	µs
Start condition set-up time	repeated start codes only	$t_{SU;STA}$	4.7	–	–	µs
Start condition hold time		$t_{HD;STA}$	4.0	–	–	µs
SCL LOW time		t_{LOW}	4.7	–	–	µs
SCL HIGH time		t_{HIGH}	4.0	–	–	µs
SCL and SDA rise time		t_r	–	–	1.0	µs
SCL and SDA fall time		t_f	–	–	0.3	µs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop condition set-up time		$t_{SU;STO}$	4.0	–	–	µs

DEVELOPMENT DATA

* Typically 0.9 to 3.3 kHz.

Notes to the characteristics

1. Outputs are open; inputs at V_{DD} or V_{SS}; I^2C-bus inactive; clock with 50% duty cycle.
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled; not 100% tested.
4. Resistance measured between output terminal (C0 to C39) and bias input (V_3 to V_4, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 1):

   $V_{OP} = V_{DD} - V_{LCD} = 9$ V;

   $V_3 - V_{LCD} \geqslant 4.70$ V; $V_4 - V_{LCD} \leqslant 4.30$ V; $I_{LOAD} = 100\ \mu$A.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

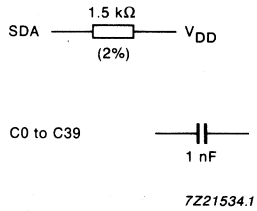
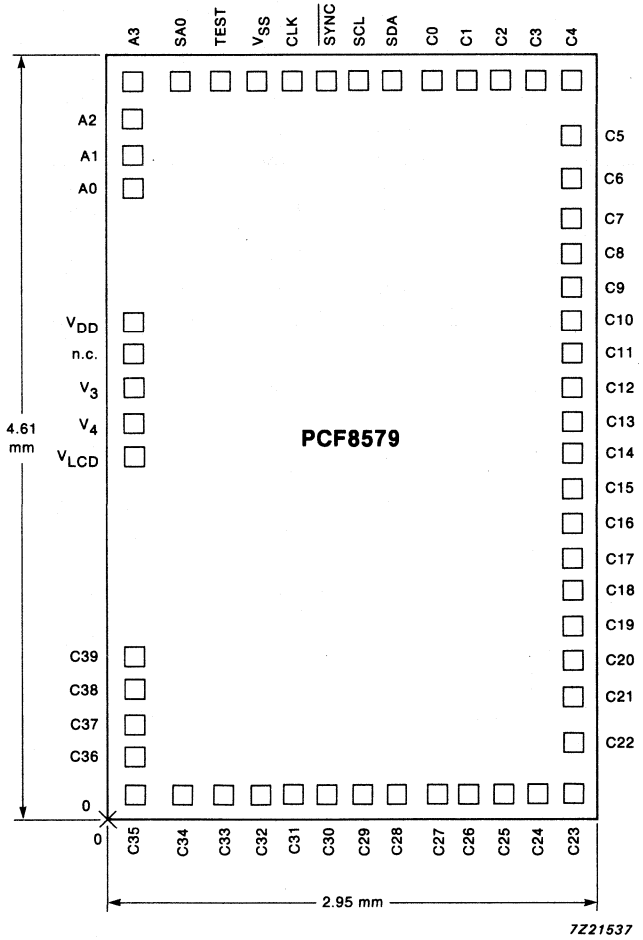


Fig.16 Test loads.

DEVELOPMENT DATA

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



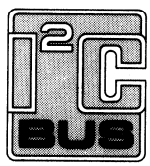
Chip area: 13.6 mm^2
Bonding pad dimensions: 120 μm x 120 μm

Fig.23 Bonding pad locations.

Table 4 Bonding pad locations (dimensions in μm)

All x/y co-ordinates are referenced to the bottom left corner, see Fig.23.

pad	X	Y	pad	X	Y
SDA	1726	4444	C27	1972	160
SCL	1522	4444	C26	2176	160
$\overline{\text{SYNC}}$	1318	4444	C25	2380	160
CLK	1114	4444	C24	2584	160
V_{SS}	910	4444	C23	2788	160
TEST	688	4444	C22	2788	472
SA0	442	4444	C21	2788	736
A3	160	4444	C20	2788	976
A2	160	4222	C19	2788	1180
A1	160	4018	C18	2788	1384
A0	160	3814	C17	2788	1588
V_{DD}	160	3010	C16	2788	1792
n.c.	160	2806	C15	2788	1996
V_2	160	2602	C14	2788	2200
V_3	160	2398	C13	2788	2404
V_{LCD}	160	2194	C12	2788	2608
C39	160	994	C11	2788	2812
C38	160	790	C10	2788	3016
C37	160	586	C9	2788	3220
C36	160	382	C8	2788	3424
C35	160	160	C7	2788	3628
C34	442	160	C6	2788	3868
C33	688	160	C5	2788	4132
C32	910	160	C4	2788	4444
C31	1114	160	C3	2584	4444
C30	1318	160	C2	2380	4444
C29	1522	160	C1	2176	4444
C28	1726	160	C0	1972	4444



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

128 x 8-BIT EEPROM WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8581 and PCF8581C are low-power CMOS EEPROMs with standard and wide operating voltage:
4.5 to 5.5 V (PCF8581); 2.5 to 6.0 V (PCF8581C).

In the following text, the generic term "PCF8581" is used to refer to both types in all packages except where specified.

The PCF8581 is organized as 128 words by 8-bits.

Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. All bytes can be read in a single operation. Up to eight bytes can be written in one operation, reducing the total write time per byte. Three address pins A0, A1 and A2 are used to define the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage: 4.5 to 5.5 V (PCF8581); 2.5 to 6.0 V (PCF8581C)
- Integrated voltage multiplier and timer for writing (no external components required)
- Automatic erase before write
- Low standby current max. 10 μA
- Eight-byte page write mode
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Designed for 10 000 write cycles per byte minimum
- 10 years minimum non-volatile data retention
- Infinite number of read cycles
- Pin and address compatibility to PCF8570, PCF8571 and PCF8582

PACKAGE OUTLINES

PCF8581P/PCF8581CP: 8-lead DIL; plastic (SOT97).
PCF8581T/PCF8581CT: 8-lead mini-pack (SO8L; SOT176C).

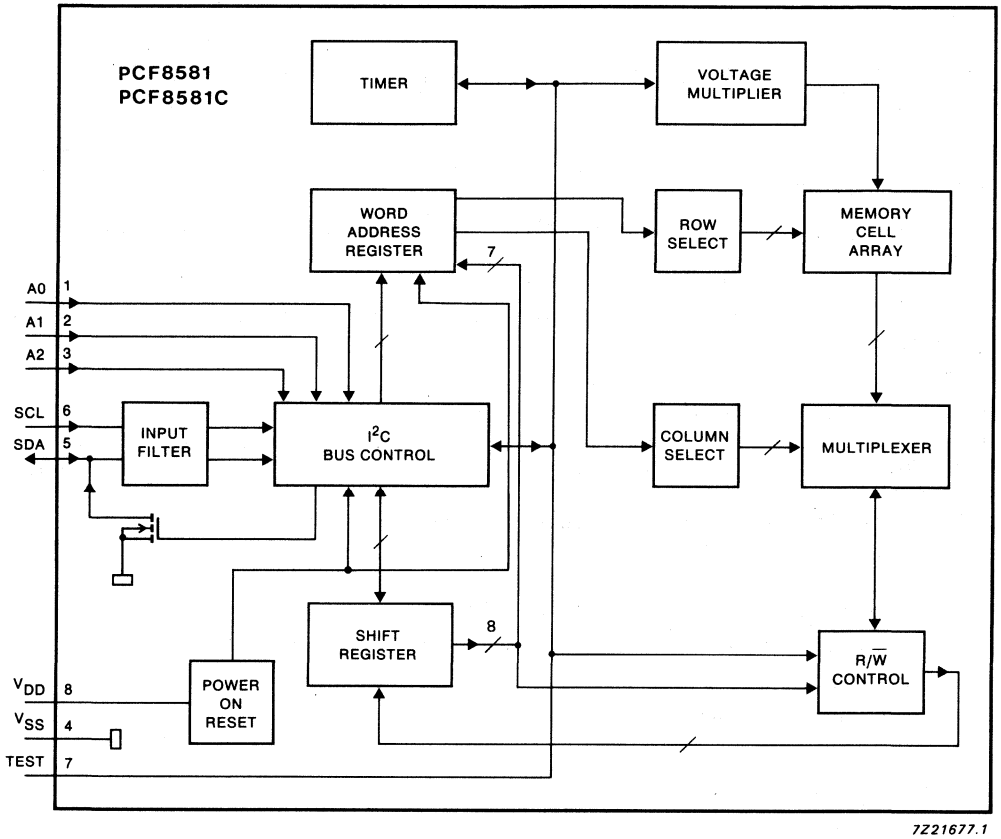


Fig.1 Block diagram.

DEVELOPMENT DATA

PINNING

1	A0	hardware address inputs	
2	A1		
3	A2		
4	V_{SS}	negative supply	
5	SDA	serial data input/output	I²C-bus
6	SCL	serial clock input	
7	TEST	test output can be connected to V_{SS}, V_{DD} or left open-circuit	
8	V_{DD}	positive supply	

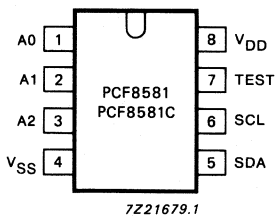


Fig.2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

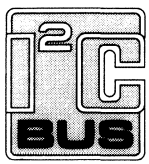
parameter	symbol	min.	max.	unit
Supply voltage range (pin 8)	V_{DD}	−0.3	7.0	V
Voltage range on any input*	V_I	−0.8	V_{DD} + 0.8	V
DC input current (any input)	$\pm I_I$	−	10	mA
DC output current (any output)	$\pm I_O$	−	10	mA
Total power dissipation	P_{tot}	−	150	mW
Power dissipation per output	P	−	50	mW
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C

* Measured via a 500 Ω resistor.

CHARACTERISTICS

V_{DD} = 2.5 to 6 V (PCF8581C) 4.5 to 5.5 V (PCF8581); V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range						
PCF8581A		V_{DD}	2.5	–	6.0	V
PCF8581		V_{DD}	4.5	–	5.5	V
Supply current						
standby	f_{SCL} = 0 Hz	I_{DD}	–	–	10	μA
operating	f_{SCL} = 100 kHz	I_{DD}	–	–	400	μA
during write	see bus protocol	I_{DD}	–	–	1000	μA
Inputs						
A0, A1, A2, SCL, SDA						
Input voltage LOW		V_{IL}	–	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	–	V
Input leakage current	pin at V_{SS} or V_{DD}	I_{LI}	–	–	1	μA
Input capacitance	pin at V_{SS}	C_I	–	–	7	pF
Outputs						
SDA						
Output current LOW	pin at 0.4 V	I_{OL}	3	–	–	mA
TEST						
Output leakage current	pin at V_{SS} or V_{DD}	I_{LO}	–	–	1	μA
Erase/write data						
Write time		t_{WR}	6	–	12	ms
Data retention time		t_{RET}	10	–	–	years



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FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

CLOCK CALENDAR WITH 256 X 8-BIT STATIC RAM

GENERAL DESCRIPTION

The PCF8583 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. One address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

Features

- I^2C-bus interface operating supply voltage: 2.5 V to 6 V
- Clock operating supply voltage (0 to 70 °C): 1.0 V to 6 V
- Data retention voltage: 1.0 V to 6 V
- Operating current (f_{SCL} = 0 Hz): max. 50 μA
- Clock function with four year calendar
- 24 or 12 hour format
- 32,768 kHz or 50 Hz time base
- Serial input/output bus (I^2C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function

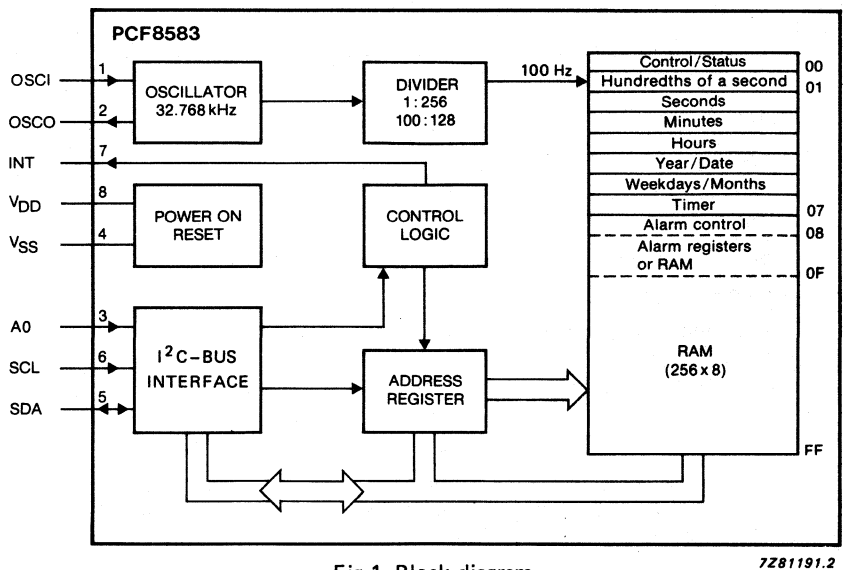


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8583P: 8-lead DIL; plastic (SOT97).
PCF8583T: 8-lead mini-pack; plastic (SO8L; SOT176A).

PINNING

1	OSCI	oscillator input, 50 Hz or event-pulse input	
2	OSCO	oscillator output	
3	A0	address input	
4	V_{SS}	negative supply	
5	SDA	serial data line	I^2C-bus
6	SCL	serial clock line	I^2C-bus
7	INT	open drain interrupt output (active low)	
8	V_{DD}	positive supply	

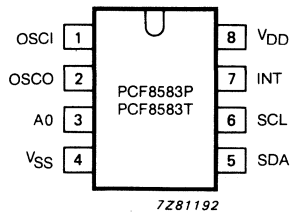


Fig.2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 8)	V_{DD}	−0.8	+ 7.0	V
Supply current (pin 4 or pin 8)	I_{DD}; I_{SS}	–	50	mA
Input voltage range	V_I	−0.8 to V_{DD}	+ 0.8	V
DC input current	I_I	–	10	mA
DC output current	I_O	–	10	mA
Power dissipation per package	P_{tot}	–	300	mW
Power dissipation per output	P_O	–	50	mW
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage						
operating		V_{DD}	2.5	–	6.0	V
clock	T_{amb} = 0 to + 70 °C	V_{DD}	1.0	–	6.0	V
Supply current						
operating	f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
clock	V_{DD} = 5 V	I_{DDO}	–	10	50	μA
clock	V_{DD} = 1 V	I_{DDO}	–	2	10	μA
Power-on reset voltage level	note 1	V_{POR}	1.5	1.9	2.3	V
Inputs; Input/output SDA						
Input voltage LOW	note 2	V_{IL}	−0.8	–	$0.3V_{DD}$	V
Input voltage HIGH	note 2	V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.8	V
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
A0; OSCI						
Input leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_{LI}\|$	–	–	250	nA
SCL; SDA						
Input capacitance	$V_I = V_{SS}$	C_I	–	–	7	pF
Output INT						
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
LOW V_{DD} data retention						
Supply voltage for data retention		V_{DDR}	1	–	6	V
Supply current	note 3					
	V_{DDR} = 1 V; T_{amb} = −25 to + 70 °C;	I_{DDR}	–	–	5	μA
	V_{DDR} = 1 V	I_{DDR}	–	–	2	μA

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Integrated oscillator capacitance		C_{OSC}	–	40	–	pF
Oscillator stability for ΔV_{DD} = 100 mV	T_{amb} = 25 °C; V_{DD} = 1.5 V	f/fOSC	–	2×10^{-7}	–	
Input frequency	note 4	f_i	–	–	1	MHz
Quartz crystal parameters						
Frequency = 32.768 kHz						
Series resistance		R_S	–	–	40	kΩ
Parallel capacitance		C_L	–	10	–	pF
Trimmer capacitance		C_T	5	–	25	pF

Notes to the characteristics

1. The power-on reset circuit resets the I²C-bus logic when $V_{DD} < V_{POR}$.
2. When the voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ± 0.5 mA.
3. Event or 50 Hz mode only (no Quartz).
4. Event mode only.

APPLICATION INFORMATION

Quartz frequency adjustment

Method 1: Fixed OSCI capacitor

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 1 Hz signal available after power-on at the interrupt output (pin 7). The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average ± 5 x 10^{-6}). Average deviations of ± 5 minutes per year can be achieved.

Method 2: OSCI Trimmer

Using the alarm function (via the I²C-bus) a signal faster than 1 Hz can be generated at the interrupt output for fast setting of a trimmer.

Procedure:

Power-on
Initialization (alarm function)

Routine:

Set clock to time T and set alarm to time T + dT.
At time T + dT (interrupt) repeat routine.

If time dT is approximately 10 ms a frequency of approximately 40 Hz is obtained.

APPLICATION INFORMATION

The PCF8583 slave address has a fixed combination 1010 as group 1.

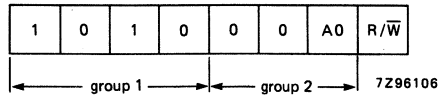
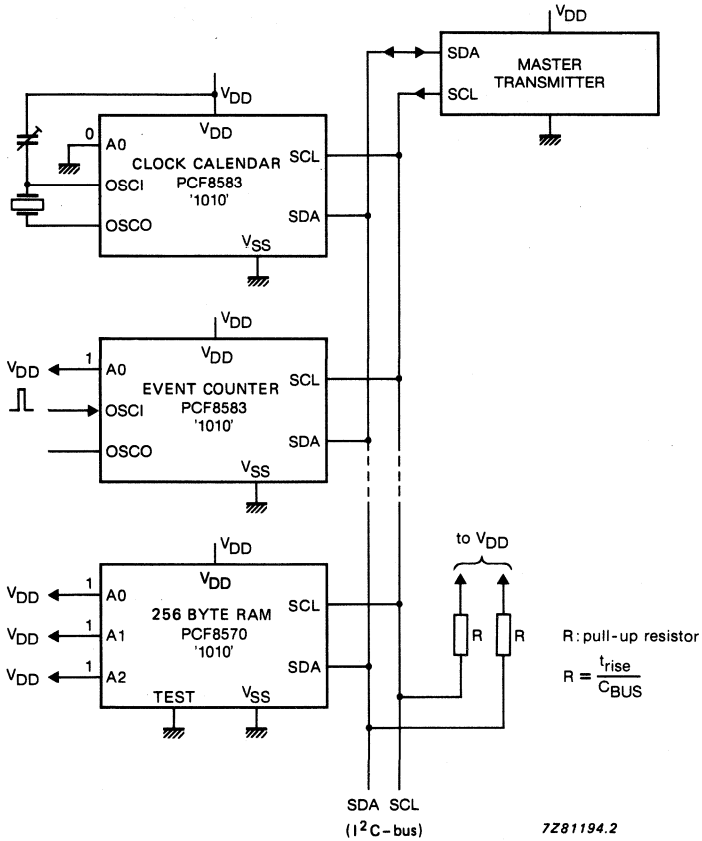


Fig.16 PCF8583 address.



Recommendation:
Connect a 4.7 μF 10 V solid aluminium (SAL) capacitor between V_{DD} and V_{SS}.

Fig.17 PCF8583 application diagram.

DEVELOPMENT DATA

8-BIT A/D AND D/A CONVERTER

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

Features

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P:16-lead DIL; plastic (SOT38).
PCF8591T:16-lead mini-pack; plastic (SO16L; SOT162A).

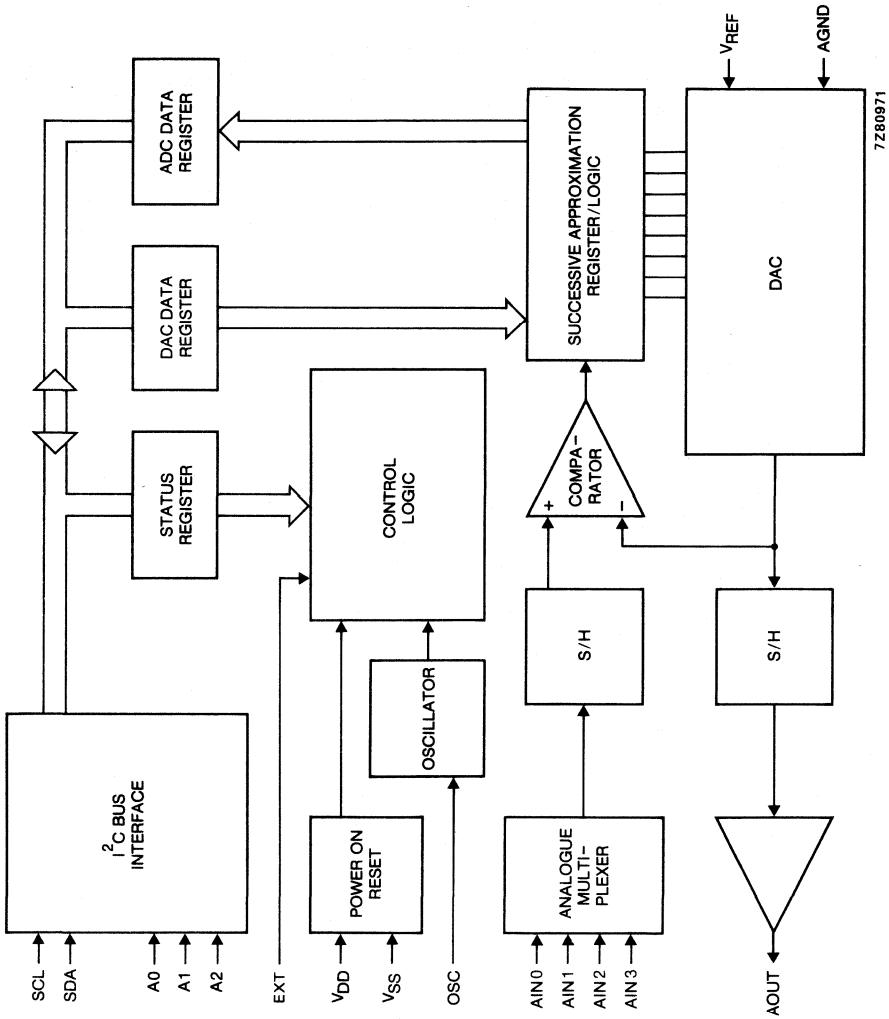


Fig. 1 Block diagram.

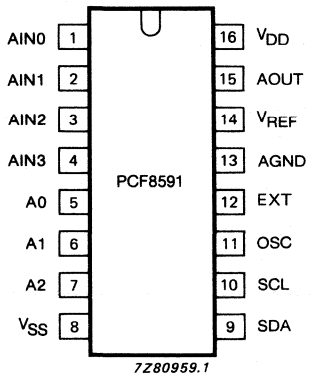


Fig. 2 Pinning diagram.

PINNING

1.	AIN0	analogue inputs (A/D converter)
2.	AIN1	
3.	AIN2	
4.	AIN3	
5.	A0	hardware address
6.	A1	
7.	A2	
8.	V_{SS}	negative supply voltage
9.	SDA	I^2C bus data input/output
10.	SCL	I^2C bus clock input/output
11.	OSC	oscillator input/output
12.	EXT	external/internal switch for oscillator input
13.	AGND	analogue ground
14.	V_{REF}	voltage reference input
15.	AOUT	analogue output (D/A converter)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

DEVELOPMENT DATA

Adressing

Each PCF8591 device in an I^2C bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be sent as the first byte after the start condition in the I^2C bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figs 3 and 10).

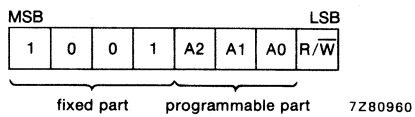


Fig. 3 Address byte.

Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analogue output, and for programming the analogue inputs as single-ended or differential inputs. The lower nibble selects one of the analogue input channels defined by the upper nibble (see Fig. 4). If the auto-increment flag is set the channel number is incremented automatically after each A/D conversion.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0. The most significant bits of both nibbles are reserved for future functions and have to be set to 0. After a power-on reset condition all bits of the control register are reset to 0. The D/A converter and the oscillator are disabled for power saving. The analogue output is switched to a high impedance state.

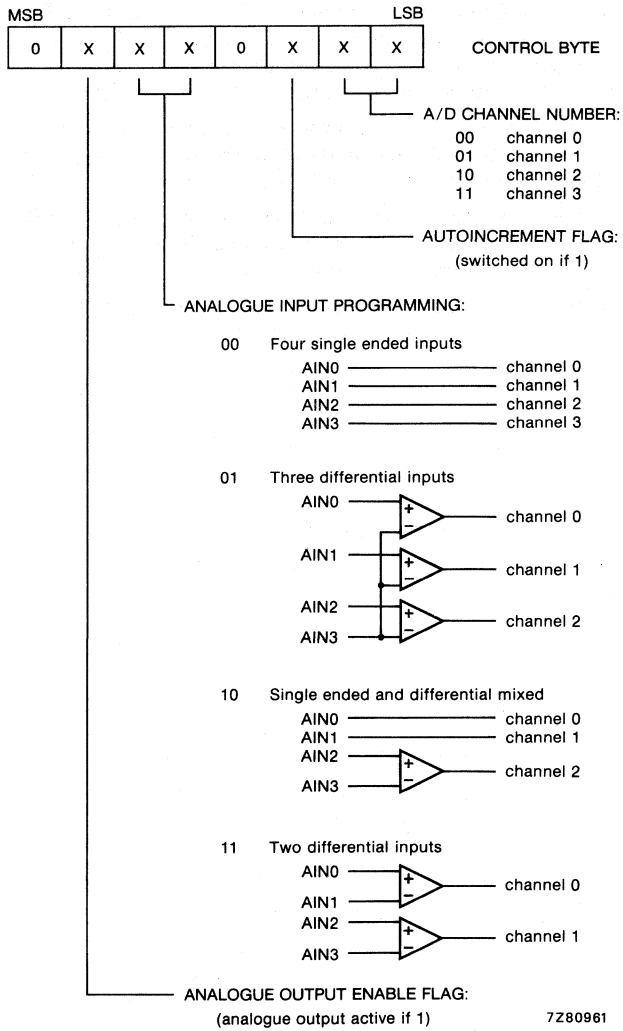


Fig. 4 Control byte.

DEVELOPMENT DATA

D/A conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analogue voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Fig. 5).

The analogue output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analogue output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analogue output AOUT is given by the formula shown in Fig. 6. The waveforms of a D/A conversion sequence are shown in Fig. 7.

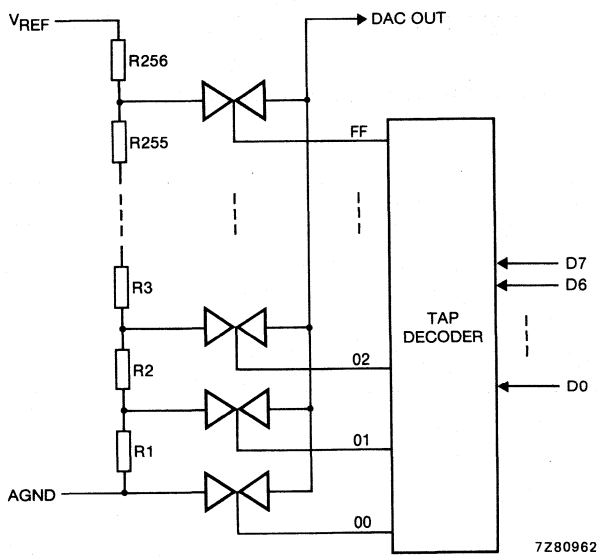


Fig. 5 DAC resistor divider chain.

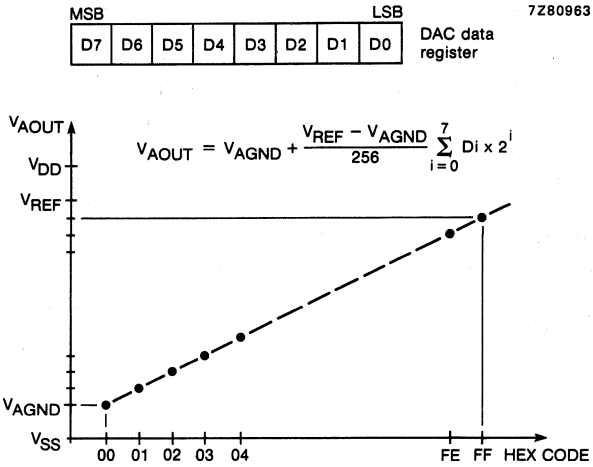


Fig. 6 DAC data and d.c. conversion characteristics.

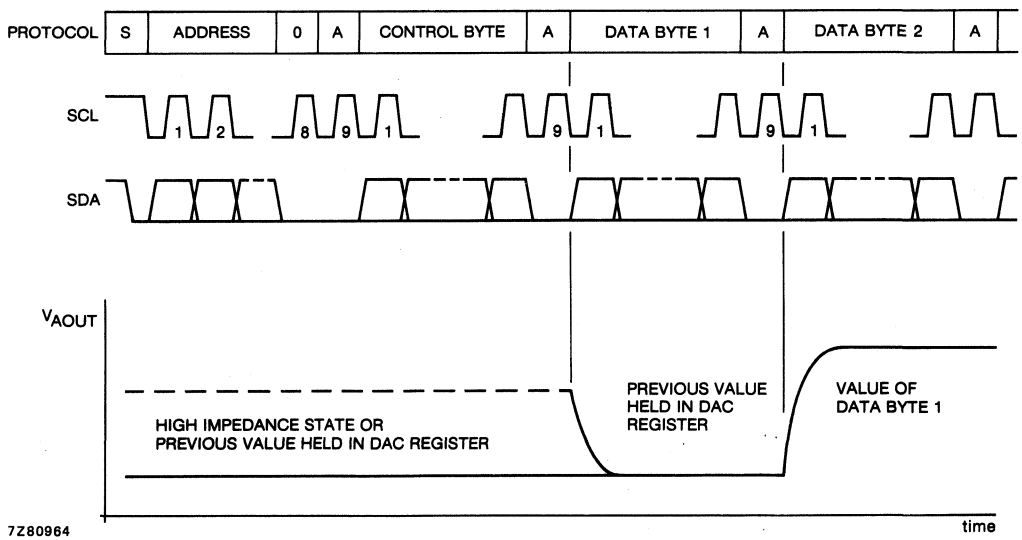


Fig. 7 D/A conversion sequence.

A/D conversion

The A/D converter makes use of the successive approximation conversion technique. The on-chip D/A converter and a high gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Fig. 8).

Once a conversion cycle is triggered an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Fig. 9). The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I^2C bus read cycle is shown in Fig. 10.

The maximum A/D conversion rate is given by the actual speed of the I^2C bus.

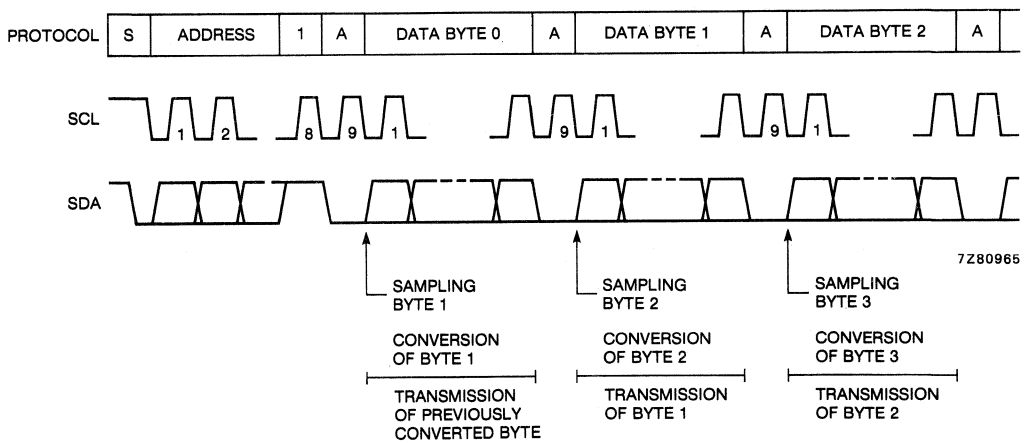


Fig. 8 A/D conversion sequence.

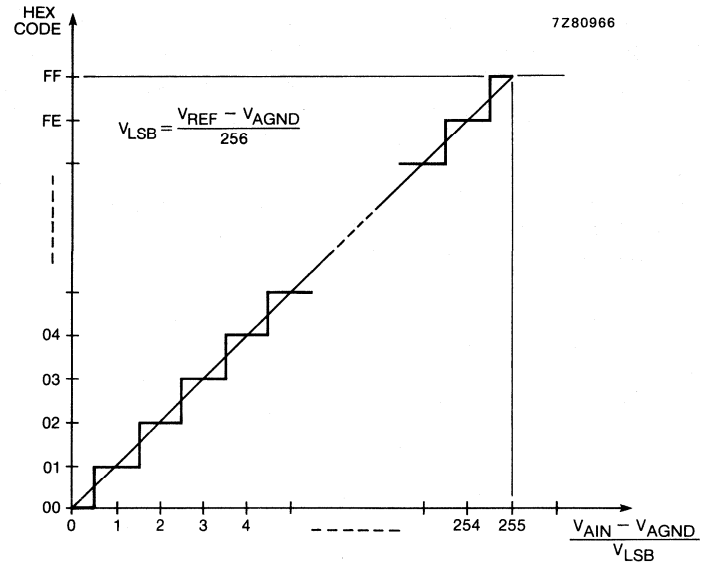


Fig. 9a A/D conversion characteristics of single-ended inputs.

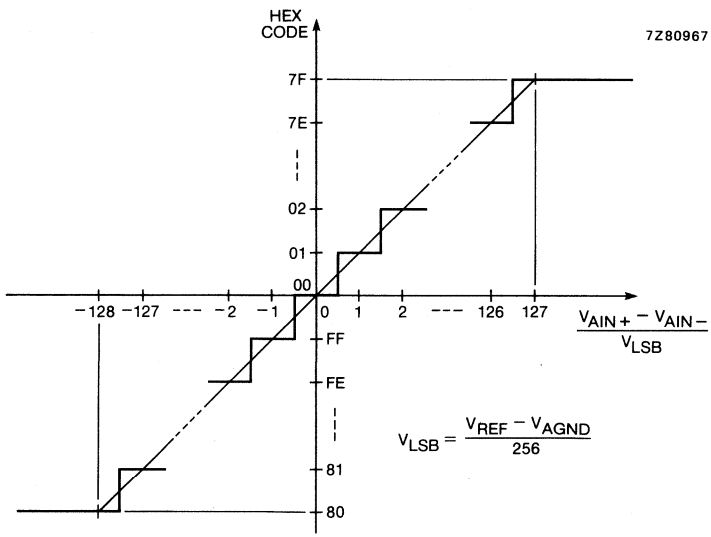


Fig. 9b A/D conversion characteristics of differential inputs.

Reference voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analogue ground and may have a d.c. off-set with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier; see Application Information and Fig. 6.

The A/D converter may also be used as a one or two quadrant analogue divider. The analogue input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high impedance state allowing the user to feed an external clock signal to OSC.

Bus protocol

After a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I^2C bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

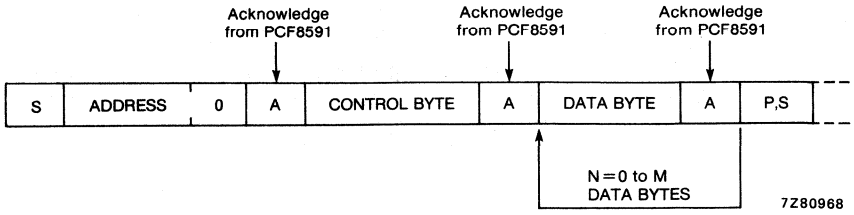


Fig. 10a Bus protocol for write mode, D/A conversion.

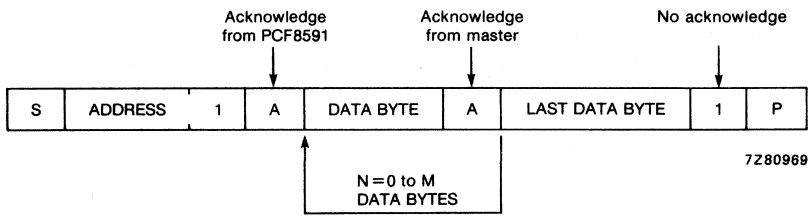


Fig. 10b Bus protocol for read mode, A/D conversion.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transfered during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

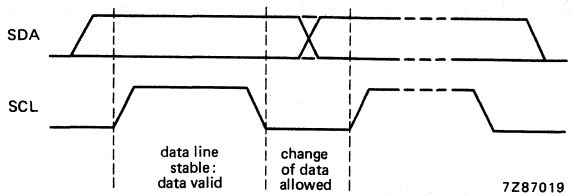


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

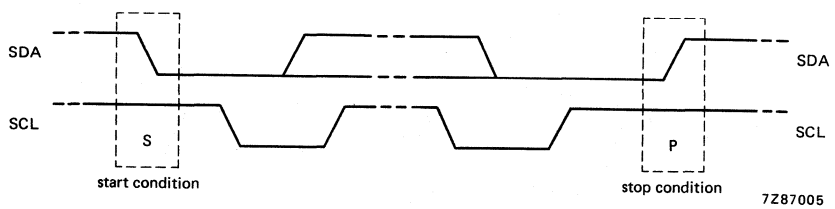


Fig. 12 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

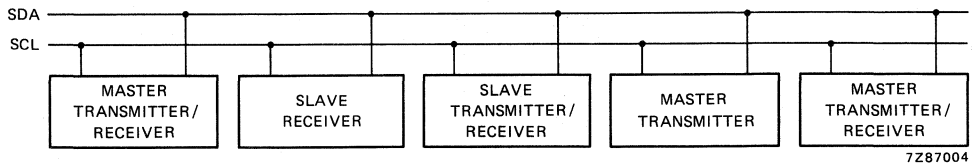


Fig. 13 System configuration.

Acknowledge.

The number of data bytes transfered between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

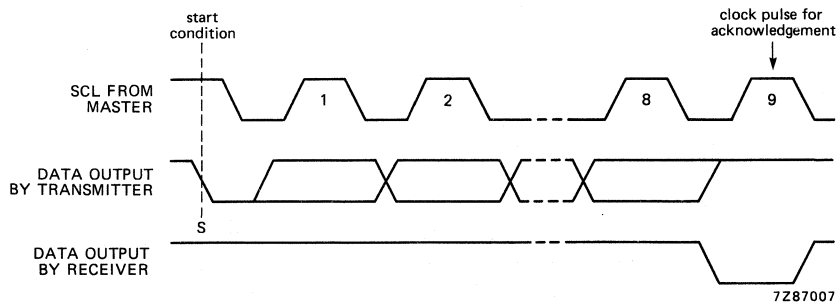


Fig. 14 Acknowledgement on the I^2C bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_R	–	–	1,0	μs
SCL and SDA fall time	t_F	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

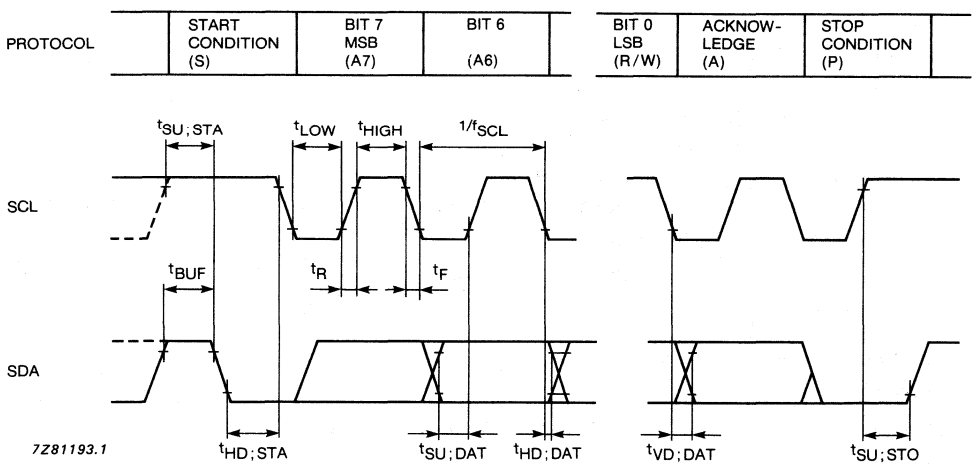


Fig. 15 I^2C bus timing diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to +8,0 V
Voltage on any pin	V_I		−0,5 to V_{DD} +0,5 V
Input current d.c.	I_I	max.	10 mA
Output current d.c.	I_O	max.	20 mA
V_{DD} or V_{SS} current	I_{DD}, I_{SS}	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	100 mW
Storage temperature range	T_{stg}		−65 to +150 °C
Operating ambient temperature range	T_{amb}		−40 to +85 °C

Note:

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	operating	V_{DD}	2,5	–	6,0	V
Supply current	standby $V_I = V_{SS}$ or V_{DD}; no load	I_{DD0}	–	1	15	μA
Supply current	operating; AOUT off; f_{SCL} = 100 kHz	I_{DD1}	–	125	250	μA
Supply current	AOUT active; f_{SCL} = 100 kHz	I_{DD2}	–	0,45	1,0	mA
Power-on reset level	note 1	V_{POR}	0,8	–	2,0	V
Digital inputs/output	SCL, SDA, A0, A1, A2					
Input voltage	LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage	HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input current	leakage; $V_I = V_{SS}$ to V_{DD}	I_I	–	–	250	nA
Input capacitance		C_I	–	–	5	pF
SDA output current	leakage; HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
SDA output current	LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Reference voltage inputs						
Voltage range*	$V_{REF} > V_{AGND}$	V_{REF}	$V_{SS}+1,6$	–	V_{DD}	V
Voltage range*	$V_{REF} > V_{AGND}$	V_{AGND}	V_{SS}	–	$V_{DD}-0,8$	V
Input current	leakage	I_I	–	–	250	nA
Input resistance	V_{REF} to AGND	R_{REF}	–	100	–	kΩ
Oscillator	OSC, EXT					
Input current	leakage	I_I	–	–	250	nA
Oscillator frequency		f_{OSC}	0,75	–	1,25	MHz

D/A CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{load} = 10 kΩ; C_{load} = 100 pF; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output						
Output voltage range	no resistive load	V_{OA}	V_{SS}	–	V_{DD}	V
Output voltage range	R_{load} = 10 kΩ	V_{OA}	V_{SS}	–	0,9xV_{DD}	V
Output current	leakage; AOUT disabled	I_{LO}	–	–	250	nA
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	50	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error	no resistive load	G_e	–	–	1	%
Settling time	to ½ LSB full scale step	t_{DAC}	–	–	90	μs
Conversion rate		f_{DAC}	–	–	11,1	kHz
Supply noise rejection	at f = 100 Hz; V_{DD} = 0,1 V_{PP}	SNRR	–	40	–	dB

DEVELOPMENT DATA

* A further extension of the range is possible, if the following conditions are fulfilled:

$$\frac{V_{REF} + V_{AGND}}{2} \geqslant 0,8\ V \text{ and } V_{DD} - \frac{V_{REF} + V_{AGND}}{2} \geqslant 0,4\ V.$$

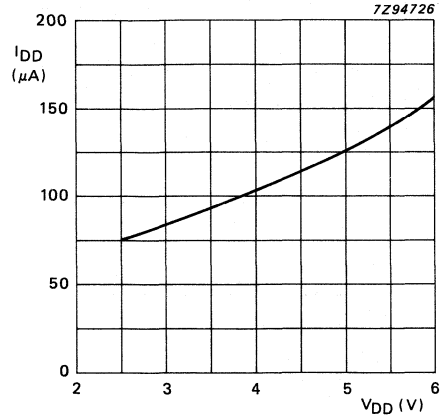
A/D CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{source} = 10 kΩ; T_{amb} = −40 °C to +85 °C unless otherwise specified

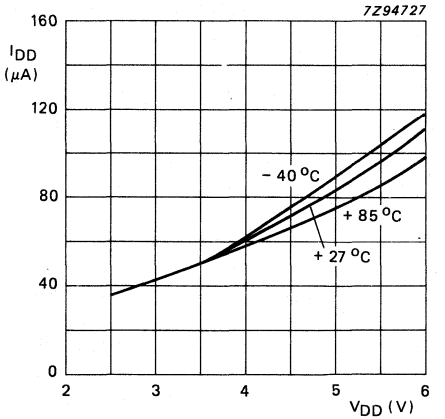
parameter	conditions	symbol	min.	typ.	max.	unit
Analogue inputs						
Input voltage range		V_{IA}	V_{SS}	–	V_{DD}	V
Input current	leakage	I_{IA}	–	–	100	nA
Input capacitance		C_{IA}	–	10	–	pF
Input capacitance	differential	C_{ID}	–	10	–	pF
Single-ended voltage	measuring range	V_{IS}	V_{AGND}	–	V_{REF}	V
Differential voltage	measuring range; $V_{FS} = V_{REF} - V_{AGND}$	V_{ID}	$\frac{-V_{FS}}{2}$	–	$\frac{+V_{FS}}{2}$	V
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	20	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error		G_e	–	–	1	%
Gain error	small-signal; ΔV_{IN} = 16 LSB	GS_e	–	–	5	%
Rejection ratio	common-mode	CMRR	–	60	–	dB
Supply noise rejection	at f = 100 Hz; $V_{DDN} = 0{,}1 \times V_{PP}$	SNRR	–	40	–	dB
Conversion time		t_{ADC}	–	–	90	μs
Sampling/conversion rate		f_{ADC}	–	–	11,1	kHz

Note

1. The power on reset circuit resets the I^2C bus logic when V_{DD} is less than V_{POR}.



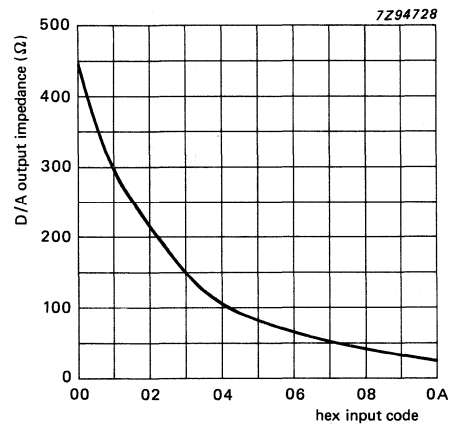
(a) internal oscillator; T_{amb} = + 27 °C.



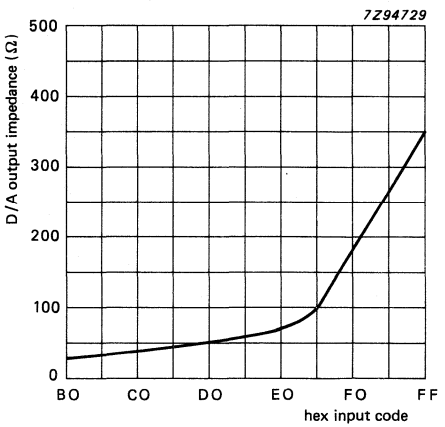
(b) external oscillator.

Fig. 16 Operating supply current against supply voltage (analogue output disabled).

DEVELOPMENT DATA



(a) output impedance near negative power rail; T_{amb} = + 27 °C.



(b) output impedance near positive power rail; T_{amb} = + 27 °C.

Fig. 17 Output impedance of analogue output buffer (near power rails).

The x-axis represents the hex input-code equivalent of the output voltage.

APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analogue inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize cross-talk of the digital to analogue signal paths the user has to design the printed-circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors ($> 10\ \mu F$) are recommended for power supply and reference voltage inputs.

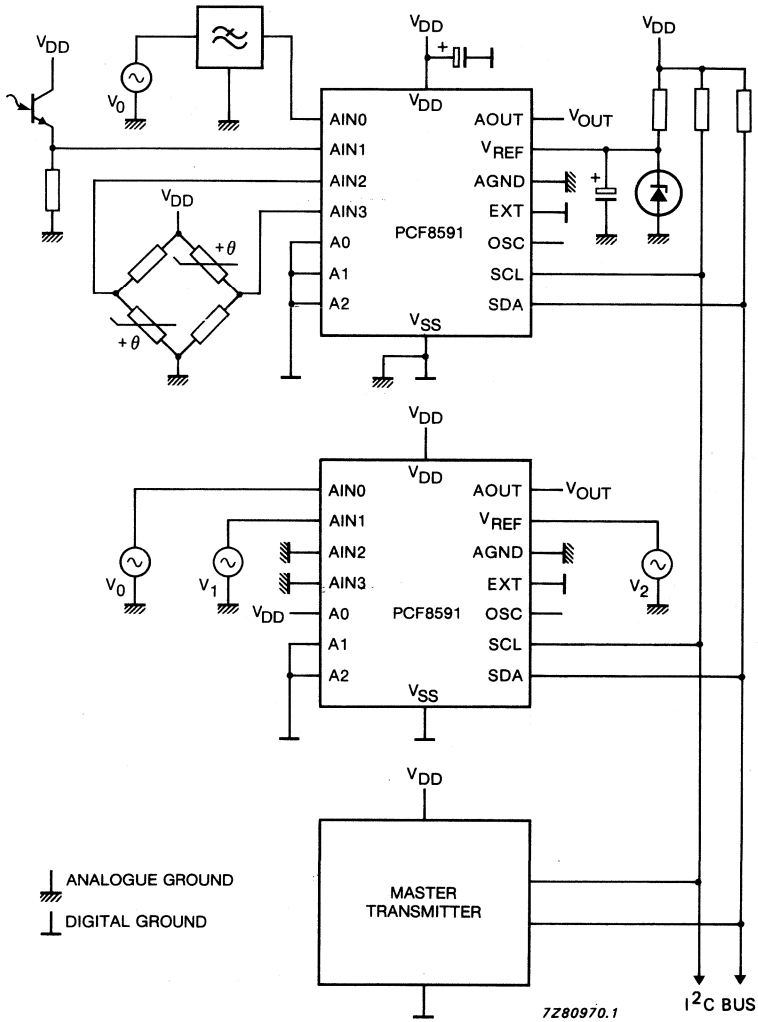


Fig. 18 Application diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCF86C410/610 family of microcontrollers is manufactured in an advanced CMOS technology. The generic term PCF86C410 is used to refer to both family members. The instruction set of the PCF86C410 is based on that of the 8051.

- PCF86C410: 4 K bytes ROM, 128 bytes RAM
- PCF86C610: 8 K bytes ROM, 256 bytes RAM

The PCF86C410 is designed for high-end feature and cordless telephones. The device has low power consumption and a wide range of supply voltage. For emulation purposes, the PCF86C000 (Piggy-back version) with 256 bytes of RAM is recommended.

The PCF86C410 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down.

The PCB86C410 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions; 49 one-byte, 46 two-byte and 16 three-byte.

Features

- Full static 80C51 CPU
- 8-bit CPU, ROM, RAM, I/O in a single 40-lead DIL/mini-pack package
- 4 K x 8 ROM, expandable externally to 64 K bytes
- 128 bytes RAM, expandable externally to 64 K bytes
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- I^2C-bus interface for serial transfer on two lines
- External memory expandable up to 128 K, external ROM up to 64 K and/or RAM up to 64 K
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Thirteen source, thirteen vector interrupt structure with two priority levels
- Enhanced architecture with:
  - non-page orientated instructions
  - direct addressing
  - four eight byte RAM register banks
  - stack depth up to 128 bytes
  - multiply, divide, subtract and compare instructions
- STOP and IDLE mode
- Wake up via external interrupts at Port 1
- Single supply voltage 1.5 V to 6.0 V
- Frequency range of 32 kHz to 16 MHz
- Very low current consumption: typ. 4 mA
- Operating temperature range: −40 to + 85 °C

PACKAGE OUTLINES

PCF86C410/610P: 40-lead DIL; plastic (SOT129).
PCF86C410/610T: 40-lead mini-pack; plastic (SOT158A).

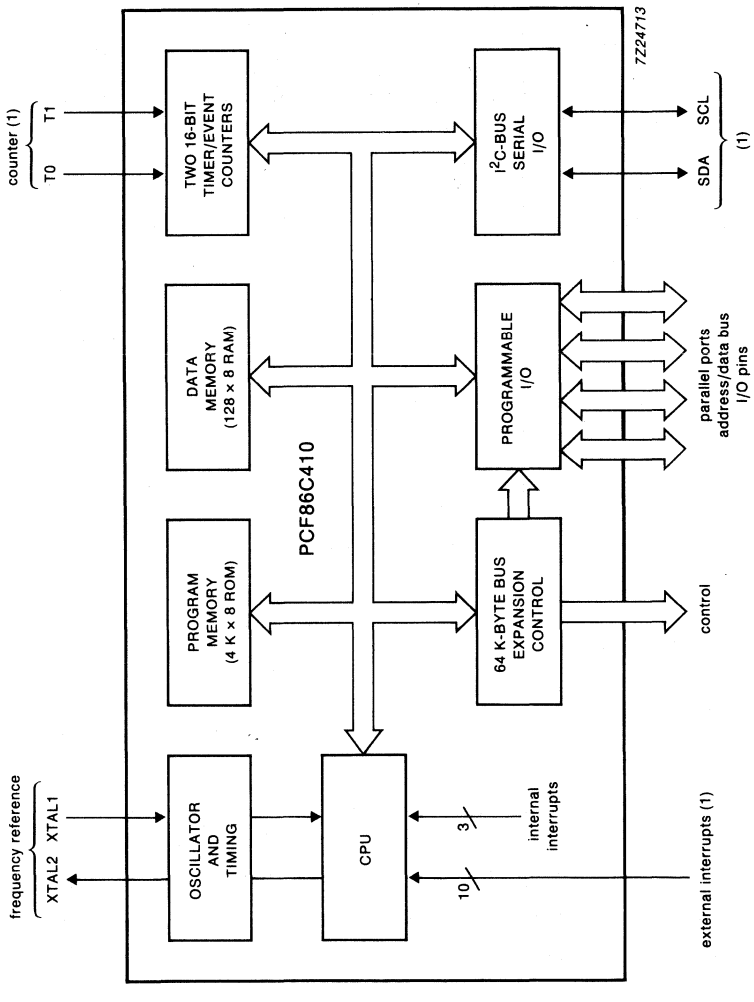


Fig.1 Block diagram.

(1) Pins shared with parallel port pins.

DEVELOPMENT DATA

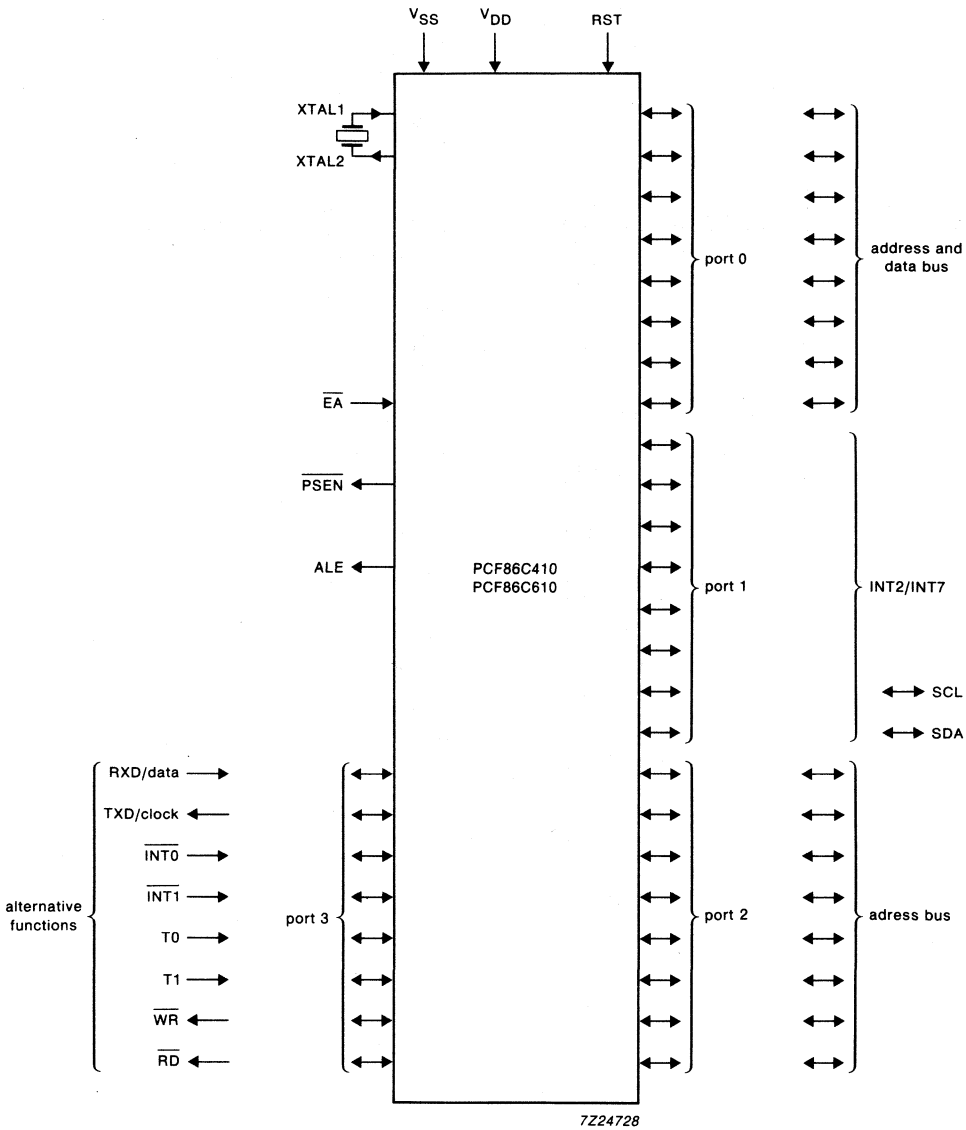


Fig.2 Functional diagram.

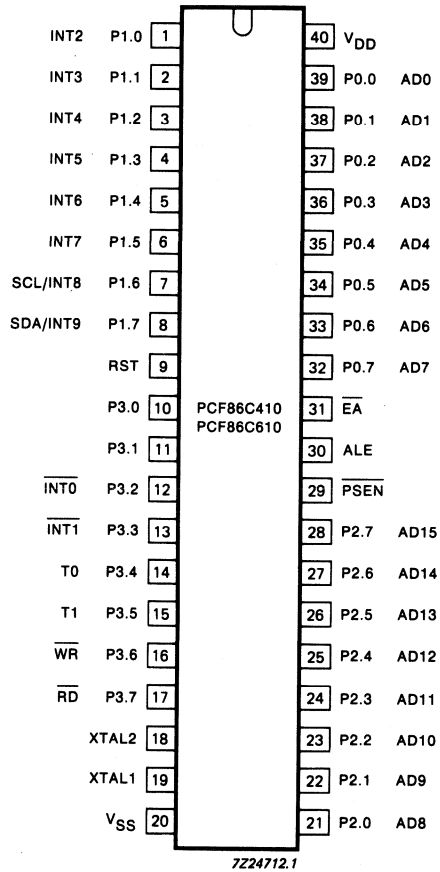


Fig.3 Pinning.

PINNING

pin no.	designation	function
1 2 3 4 5 6	P1.0/INT2 P1.1/INT3 P1.2/INT4 P1.3/INT5 P1.4/INT6 P1.5/INT7	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled HIGH by the internal pullups, and in that state can be used as inputs. The Port 1 output buffer can sink/source 4 LS TTL loads. As inputs, Port 1 pins that are externally pulled LOW will source current (I_{IL} in the characteristics) due to the internal pullups. Port 1 also serves the alternative functions INT2 to INT9.
7	P1.6/INT8	**SCL:** I^2C-bus serial port clock line.
8	P1.7/INT9	**SDA:** I^2C-bus serial port data line.
9	RST	**Reset:** A high level on this pin for two machine cycles while the oscillator is running resets the device.
10-17	P3.0-P3.7	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source 4 LS TTL inputs. Port 3 pins that have 1s written to them are pulled HIGH by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled LOW will source current (I_{IL} in the characteristics) due to the internal pull-ups.
12	P3.2/$\overline{\text{INT0}}$	**$\overline{\text{INT0}}$:** external interrupt 0.
13	P3.3/$\overline{\text{INT1}}$	**$\overline{\text{INT1}}$:** external interrupt 1.
14	P3.4/T0	**T0:** Timer 0 external input.
15	P3.5/T1	**T1:** Timer 1 external input.
16	P3.6/$\overline{\text{WR}}$	**$\overline{\text{WR}}$:** external data memory write strobe.
17	P3.7/$\overline{\text{RD}}$	**$\overline{\text{RD}}$:** external data memory read strobe.
18	XTAL2	**Crystal output:** output of the inverting amplifier of the oscillator. Left open when external clock is used.
19	XTAL1	**Crystal input:** input to the inverting amplifier of the oscillator, also the input for an externally generated clock source.
20	V_{SS}	**Ground:** circuit ground potential.
21-28	P2.0-P2.7	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled HIGH by the internal pullups, and in that state can be used as inputs. The Port 2 output buffer can sink/source 4 LS TTL loads. Port 2 emits the high-order address byte during accesses to external memory that use 16-bit addresses i.e. using (MOVX @DPTR). In this application it uses the strong internal pullups when emitting 1s. During accesses to external memory that use 8-bit addresses (MOVX @Ri). Port 2 emits the contents of the P2 Special Function Register.
29	$\overline{\text{PSEN}}$	**Program store enable output:** read strobe to external program memory. When executing code out of external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle. However, during each access to external data memory two $\overline{\text{PSEN}}$ activations are skipped.
30	ALE	**Address Latch Enable:** output pulse for latching the low byte of the address during access to external memory. ALE is emitted at a constant rate of 1/6 of the oscillator frequency, and may be used for external timing or clocking purposes.

DEVELOPMENT DATA

pin no.	designation	function
31	$\overline{EA}$	**External Access:** When $\overline{EA}$ is held HIGH the CPU executes out of internal program memory (unless the program counter exceeds 0FFFH). Holding $\overline{EA}$ LOW forces the CPU to execute out of external memory regardless of the value of the program counter.
32-39	P0.0-P0.7	**Port 0:** Port 0 is an 8-bit open drain bidirectional I/O port. As an open drain output port it can sink 8 LS TTL loads. Port 0 pins that have 1s written to them float, and in that state will function as high impedance inputs. Port 0 is also the multiplexed low order address and data bus during access to external memory. In this application it uses strong internal pull-ups when emitting logic 1s.
40	V_{DD}	**Power supply:** 1.5 V to 6.0 V.

4.0 DC CHARACTERISTICS

V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; all voltages with respect to V_{SS}; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	f_{clk}	V_{DD}	1.5	–	6.0	V
RAM retention voltage in power-down mode		V_{DD}	1.0	–	6.0	V
Supply current						
operating (note 1)	V_{DD} = 5 V; f_{clk} = 16 MHz	I_{DD}	–	–	*	mA
	V_{DD} = 3 V; f_{clk} = 3.58 MHz	I_{DD}	–	–	*	µA
idle mode (note 2)	V_{DD} = 5 V; f_{clk} = 16 MHz	I_{DD}	–	–	*	mA
	V_{DD} = 3 V; f_{clk} = 3.58 MHz	I_{DD}	–	–	*	µA
power-down	V_{DD} = 2 V (note 3)	I_{PD}	–	–	10	µA
Inputs (note 6)						
Input voltage LOW		V_{IL}	V_{SS}	–	0.3	V
Input voltage HIGH		V_{IH}	0.7	–	V_{DD}	V
Outputs						
Output sink current LOW (except SDA and SCL)	V_{DD} = 5 V; V_{OL} = 0.4 V	I_{OL}	1.6	–	–	mA
	V_{DD} = 2.5 to 6.0 V	I_{OL}	0.7	–	–	mA
SDA and SCL	V_{DD} = 2.5 to 6.0 V	I_{OL}	3.0	–	–	mA
Output source current HIGH (push-pull options only)	V_{DD} = 5 V; V_{OL} = 0.4 V	$-I_{OH}$	1.6	–	–	mA
	V_{DD} = 3 V; V_{OL} = 0.4 V	$-I_{OH}$	0.7	–	–	mA
Input current logic 0	V_{DD} = 5 V; V_{IN} = 0.4 V	$-I_{IL}$	–	–	100	µA
	V_{DD} = 3 V; V_{IN} = 0.4 V	$-I_{IL}$	–	–	50	µA
Input current logic (1-to-0 transition)	V_{DD} = 5 V; V_{IN} = $V_{DD}/2$	$-I_{TL}$	–	–	1.0	mA
	V_{DD} = 3 V; V_{IN} = $V_{DD}/2$	$-I_{TL}$	–	–	500	µA
Input leakage current (Port 0, $\overline{EA}$, SCL, SDA)	$V_{SS} < V_I < V_{DD}$	$\pm I_{LI}$	–	–	10	µA
RST pull-down resistor		R_{RST}	50	–	150	kΩ

DEVELOPMENT DATA

* Value to be fixed.

DC CHARACTERISTICS (continued)

Notes to the DC characteristics

1. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 10$ ns; $V_{IL} = V_{SS} + 0.5$ V; $V_{IH} = V_{DD} - 0.5$ V; XTAL2 not connected; $\overline{EA}$ = RST + PORT 0 = V_{DD}.
2. The IDLE mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 10$ ns; $V_{SS} + 0.5$ V; $V_{IH} = V_{DD} - 0.5$ V; XTAL2 is not connected; $\overline{EA}$ = Port 0 = V_{DD}.
3. The power-down current is measured with all output pins disconnected; XTAL1 not connected; $\overline{EA}$ = Port 0 = V_{DD}; RST = V_{SS}.
4. Capacitive loading on Port 0 and Port 2 may cause spurious noise pulses to be superimposed on the LOW level output voltage of ALE, Port 1 and Port 2 pins when these pins make a 1-to-0 transition during bus operations. In the most adverse conditions (capacitive loading > 100 pF) the noise pulse on the ALE line may exceed 0.8 V. In this event it may be required to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger strobe input.
5. Capacitive loading on Port 0 and Port 2 may cause the HIGH level output voltage on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9% of V_{DD} specification when the address bits are stabilizing.
6. The input threshold voltage of P1.6/SCL and P1.7/SDA meet the I^2C-bus specification, so an input voltage below 0.3 V_{DD} will be recognized as a logic 0, while an input voltage above 0.7 V_{DD} will be recognized as a logic 1.

5.0 AC CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; C_L = 100 pF for Port 0; ALE and $\overline{PSEN}$; C_L = 80 pF for all other outputs; unless otherwise specified

		12 MHz		variable clock		
parameter	symbol	min.	max.	min.	max.	unit
ALE pulse duration	t_{LL}	127	–	$2t_{CK}-40$	–	ns
Address set-up time to ALE	t_{AL}	43	–	$t_{CK}-40$	–	ns
Address hold time after ALE	t_{LA}	48	–	$t_{CK}-35$	–	ns
Time from ALE to control pulse $\overline{PSEN}$	t_{LC}	58	–	$t_{CK}-25$	–	ns
Time from ALE to valid instruction input	t_{LIV}	–	233	–	$4t_{CK}-100$	ns
Control pulse duration $\overline{PSEN}$	t_{CC}	215	–	$3t_{CK}-35$	–	ns
Time from $\overline{PSEN}$ to valid instruction input	t_{CIV}	–	125	–	$3t_{CK}-25$	ns
Input instruction hold time after $\overline{PSEN}$	t_{CI}	0	–	0	–	ns
Input instruction float delay after $\overline{PSEN}$	t_{CIF}	–	63	–	$t_{CK}-20$	ns
Address valid after $\overline{PSEN}$	t_{AC}	75	–	$t_{CK}-8$	–	ns
Address to valid instruction input	t_{AIV}	–	302	–	$5t_{CK}-115$	ns
Address float time to $\overline{PSEN}$	t_{AFC}	12	–	0	–	ns

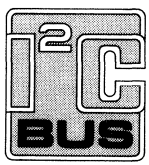
DEVELOPMENT DATA

AC CHARACTERISTICS (continued)

		12 MHz		variable clock		
parameter	symbol	min.	max.	min.	max.	unit
External data memory						
$\overline{RD}$ pulse duration	t_{RR}	400	–	$6t_{CK}-100$	–	ns
$\overline{WR}$ pulse duration	t_{WW}	400	–	$6t_{CK}-100$	–	ns
Address hold time after ALE	t_{LA}	48	–	$t_{CK}-35$	–	ns
$\overline{RD}$ to valid data input	t_{RD}	–	250	–	$5t_{CK}-165$	ns
Data hold time after $\overline{RD}$	t_{DFR}	–	97	–	$2t_{CK}-70$	ns
Time from ALE to valid data input	t_{LD}	–	517	–	$8t_{CK}-150$	ns
Address to valid data input	t_{AD}	–	585	–	$9t_{CK}-165$	ns
Time from ALE to $\overline{RD}$ and $\overline{WR}$	t_{LW}	200	300	$3t_{CK}-50$	$3t_{CK}+50$	ns
Time from address to $\overline{RD}$ or $\overline{WR}$	t_{AW}	203	–	$4t_{CK}-130$	–	ns
Time from $\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	t_{WHLH}	43	123	$t_{CK}-40$	$t_{CK}+40$	ns
Data valid to $\overline{WR}$ transition	t_{DWX}	23	–	$t_{CK}-60$	–	ns
Data set-up time before $\overline{WR}$	t_{DW}	433	–	$7t_{CK}-150$	–	ns
Data hold time after $\overline{WR}$	t_{WD}	33	–	$t_{CK}-50$	–	ns
Address float delay after $\overline{RD}$	t_{AFR}	–	12	–	12	ns

Notes to the AC characteristics

1. The maximum operating frequency is limited to 12 MHz for all versions.
2. The minimum operating frequency is limited to 1.2 MHz for all versions.
3. Interfacing the PCB86C410 to devices with float times up to 75 ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

2 TO 6 W AUDIO POWER AMPLIFIER

The TDA1011 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The device can deliver up to 6 W into 4 Ω at 16 V loaded supply in mains-fed applications. The maximum permissible supply voltage of 24 V makes this circuit very suitable for d.c. and a.c. apparatus, while the very low applicable supply voltage of 3,6 V permits 6 V applications.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 20	V
Peak output current	I_{OM}	max.	3	A
Output power at d_{tot} = 10%				
V_P = 16 V; R_L = 4 Ω	P_o	typ.	6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2	%
Input impedance				
preamplifier (pin 8)	$\lvert Z_i \rvert$	>	100	kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ.	20	kΩ
Total quiescent current	I_{tot}	typ.	14	mA
Operating ambient temperature	T_{amb}	−25 to + 150		°C
Storage temperature	T_{stg}	−55 to + 150		°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

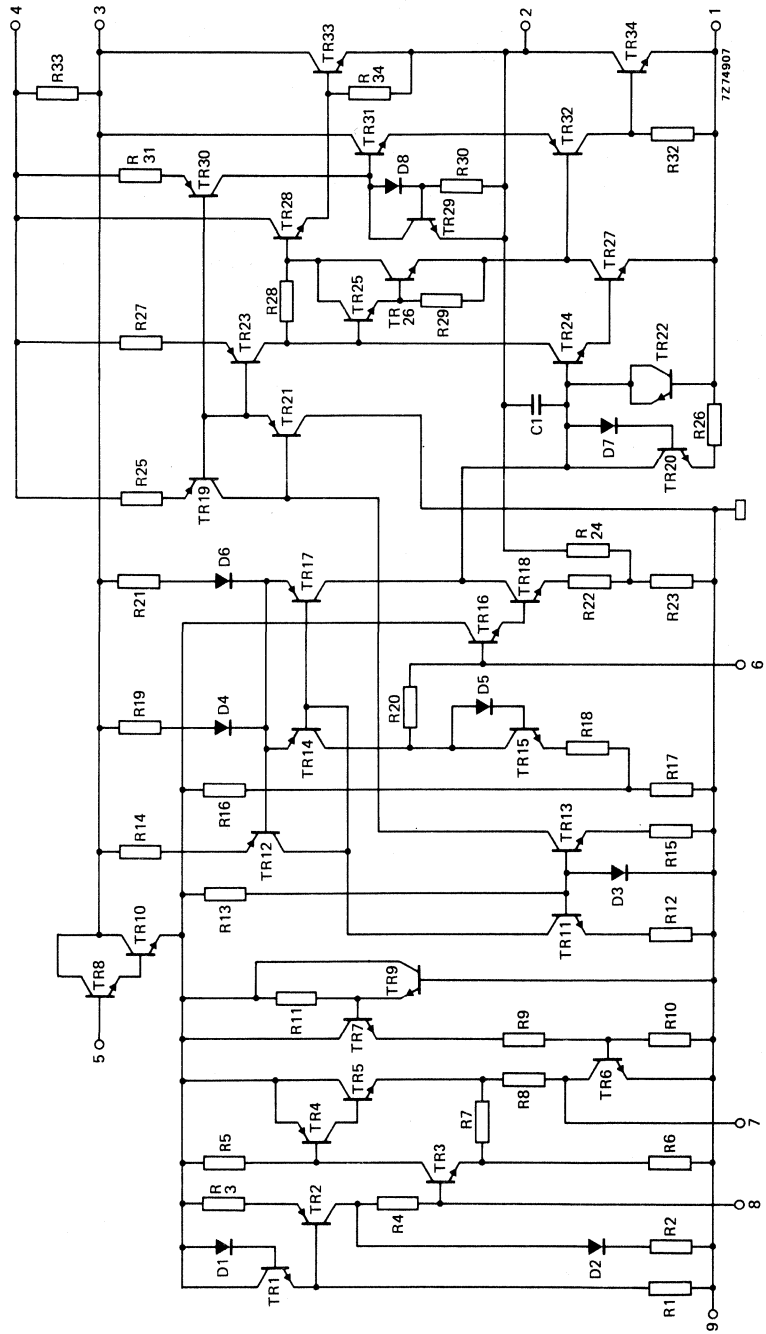


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24 V
Peak output current	I_{OM}	max.	3 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100 hours

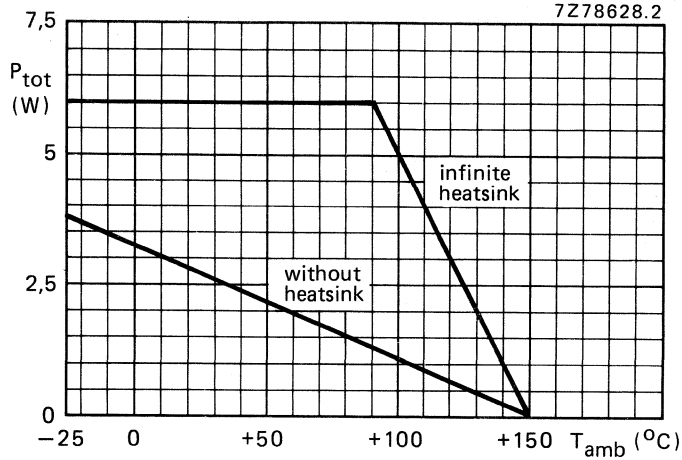


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 12 V; R_L = 4 Ω; T_{amb} = 60 °C maximum; P_o = 3,8 W.

The maximum sine-wave dissipation is 1,8 W.

The derating of 10 K/W of the package requires the following external heatsink (for sine-wave drive):

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150-60}{1,8} = 50\ K/W.$$

Since $R_{th\ j\text{-}tab}$ = 10 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 50 − (10 + 1) = 39 K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P	3,6 to 20	V
Repetitive peak output current	I_{ORM}	< 2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ. 14 < 22	mA mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)			
with bootstrap:			
V_P = 16 V; R_L = 4 Ω	P_o	typ. 6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	> 3,6 typ. 4,2	W W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
without bootstrap:			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 3,0	W
Voltage gain:			
preamplifier (note 2)	G_{v1}	typ. 23 21 to 25	dB dB
power amplifier	G_{v2}	typ. 29 27 to 31	dB dB
total amplifier	$G_{v\,tot}$	typ. 52 50 to 54	dB dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ. 0,3 < 1	% %
Frequency response; −3 dB (note 3)	B	60 Hz to 15	kHz
Input impedance:			
preamplifier (note 4)	$\lvert Z_{i1} \rvert$	> 100 typ. 200	kΩ kΩ
power amplifier	$\lvert Z_{i2} \rvert$	typ. 20	kΩ
Output impedance preamplifier	$\lvert Z_{o1} \rvert$	typ. 1	kΩ
Output voltage preamplifier (r.m.s. value)			
d_{tot} < 1% (note 2)	$V_{o(rms)}$	> 0,7	V
Noise output voltage (r.m.s. value; note 5)			
R_S = 0 Ω	$V_{n(rms)}$	typ. 0,2	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ. 0,6 < 1,4	mV mV
Noise output voltage at f = 500 kHz (r.m.s. value)			
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ. 8	μV
Ripple rejection (note 6)			
f = 1 to 10 kHz	RR	typ. 42	dB
f = 100 Hz; C2 = 1 μF	RR	> 35	dB
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ. 35	mA

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at P_o = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

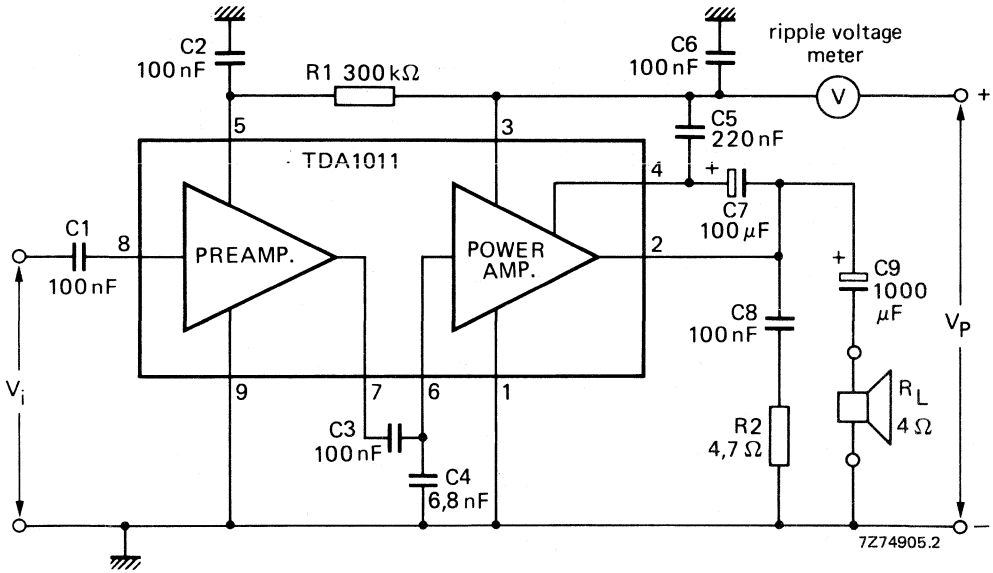


Fig. 3 Test circuit.

APPLICATION INFORMATION

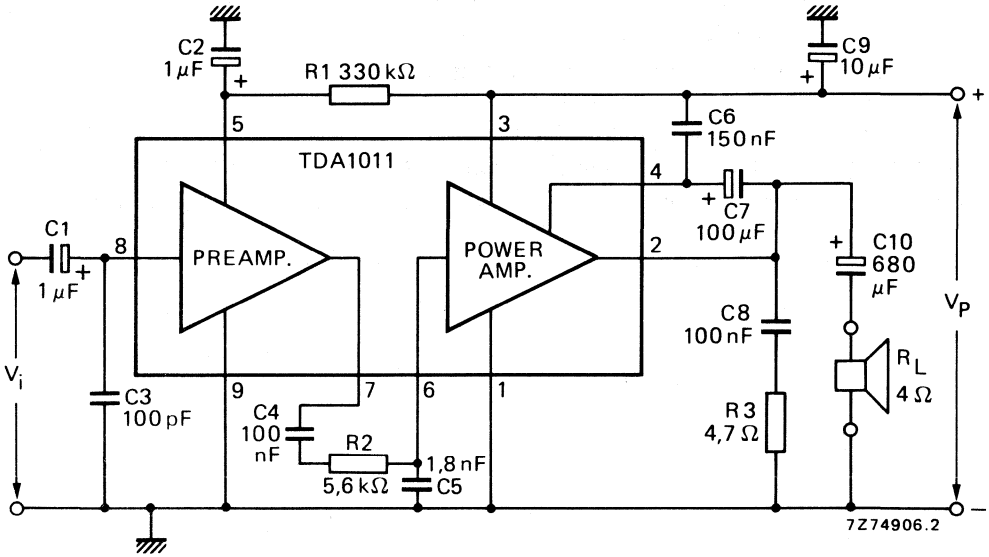


Fig. 4 Circuit diagram of a 4 W amplifier.

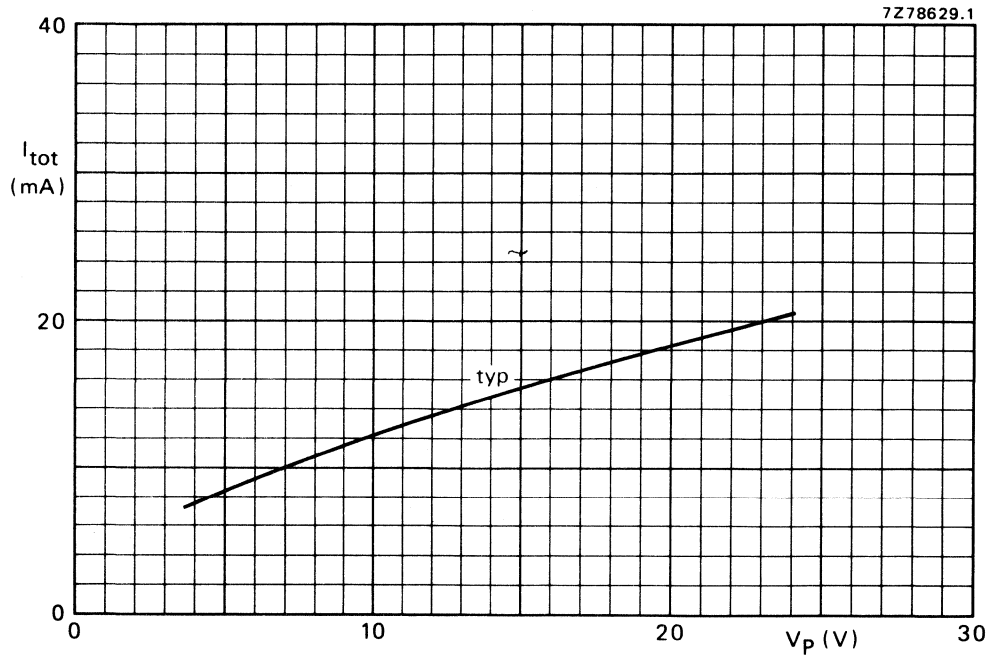


Fig. 5 Total quiescent current as a function of supply voltage.

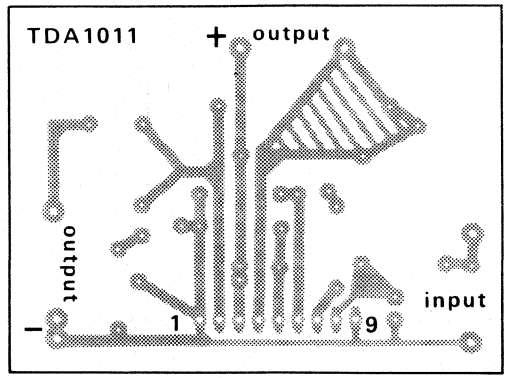


Fig. 6 Track side of printed-circuit board used for the circuit of Fig. 4; p.c. board dimensions 62 mm x 48 mm.

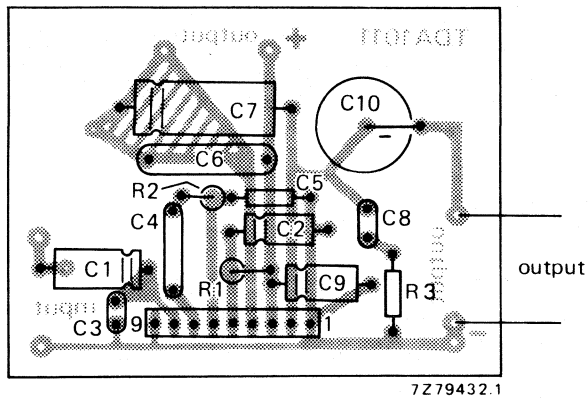


Fig. 7 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

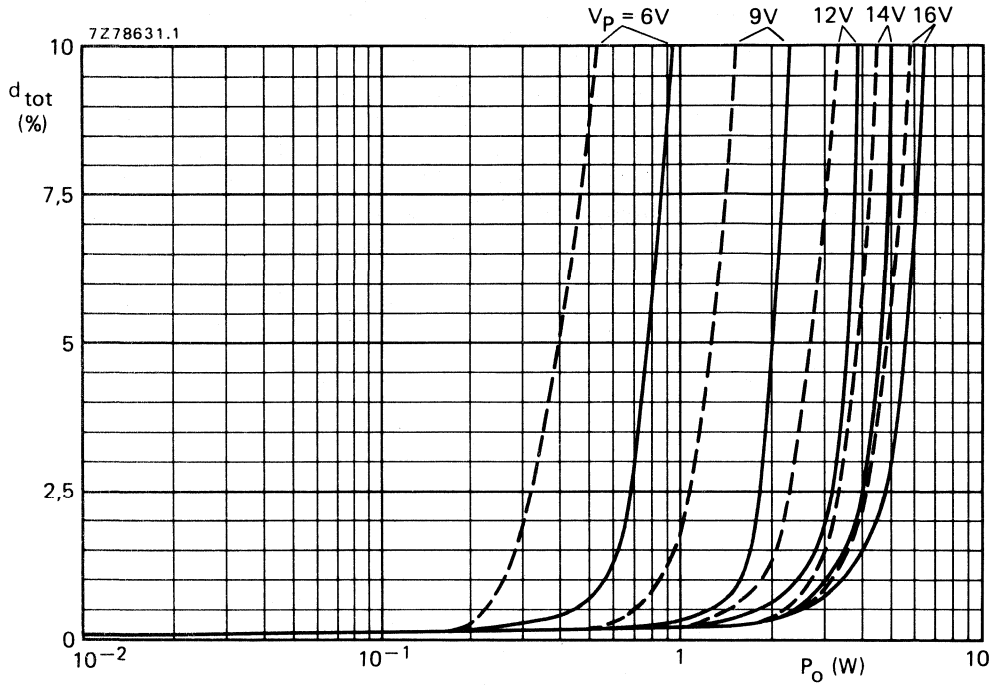


Fig. 8 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; – – – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

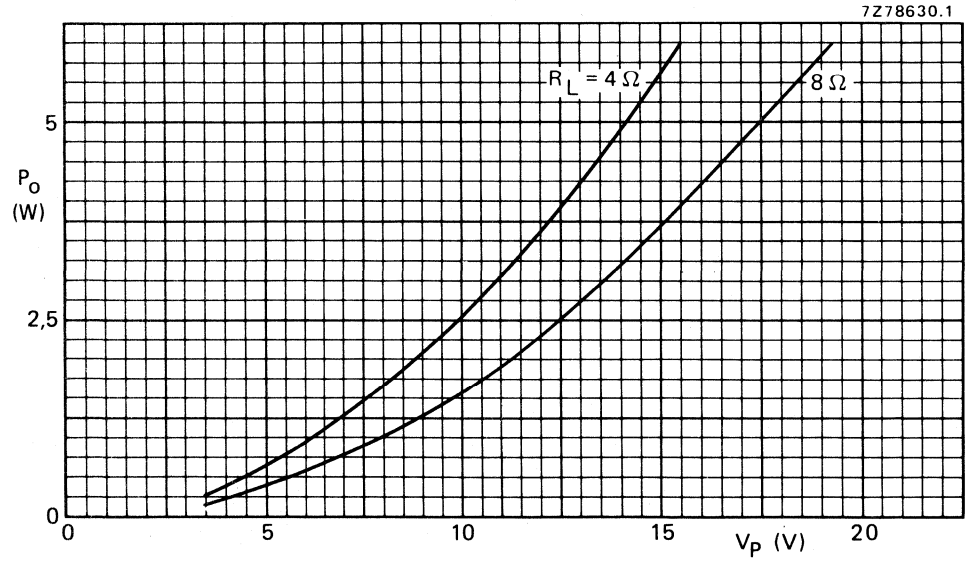


Fig. 9 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

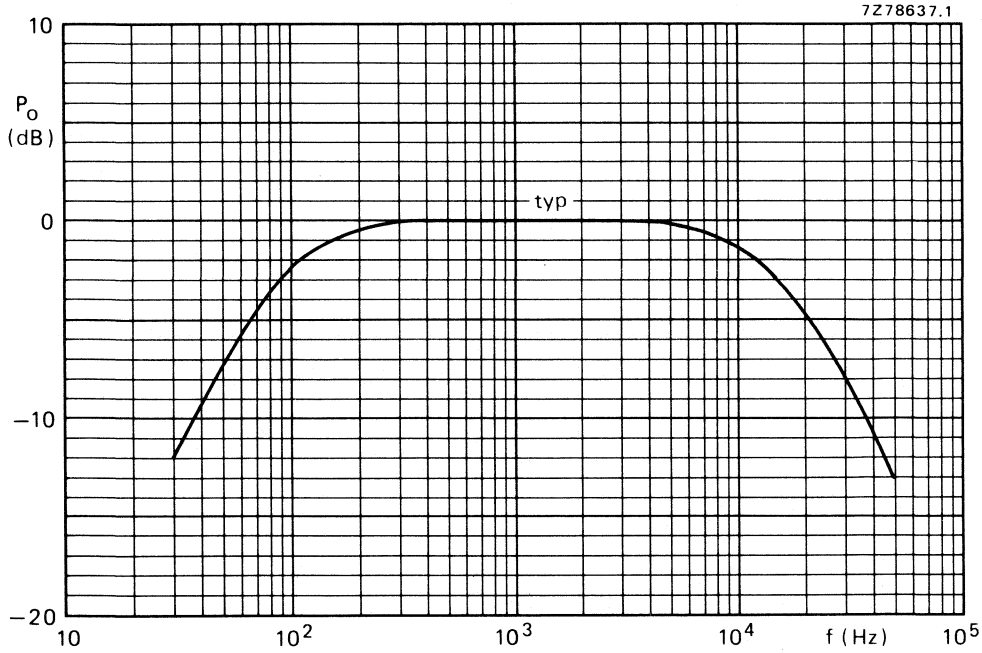


Fig. 10 Voltage gain as a function of frequency; P_o relative to 0 dB = 1 W; V_P = 12 V; R_L = 4 Ω.

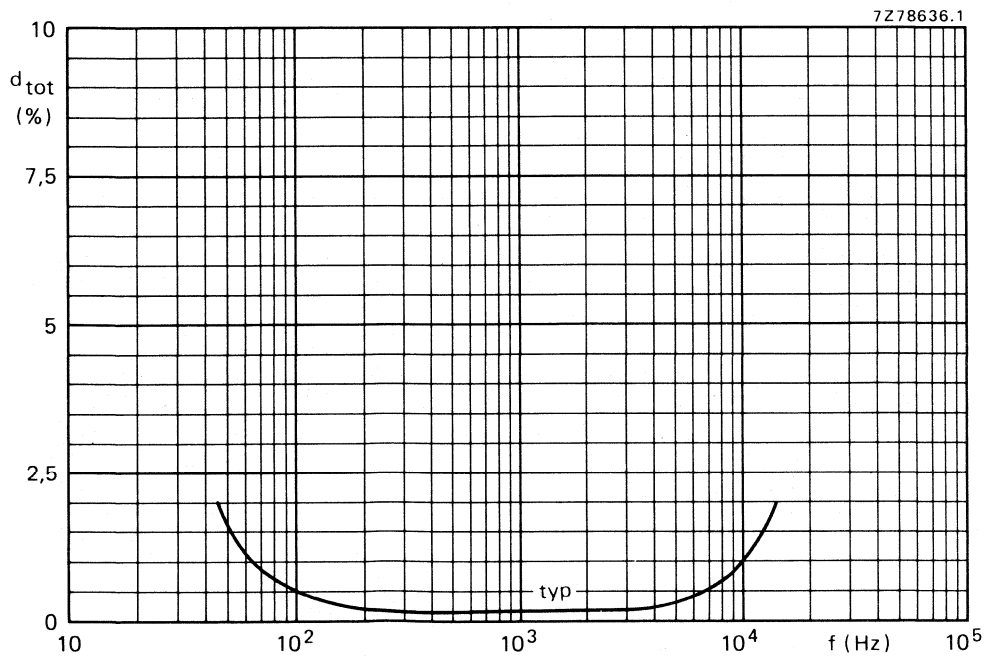


Fig. 11 Total harmonic distortion as a function of frequency; P_o = 1 W; V_P = 12 V; R_L = 4 Ω.

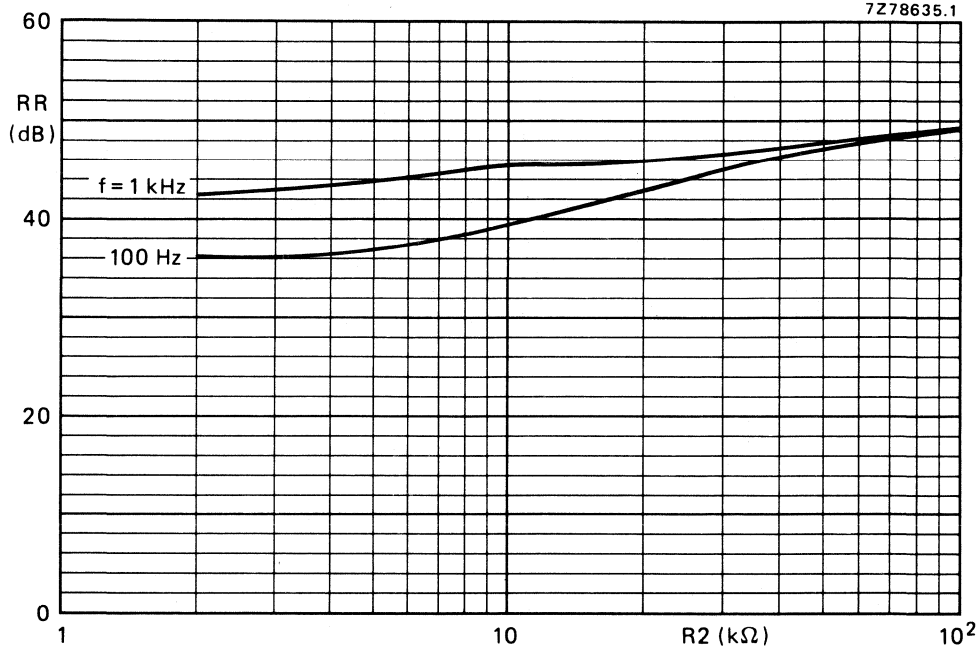


Fig. 12 Ripple rejection as a function of R2 (see Fig. 4); $R_S = 0$; typical values.

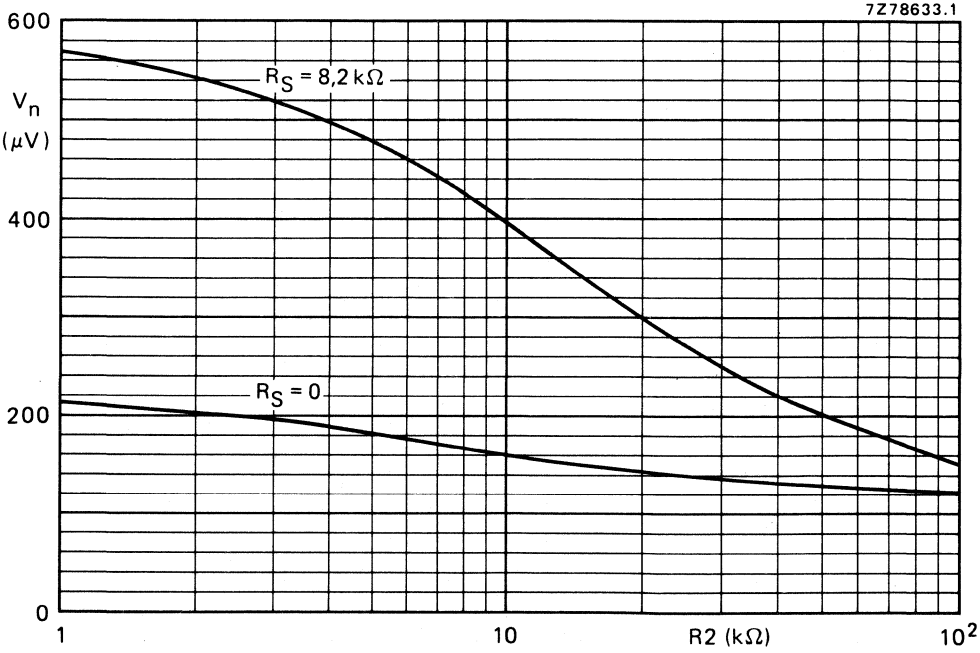


Fig. 13 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

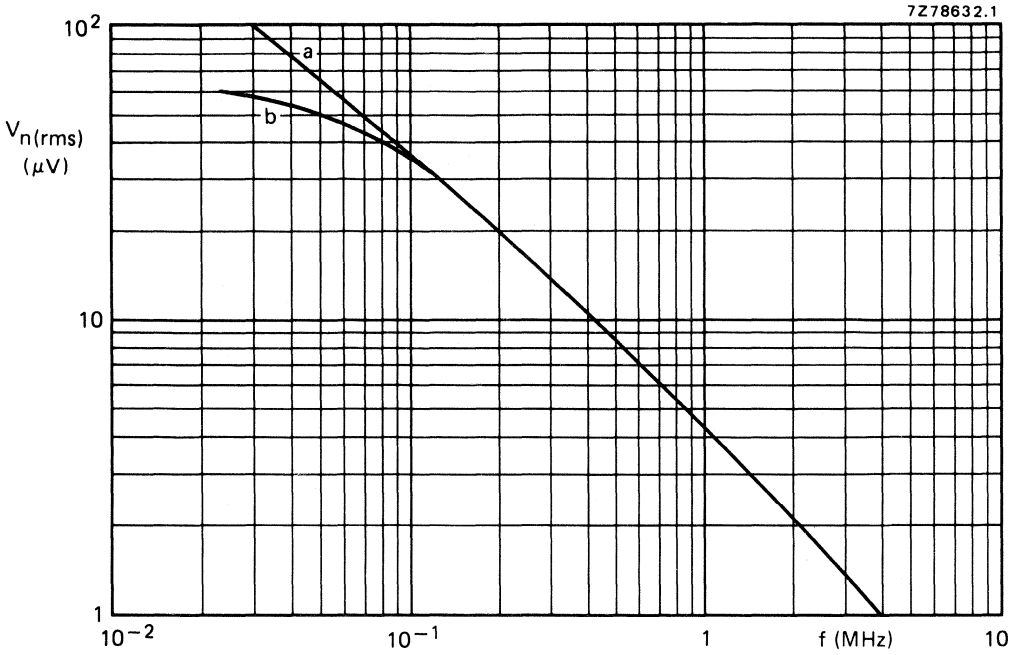


Fig. 14 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

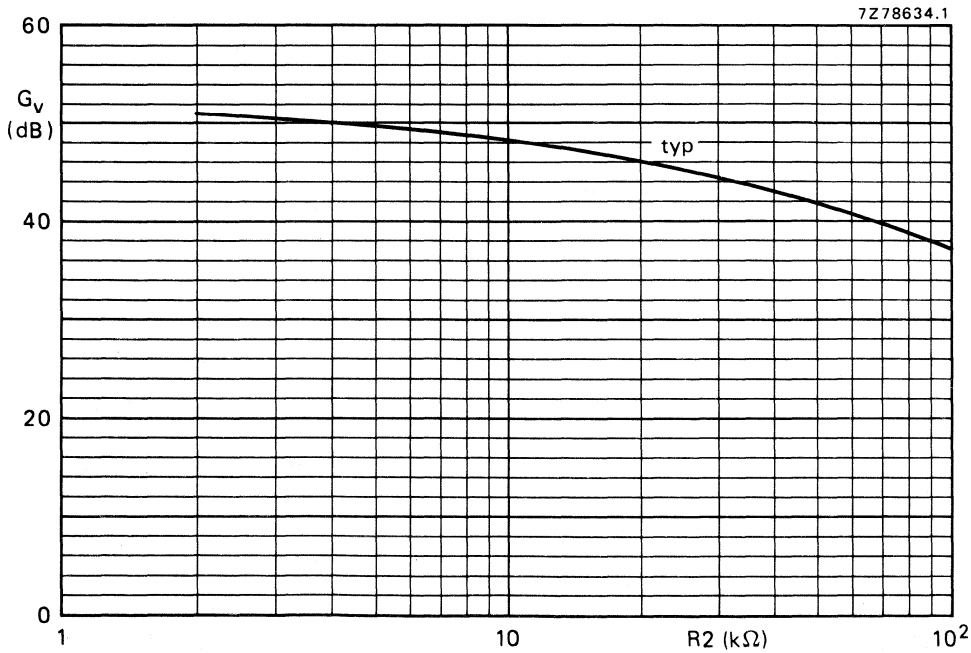


Fig. 15 Voltage gain as a function of R2 (see Fig. 4).

2 TO 6 W AUDIO POWER AMPLIFIER

The TDA1011A is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The device can deliver up to 6 W into 4 Ω at 16 V loaded supply in mains-fed applications. The maximum permissible supply voltage of 24 V makes this circuit very suitable for d.c. and a.c. apparatus, while the low applicable supply voltage of 5,4 V permits 9 V applications. The power amplifier has an inverted input/output which makes the circuit optimal for applications with active tone control and spatial stereo. Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P		5,4 to 20	V
Peak output current	I_{OM}	max.	3	A
Output power at d_{tot} = 10%				
V_P = 16 V; R_L = 4 Ω	P_o	typ.	6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2	%
Input impedance preamplifier (pin 8)	$\lvert Z_i \rvert$	>	100	kΩ
Total quiescent current	I_{tot}	typ.	14	mA
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

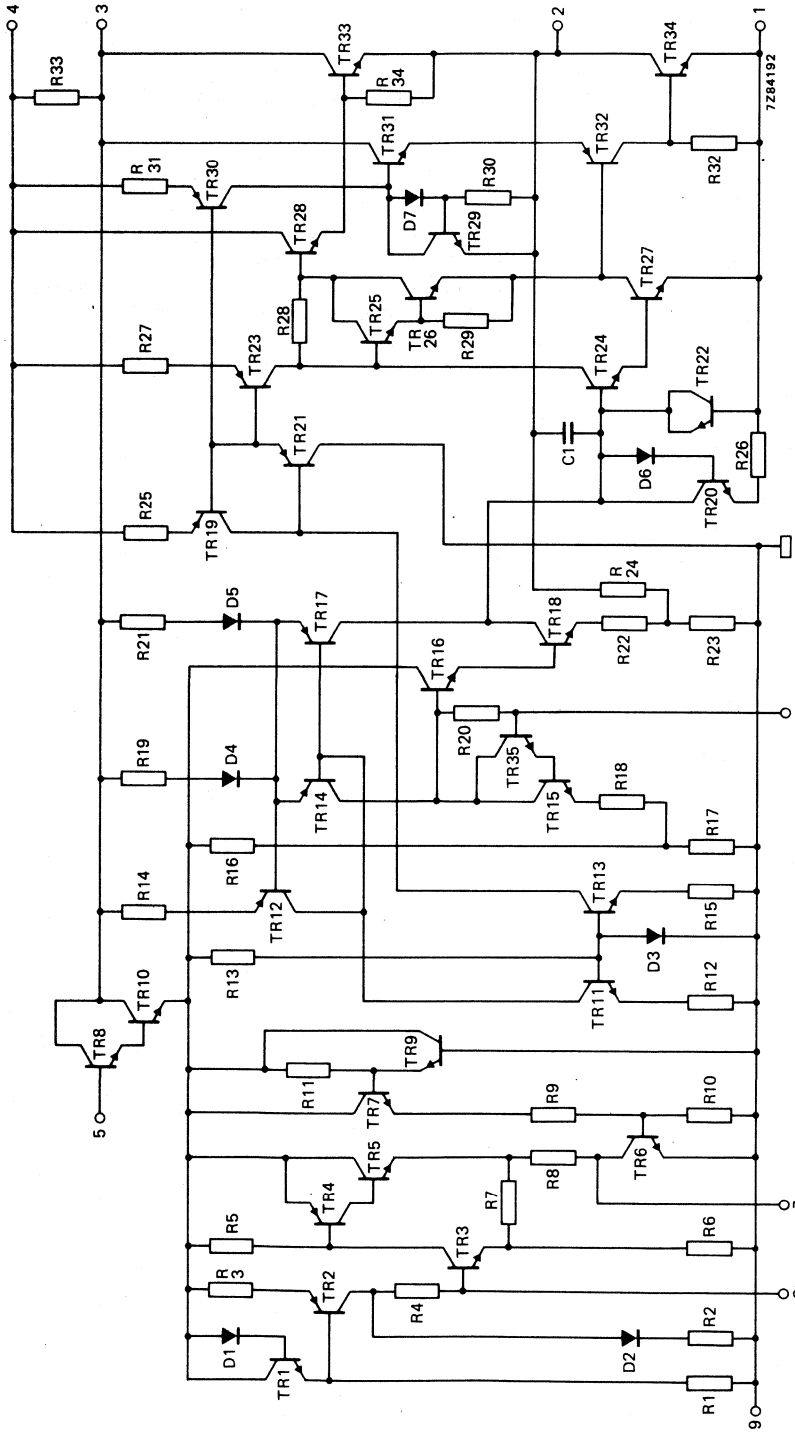


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24 V
Peak output current	I_{OM}	max.	3 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100 hours

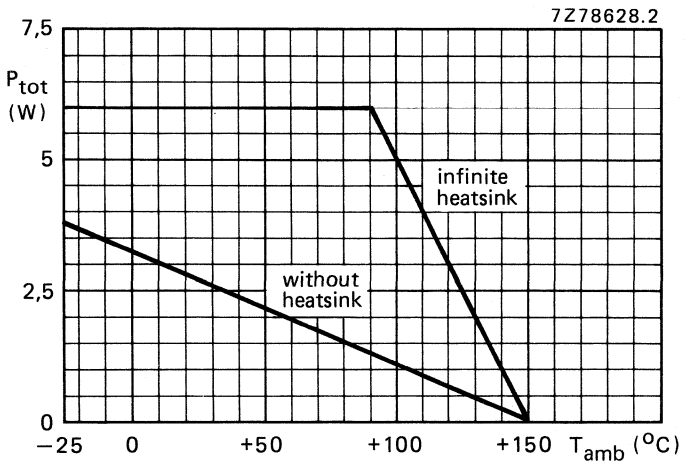


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 12 V; R_L = 4 Ω; T_{amb} = 60 °C maximum; P_o = 3,8 W.

The maximum sine-wave dissipation is 1,8 W.

The derating of 10 K/W of the package requires the following external heatsink (for sine-wave drive):

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{1{,}8} = 50\ \text{K/W}.$$

Since $R_{th\ j\text{-}tab}$ = 10 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 50 − (10 + 1) = 39 K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P	5,4 to 20	V
Repetitive peak output current	I_{ORM}	< 2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ. 14 < 22	mA mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)			
with bootstrap:			
V_P = 16 V; R_L = 4 Ω	P_o	typ. 6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	> 3,6 typ. 4,2	W W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
without bootstrap:			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 3,5	W
Voltage gain:			
preamplifier (note 2)	G_{v1}	typ. 23 21 to 25	dB dB
power amplifier (note 3)	G_{v2}	typ. 29	dB
total amplifier (note 3)	$G_{v\,tot}$	typ. 52	dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ. 0,3 < 1	% %
Frequency response; −3 dB (note 4)	B	60 Hz to 15	kHz
Input impedance:			
preamplifier (note 5)	$\lvert Z_{i1} \rvert$	> 100 typ. 200	kΩ kΩ
Output impedance preamplifier	$\lvert Z_{o1} \rvert$	typ. 1	kΩ
Output voltage preamplifier (r.m.s. value)			
d_{tot} < 1% (note 2)	$V_{o(rms)}$	> 1,2	V
Noise output voltage (r.m.s. value; note 6)			
R_S = 0 Ω	$V_{n(rms)}$	typ. 0,5	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ. 0,8	mV
Noise output voltage at f = 500 kHz (r.m.s. value)			
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ. 8	μV
Ripple rejection (note 6)			
f = 1 to 10 kHz	RR	typ. 42	dB
f = 100 Hz; C2 = 1 μF	RR	> 35	dB
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ. 35	mA
Stand-by current at maximum V_P (note 8)	I_{sb}	< 100	μA

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured with R2 = 20 kΩ.
4. Measured at P_O = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
5. Independent of load impedance of preamplifier.
6. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
7. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude: 2 V).
8. The total current when disconnecting pin 5 or short-circuited to ground (pin 9).
9. The tab must be electrically floating or connected to the substrate (pin 9).

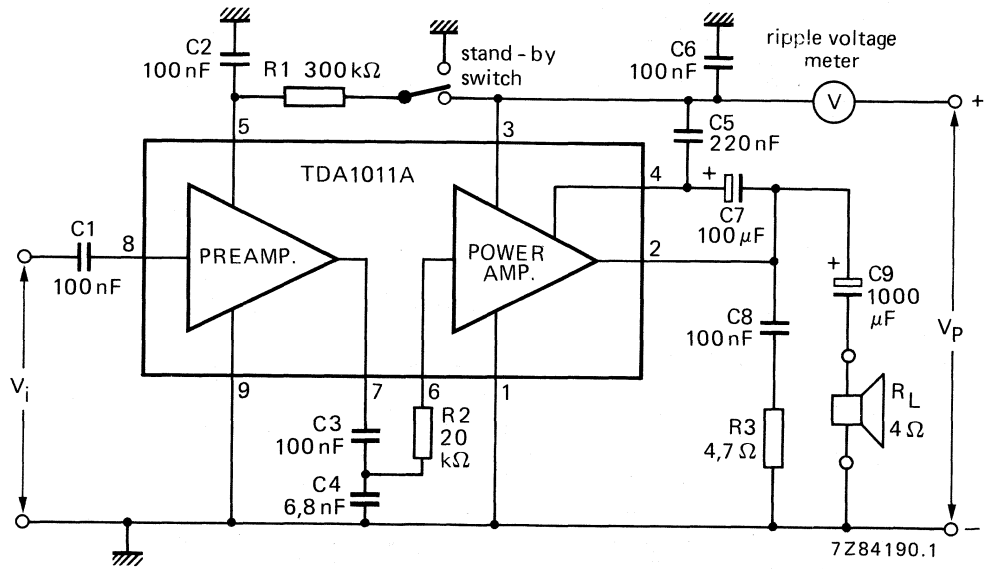


Fig. 3 Test circuit.

APPLICATION INFORMATION

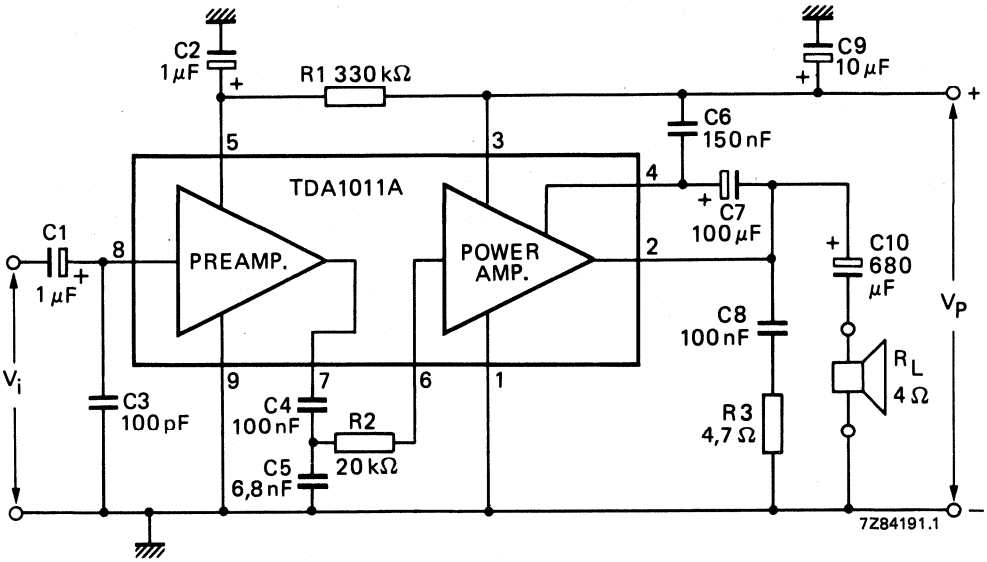


Fig. 4 Circuit diagram of a 4 W amplifier.

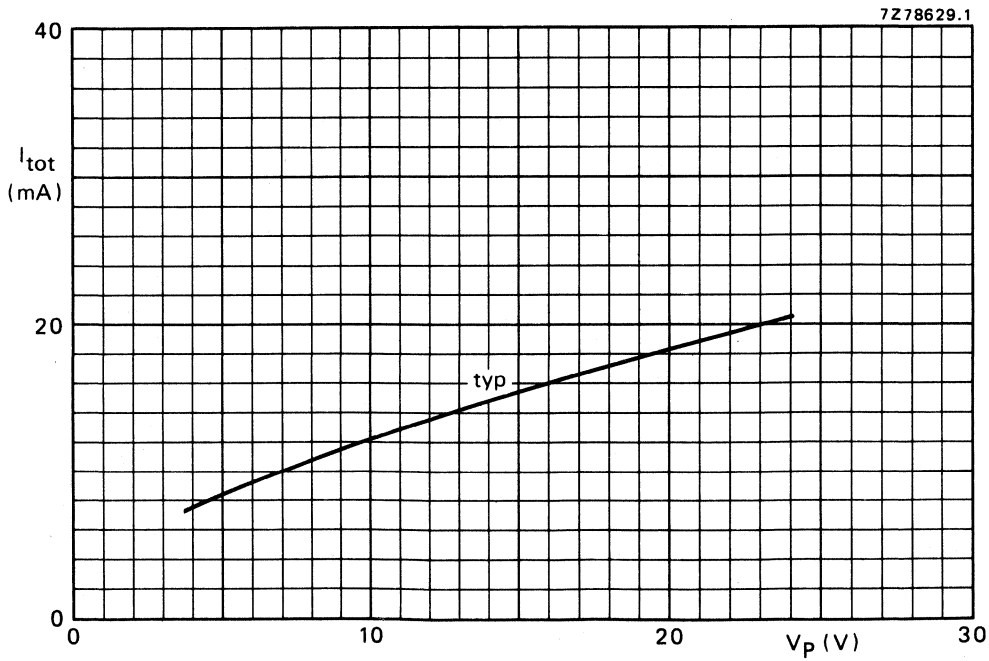


Fig. 5 Total quiescent current as a function of supply voltage.

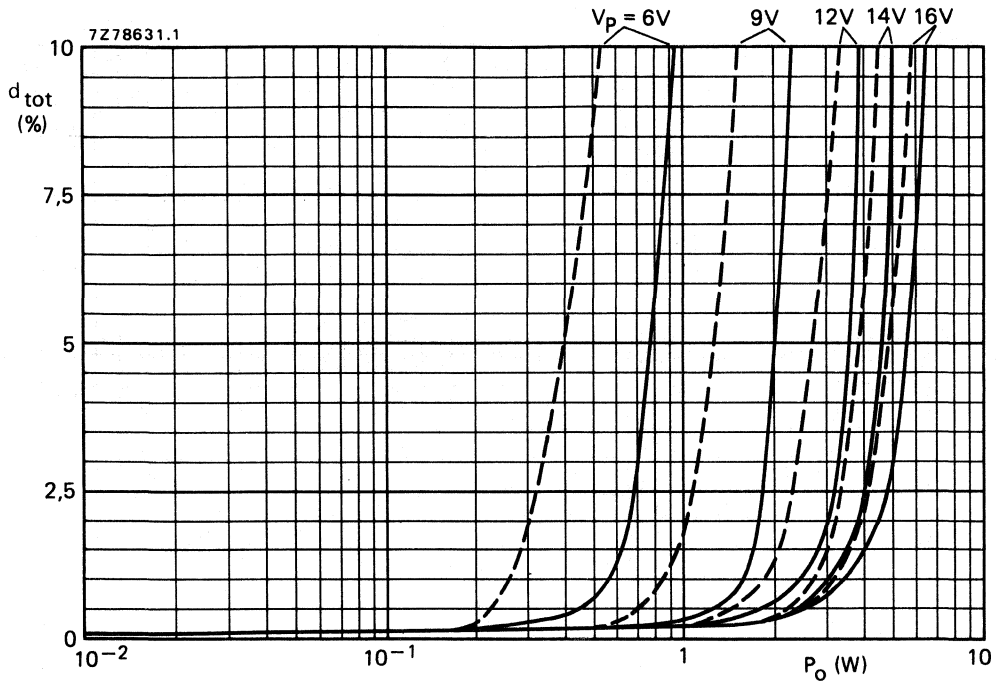


Fig. 6 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; — — — without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

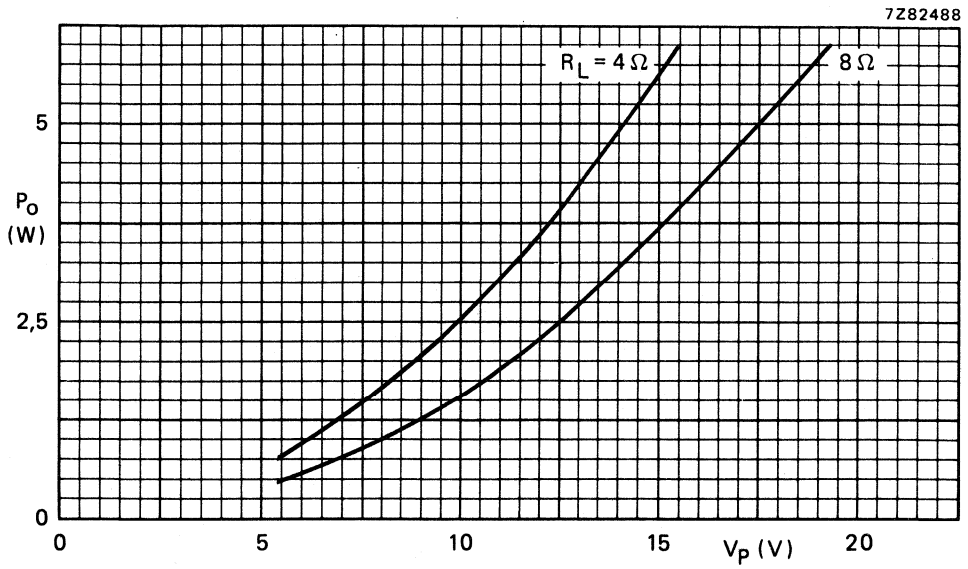


Fig. 7 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C1

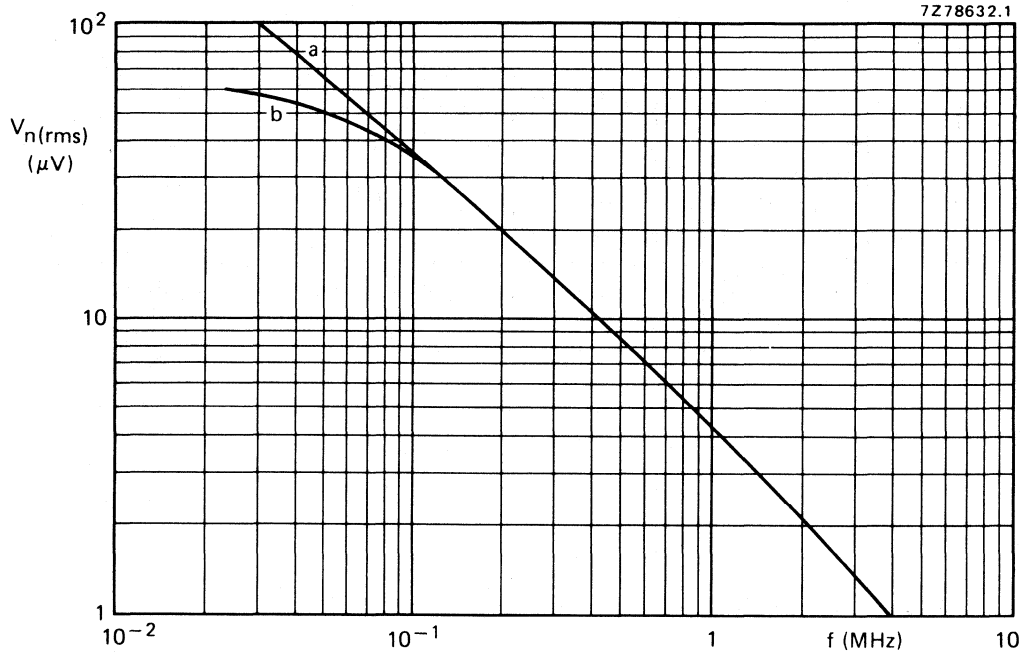


Fig. 8 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

0,5 W AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1015T is a low-cost audio amplifier which can deliver up to 0,5 W output power into a 16 Ω load impedance at a supply voltage of 9 V. The amplifier is specially designed for portable applications such as radios and recorders. The IC has a very low supply voltage requirement (3,6 V min.).

Features

- High input impedance
- Separated preamplifier and power amplifier
- Limited noise behaviour at radio frequencies
- Short-circuit protected
- Miniature encapsulation

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 12	V
Peak output current	I_{OM}	max.	1	A
Output power	P_o	typ.	0,5	W
Voltage gain power amplifier	G_{v1}	typ.	29	dB
Voltage gain preamplifier	G_{v2}	typ.	23	dB
Total quiescent current	I_{tot}	max.	22	mA
Operating ambient temperature range	T_{amb}		−25 to +150	°C
Storage temperature range	T_{stg}		−55 to +150	°C

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

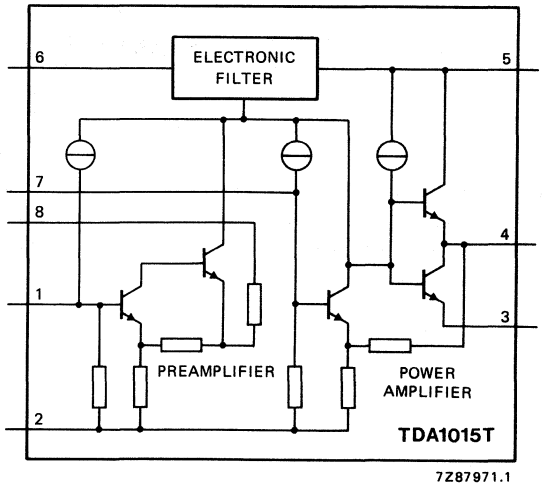


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	12 V
Peak output current	I_{OM}	max.	1 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range			−55 to +150 °C
A.C. short-circuit duration of load during sine-wave drive at V_P = 9 V	t_{sc}	max.	1 hour

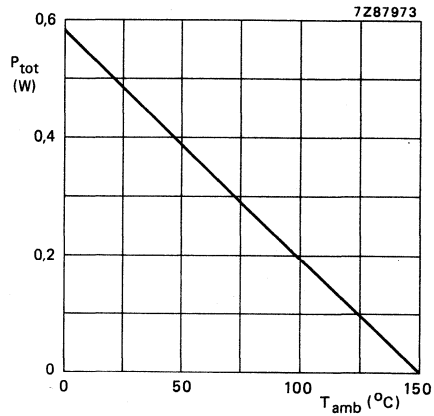


Fig. 2 Power derating curve.

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 9 V; R_L = 16 Ω; f = 1 kHz; see Fig. 3; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_P	3,6	9	12	V
Repetitive peak output current	I_{ORM}	–	–	1	A
Total quiescent current	I_{tot}	–	12	22	mA
A.F. output power at d_{tot} = 10% (note 1)					
V_P = 9 V; R_L = 16 Ω	P_o	–	0,5	–	W
V_P = 6 V; R_L = 8 Ω	P_o	–	0,3	–	W
Voltage gain power amplifier	G_{v1}	–	29	–	dB
Voltage gain preamplifier (note 2)	G_{v2}	–	23	–	dB
Total voltage gain	G_{tot}	49	52	55	dB
Frequency response at −3 dB (note 3)	B	–	60 to 15 000	–	Hz
Input impedance power amplifier	$\|Z_{i1}\|$	–	20	–	kΩ
Input impedance preamplifier (note 4)	$\|Z_{i2}\|$	100	200	–	kΩ
Output impedance preamplifier	$\|Z_{o2}\|$	0,5	1	1,5	kΩ
Output voltage preamplifier (r.m.s. value) $d_{tot} < 1\%$ (note 2)	$V_{o2(rms)}$	–	0,7	–	V
Noise output voltage (r.m.s. value) (note 5)					
R_S = 0 Ω	$V_{n(rms)}$	–	0,2	–	mV
R_S = 10 kΩ	$V_{n(rms)}$	–	0,5	–	mV
Noise output voltage (r.m.s. value) f = 500 kHz; B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	–	8	–	μV
Ripple rejection at f = 100 Hz; C2 = 1 μF (note 6)	RR	–	38	–	dB

Notes to the characteristics

1. Output power is measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistance of 20 kΩ.
3. The frequency response is mainly determined by the capacitors, C1, C3 (low frequency) and C4 (high frequency).
4. Independent of load impedance of preamplifier.
5. Effective unweighted r.m.s. noise voltage measured in a bandwidth from 60 Hz to 15 kHz (slopes 12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude of 2 V).

APPLICATION INFORMATION

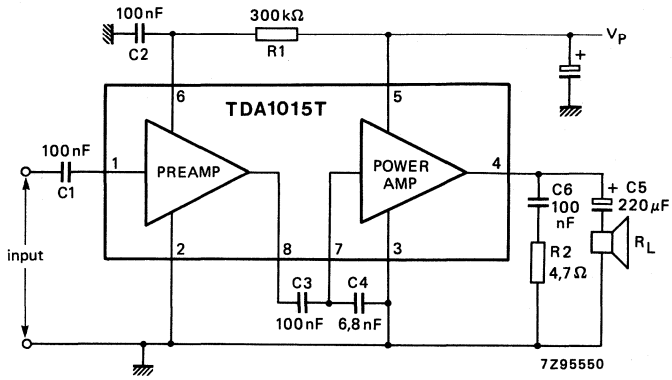


Fig. 3 Test circuit.

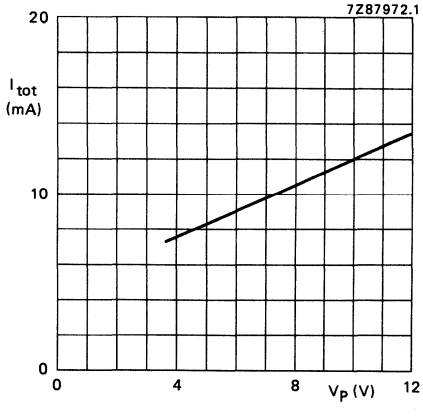


Fig. 4 Total quiescent current as a function of supply voltage.

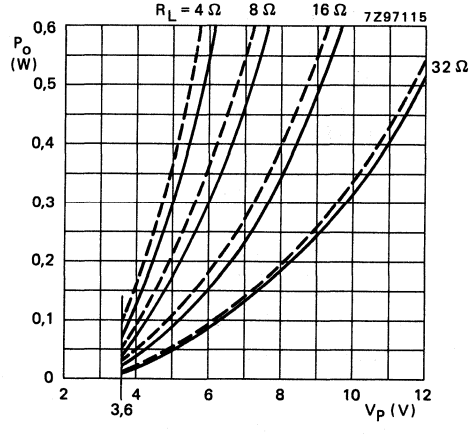


Fig. 5 Output power as a function of supply voltage; d_{tot} = 10%; f = 1 kHz.
——— measured in Fig. 3
– – – – measured with a 1,5 MΩ resistor connected between pins 7 and 2.

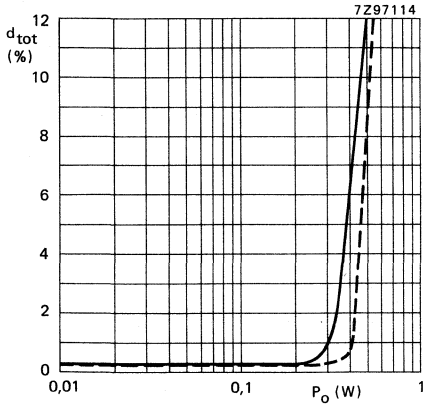


Fig. 6 Total distortion as a function of output power; V_P = 9 V; R_L = 16 Ω; f = 1 kHz.
——— measured in Fig. 3
– – – – – measured with a 1,5 MΩ resistor connected between pins 7 and 2.

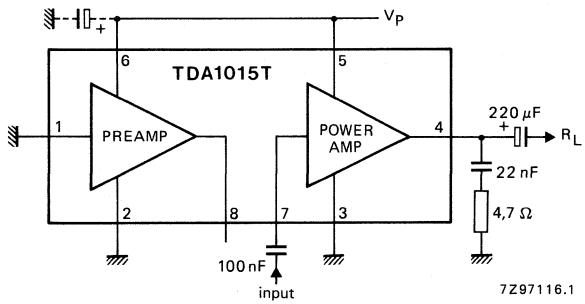


Fig. 7 Application circuit for power stage only and battery power supply; G_{v1} = 29 dB; $|Z_{i1}|$ = 20 kΩ.

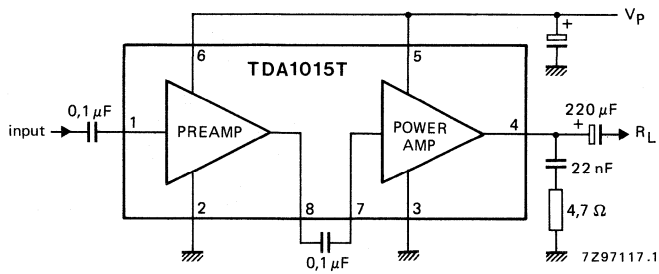


Fig. 8 Application circuit for preamplifier and power amplifier stages and battery power supply; $G_{v\,tot}$ = 52 dB; $|Z_{i2}|$ = 200 kΩ.

FM/IF AMPLIFIER CIRCUIT

The TDA1576 is a monolithic integrated f.m./i.f. amplifier circuit provided with the following functions:

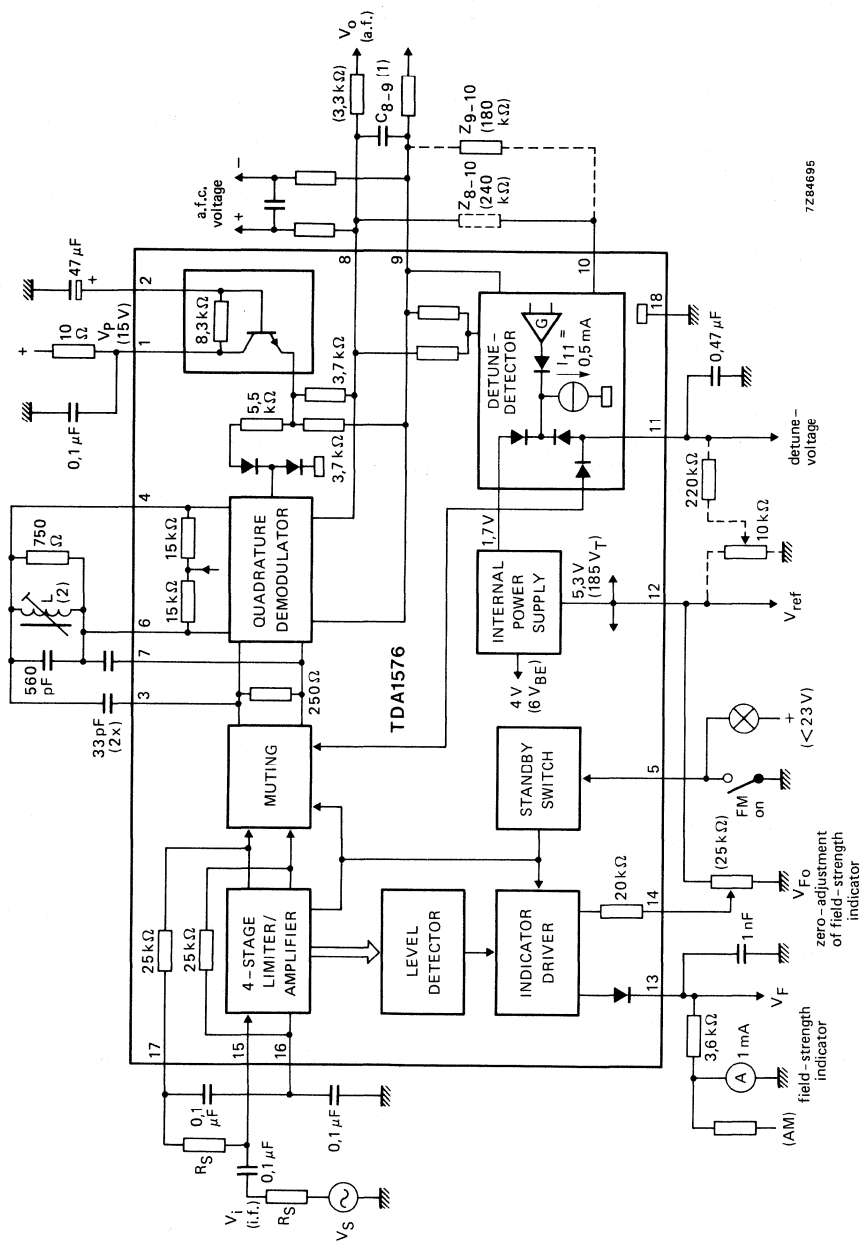
- symmetrical limiting i.f. amplifier
- symmetrical quadrature demodulator
- internal muting circuit
- symmetrical a.f.c. output
- field-strength indication output
- detune-detector
- reference voltage output
- electronic smoothing of the supply voltage
- standby on/off switching circuit.

QUICK REFERENCE DATA

f_o = 10,7 MHz; Δf = ± 22,5 kHz; f_m = 400 Hz; Q_L = 20; de-emphasis τ = 50 μs					
Supply voltages (pin 1)	V_P		8,5	15	V
Supply current	I_P	typ.	16	18	mA
Sensitivity at −3 dB before limiting	V_i	typ.	22		μV
I.F. sensitivity for					
S + N/N = 26 dB	V_i	typ.	8		μV
S + N/N = 46 dB	V_i	typ.	35		μV
A.F. output voltage	V_o	typ.	67	135	mV
Total distortion					
single tuned circuit	d_{tot}	typ.	0,1		%
two tuned circuits	d_{tot}	typ.	0,02		%
Signal plus noise-to-noise ratio; $V_i > 1$ mV	S + N/N	typ.	76	80	dB
A.M. rejection	α	typ.	50		dB
A.F.C. offset drift	$\pm \Delta f$	typ.	3		kHz
		<	6		kHz
Field-strength indication range	ΔV_i	typ.	90		dB
Permissible indicator (load) current	I_L	<	2		mA
Supply voltage range (pin 1)	V_P		7,5 to 20		V
Ambient temperature range	T_{amb}		−30 to +80		°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) For de-emphasis $\tau = 50\ \mu s$: $C_{8\text{-}9} = 6{,}8$ nF.
For stereo operation: $C_{8\text{-}9} = 56$ pF.

(2) L = 0,38 μH; $Q_o = 70$; $Q_L = 20$; adjusted to minimum 2nd harmonic distortion (d_2); at $V_i = 1$ mV; coil: 6 turns CuL (0,25 mm) on coil former KAN (C).

Fig. 1 Block diagram and test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-18}$	max.	23	V
Voltages				
at pin 2	V_{2-18}	max.	V_P	V
	$-V_{2-18}$	max.	0	V
at pin 5	V_{5-18}	max.	23	V
	$-V_{5-18}$	max.	0	V
at pin 12	V_{12-18}	max.	7	V
	$-V_{12-18}$	max.	0	V
at pin 13	V_{13-18}	max.	6	V
at pin 14	V_{14-18}	max.	23	V
	$-V_{14-18}$	max.	0	V
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr\text{-}a}$	=	80	K/W

CHARACTERISTICS

f_o = 10,7 MHz; Δf = ± 22,5 kHz; f_m = 400 Hz; R_S = 60 Ω; de-emphasis τ = 50 μs (C_{8-9} = 6,8 nF); T_{amb} = 25 °C; measured in Fig. 1, unless otherwise specified. The demodulator circuit is adjusted at minimum 2nd harmonic (d_2) distortion: V_i = 1 mV; Δf = ± 75 kHz.

Supply voltage range (pin 1)		V_P		7,5 to 20	V
		V_P = 8,5 V		V_P = 15 V	
Supply current; without load ($I_{12} = I_{13} = 0$)	I_P	typ.	16	18	mA
			10 to 23	12 to 25	mA
I.F. amplifier/detector					
Sensitivity at −3 dB before limiting	V_i	typ.	22		μV
		<	30		μV
I.F. sensitivity for					
S + N/N = 26 dB	V_i	typ.	8		μV
S + N/N = 46 dB	V_i	typ.	35		μV
I.F. output voltage (peak-to-peak value)					
V_i = 1 mV; $Z_{3-18} = Z_{7-18}$ = 1 MΩ in parallel with 10 pF	$V_{3-7(p-p)}$	typ.	680		mV
I.F. output resistance	R_{3-7}	typ.	250		Ω
Detector input impedance	R_{4-6}	typ.	30		kΩ
	C_{4-6}	typ.	1		pF
Output resistance	R_8; R_9	typ.	3,7		kΩ
D.C. output voltage	$V_{8-18} = V_{9-18}$	typ.	5,5	9,8	V
A.F. output voltage; Q_L = 20	V_o	typ.	67	135	mV
			60 to 75	120 to 150	mV
Total distortion					
single tuned circuit; Q_L = 20	d_{tot}	typ.	0,1		%
two tuned circuits	d_{tot}	typ.	0,02		%
Signal plus noise-to-noise ratio					
B = 250 Hz to 15 kHz; V_i > 1 mV	S + N/N	typ.	76	80	dB
A.M. rejection; V_i = 10 mV					
f.m.: f_m = 70 Hz; Δf = ± 22,5 kHz					
a.m.: f_m = 1 kHz; m = 0,3	α	typ.	54		dB*
I.F. input voltage range; α > 40 dB	V_i		0,5 to 500		mV
Hum suppression at f = 100 Hz					
$V_P = V_{1-18}$ = 100 mV r.m.s.; C_{2-18} = 47 μF	α_{100}	>	43		dB
		typ.	48		dB
A.F.C. tuning slope at Q_L = 20	$\frac{\Delta V_{8-9}}{\Delta f_o}$	typ.	8,5	17	mV/kHz
A.F.C. offset voltages; Q_L = 20					
at V_i = 1 mV	$\pm \Delta V_{8-9}$	<	100	200	mV
at V_i = 30 μV to 500 mV		typ.	25	50	mV
(reference at 1 mV and muting)	$\pm \Delta V_{8-9}$	<	50	100	mV

* Simultaneously measured.

Field-strength indication

			V_P = 8,5 V	V_P = 15 V	
Indicator sensitivity; I_{14} = 0	V_i		20 μV to 600 mV		
Field-strength indicator voltage					
R_{13-18} = 3,6 kΩ; I_{14} = 0					
V_i = 0	$V_F = V_{13-18}$	typ.	0		mV
		<	200		mV
V_i = 250 mV	$V_F = V_{13-18}$	typ.	3,6		V
			3,2 to 4,1		V
Available output current	$-I_{13}$	>	2		mA
Reverse voltage at the output for FM 'off'; $V_{5-18} > 3{,}5$ V	V_{13-18}	>	5		V

Detune-detector

Quiescent input current; V_{10-9} = 0	I_{10}	typ.	20		nA
		<	100		nA
Output voltage range	V_{11-18}		1,8 to 5,0		V
Available output current	I_{11}	typ.	0,5		mA
			0,35 to 0,65		mA
Voltage gain: $\Delta V_{11}/\Delta(\pm V_{10-9})$ at I_{11} = 0,25 mA	G_v	typ.	–	3,3	
Input offset voltage (pin 10) at V_{11-18} = 2,5 V	V_{10-9}	typ.	20		mV

Reference voltage

Output voltage; $-I_{12}$ = 1 mA	$V_{ref} = V_{12-18}$	typ.	5,1	5,3	V
Available output current	$-I_{12}$	typ.	2,5		mA

Standby switch

Required control voltage within the rated ambient temperature and supply voltage ranges					
for FM 'on'	$V_{5\ on}$	<	2		V
for FM 'off'	$V_{5\ off}$	>	3,5		V
Input switching current for FM 'on'	$-I_5$	<	100		μA

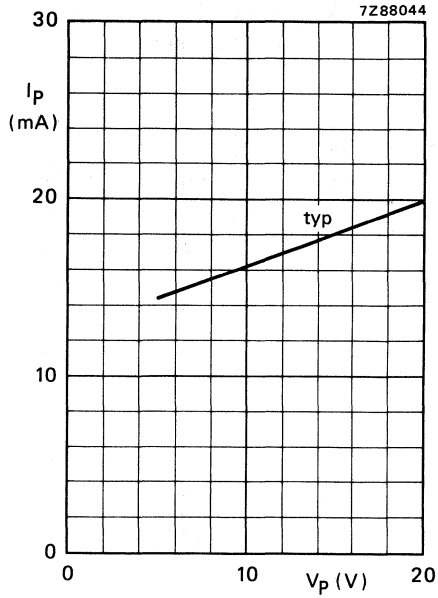


Fig. 2 Supply current consumption; without load.

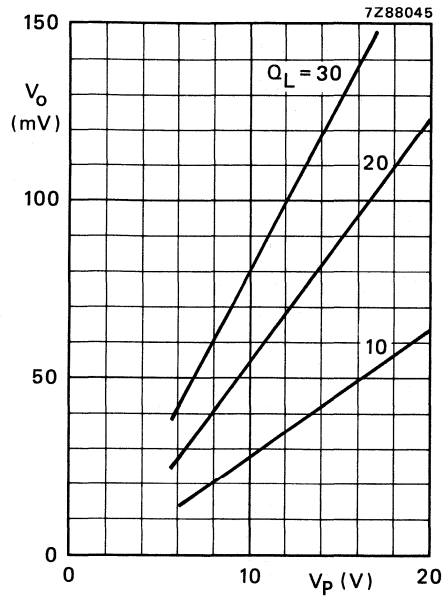


Fig. 3 A.F. output voltage; V_i = 1 mV (i.f.); Δf = ± 15 kHz; f_m = 400 Hz; typical values.

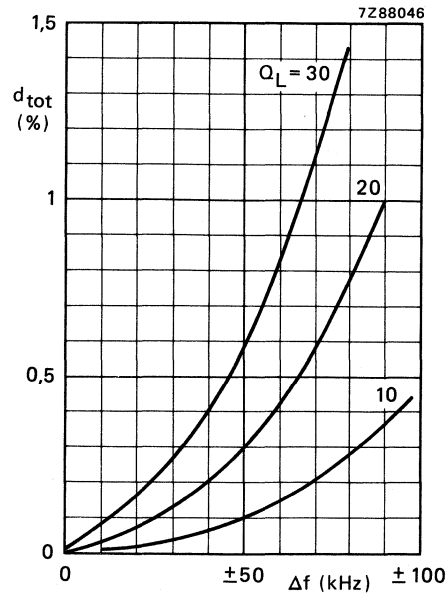


Fig. 4 Total distortion for single tuned circuit; V_i = 1 mV (i.f.); f_m = 400 Hz; adjusted at minimum 2nd harmonic distortion; typical values.

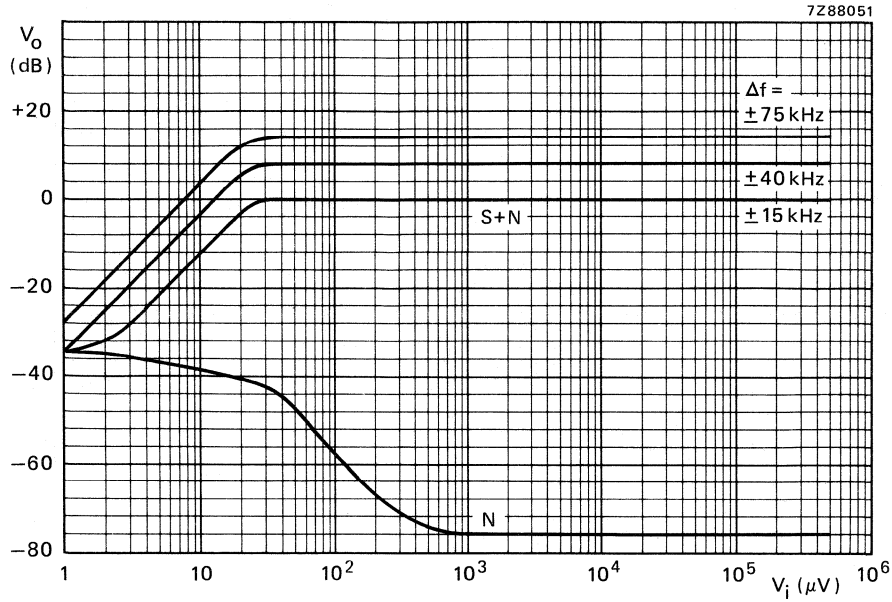


Fig. 5 A.F. output voltage level as a function of i.f. input voltage; S = signal voltage; N = noise voltage; V_P = 15 V; f_m = 400 Hz; B = 250 Hz to 16 kHz; Q_L = 20; C_{8-9} = 6,8 nF; typical values.

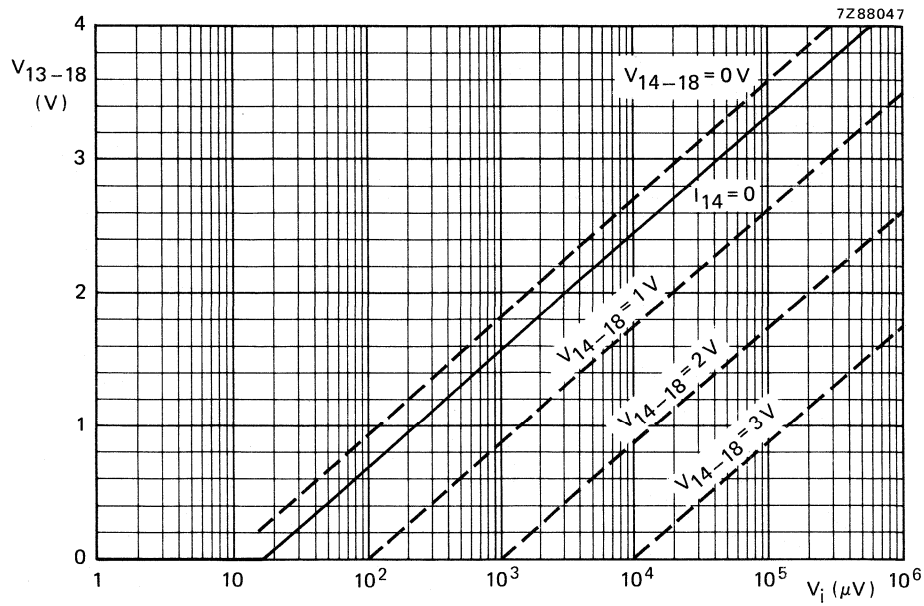


Fig. 6 Voltage at field-strength indicator output (proportional to V_{12-18}); R_{13-18} = 3,6 kΩ.

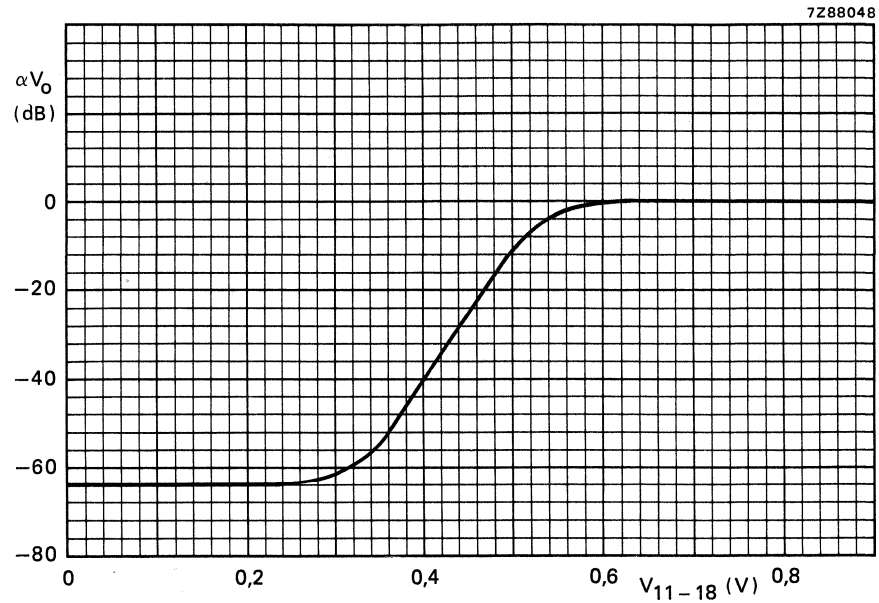


Fig. 7 Attenuation of output voltage (αV_o) as a function of the muting control voltage $V_{11\text{-}18}$.

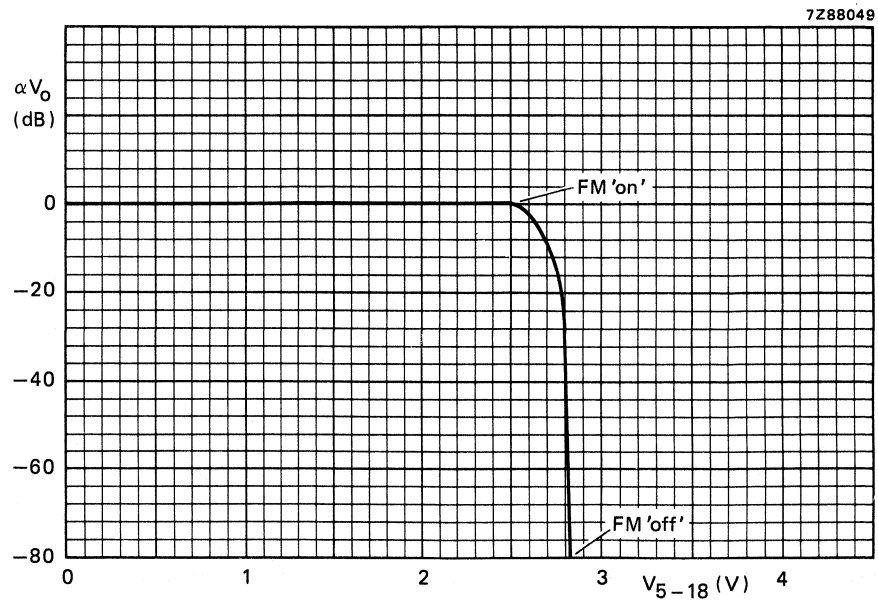
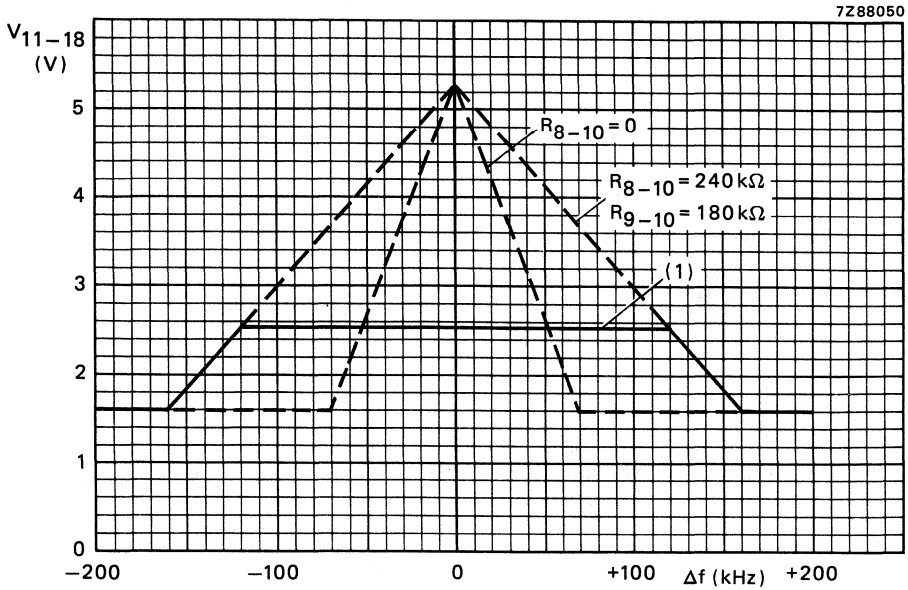


Fig. 8 FM 'on'/FM 'off' stand-by switch; attenuation of output voltage (αV_o) as a function of control voltage $V_{5\text{-}18}$.



(1) Limited by external preset ($\alpha \cdot V_{12\text{-}18}$).

Fig. 9 Detune-detector output voltage; V_P = 7,5 to 20 V; Q_L = 20.

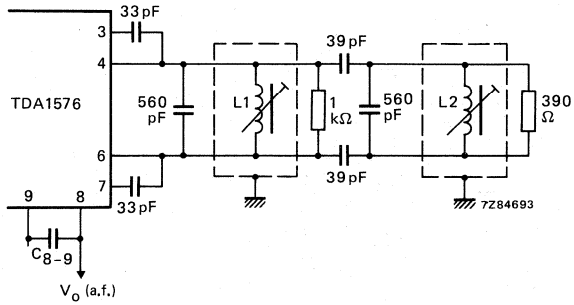


Fig. 10 Example of the TDA1576 when using a demodulator with two tuned circuits. Adjustment of the demodulator circuit is obtained with an i.f. signal which is higher than the 3 dB limiting level, L2 should be short-circuited or detuned, L1 should be adjusted to min. d_2 distortion, and then L2 to min. d_2 distortion. Coil data: L1 = L2 = 0,38 μH; Q_o = 70; coil former KAN (C).

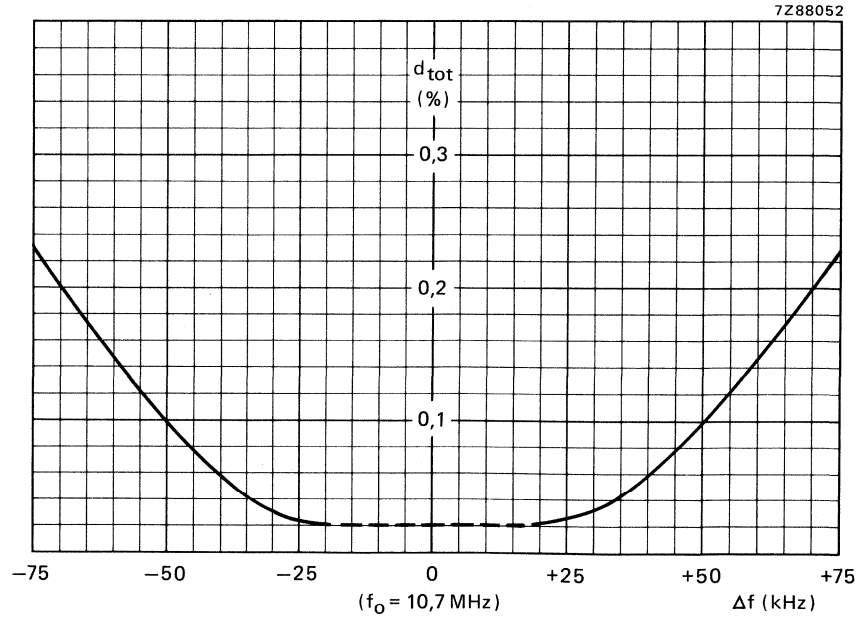
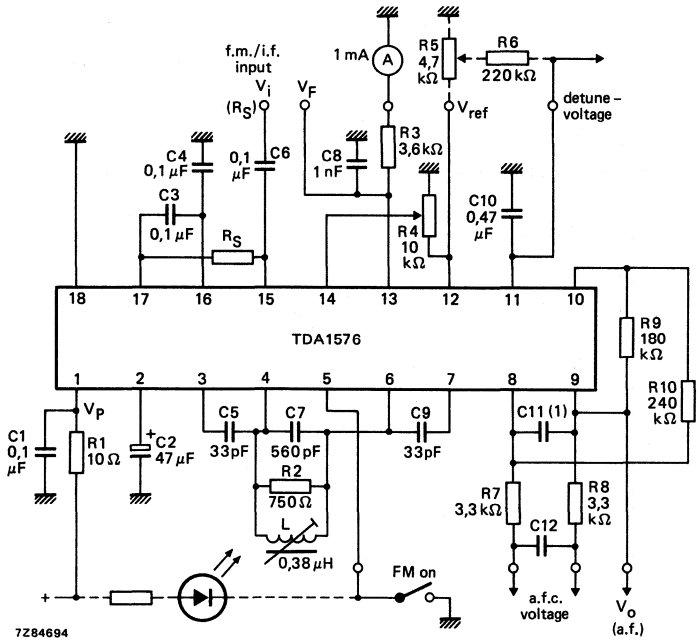


Fig. 11 Total distortion as a function of detuning; f_m = 400 Hz; C_{8-9} = 6,8 nF; $\Delta f = \pm$ 75 kHz; V_o = 330 mV for a frequency deviation $\Delta f = \pm$ 75 kHz.



(1) For mono: C11 = 6,8 nF; for stereo: C11 = 56 pF.

Fig. 12 Application example of using TDA1576.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050 is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

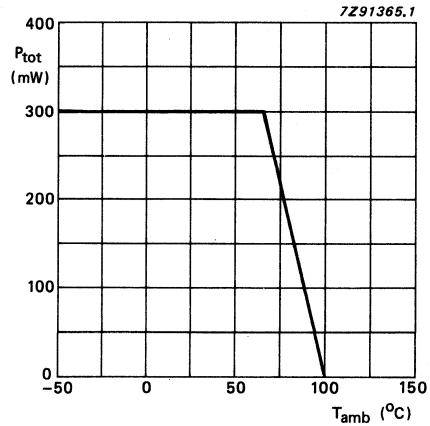


Fig. 1 Power derating curve.

THERMAL RESISTANCE

From junction to ambient $R_{thj\text{-}a}$ = 110 K/W

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\|\Delta V\|$	–	–	70	mV
Input impedance (at R_S = ∞)	$\|Z_i\|$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\|Z_i\|$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

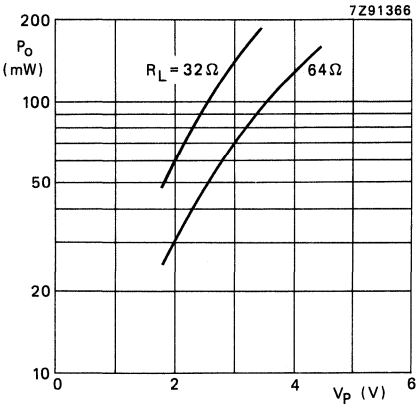


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

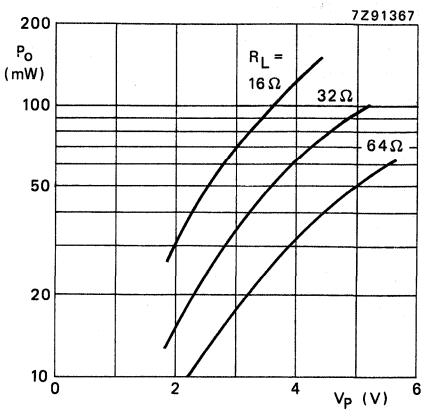


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

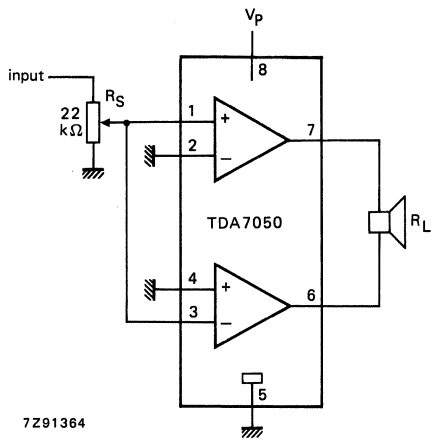


Fig. 4 Application diagram (BTL); also used as test circuit.

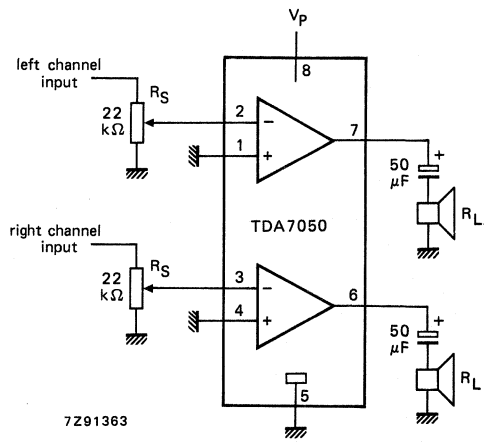


Fig. 5 Application diagram (stereo); also used as test circuit.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

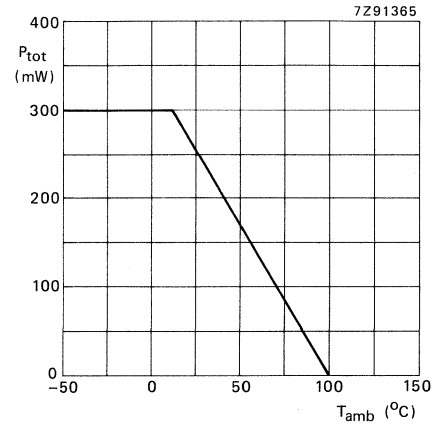


Fig. 1 Power derating curve.

SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{j\ max} - T_{amb}}{R_{th\ j\text{-}a}} = \frac{100-60}{300} = 0{,}1\ W.$$

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

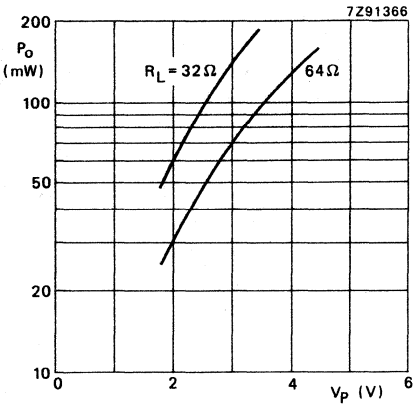


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

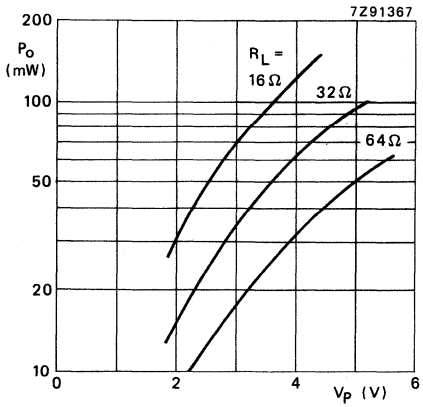


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

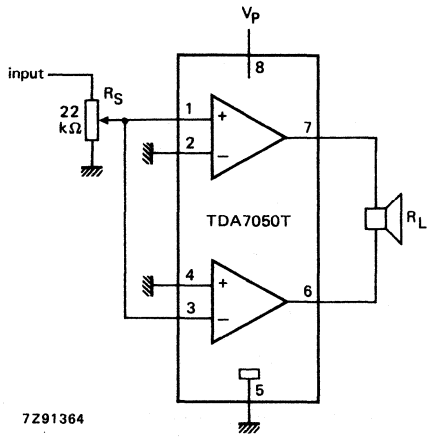


Fig. 4 Application diagram (BTL); also used as test circuit.

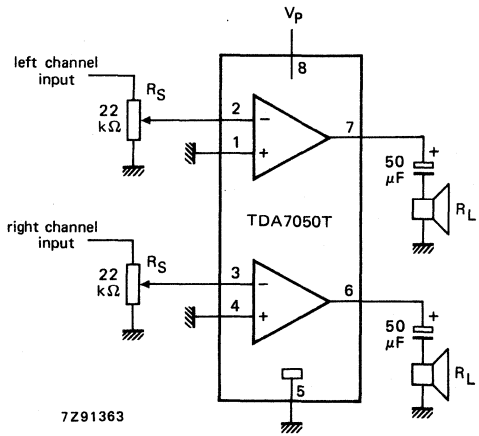


Fig. 5 Application diagram (stereo); also used as test circuit.

1 W BTL MONO AUDIO AMPLIFIER

GENERAL DESCRIPTION

The TDA7052 is a mono output amplifier in a 8-lead dual-in-line (DIL) plastic package. The device is designed for battery-fed portable audio applications.

Features:

- No external components
- No switch-on or switch-off clicks
- Good overall stability
- Low power consumption
- No external heatsink required
- Short-circuit proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	38	39	40	dB
Output power	THD = 10%; 8 Ω	P_O	–	1,2	–	W
Total harmonic distortion	P_O = 0,1 W	THD	–	0,2	1,0	%

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

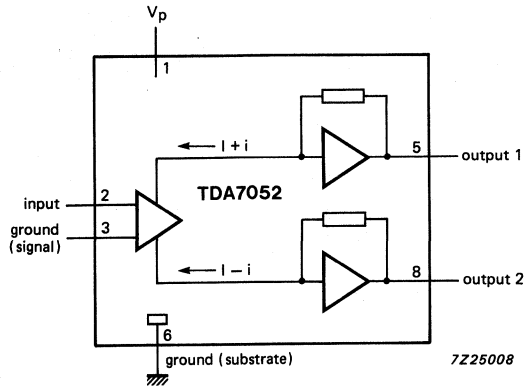


Fig. 1 Block diagram.

PINNING

1	V_P	supply voltage	5	OUT1	output 1
2	IN	input	6	GND2	ground (substrate)
3	GND1	ground (signal)	7	n.c.	not connected
4	n.c.	not connected	8	OUT2	output 2

FUNCTIONAL DESCRIPTION

The TDA7052 is a mono output amplifier designed for battery-fed portable audio applications, such as tape recorders and radios.
The gain is fixed internally at 40 dB. A large number of tape recorders and radios are still designed for mono sound, plus a space-saving trend by reduction of the number of battery cells. This means a decrease in supply voltage which results in an reduction of output power. To compensate for this reduction, the TDA7052 uses the Bridge-Tied-Load principle (BTL) which can deliver an output power of 1,2 W (THD = 10%) into an 8 Ω load with a power supply of 6 V. The load can be short-circuited at each signal excursion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	18	V
Non-repetitive peak output current	I_{OSM}	–	1,5	A
Total power dissipation	P_{tot}	see Fig. 2		
Crystal temperature	T_c	–	150	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

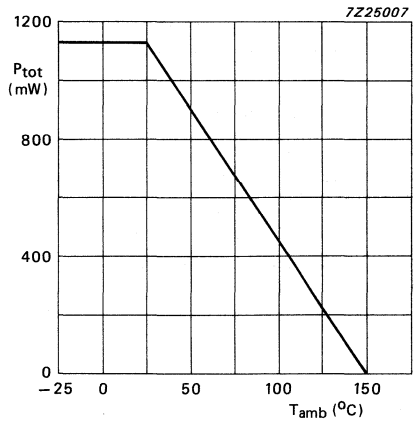


Fig. 2 Power derating curve.

POWER DISSIPATION

Assume V_P = 6 V; R_L = 8 Ω; T_{amb} = 50 °C maximum.
The maximum sinewave dissipation is 0,9 W.

$$R_{th\,j\text{-}a} = \frac{150 - 50}{0{,}9} \approx 110 \text{ K/W}.$$

Where $R_{th\,j\text{-}a}$ of the package is 110 K/W, so no external heatsink is required.

CHARACTERISTICS

V_P = 6 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	38	39	40	dB
Output power	THD = 10%	P_o	–	1,2	–	W
Noise output voltage (RMS value)						
	note 1	$V_{no(rms)}$	–	150	300	μV
	note 2	$V_{no(rms)}$	–	60	–	μV
Frequency response		f_r	–	20 Hz to 20 kHz	–	Hz
Supply voltage ripple rejection	note 3	SVRR	40	50	–	dB
DC output offset voltage pin 5 to 8	R_S = 5 kΩ	ΔV_{5-8}	–	–	100	mV
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%
Input impedance		$\|Z_I\|$	–	100	–	kΩ
Input bias current		I_{bias}	–	100	300	nA

Notes to the characteristics

1. The unweighted RMS noise output voltage is measured at a bandwidth of 60 Hz to 15 kHz with a source impedance (R_S) of 5 kΩ.
2. The RMS noise output voltage is measured at a bandwidth of 5 kHz with a source impedance of 0 Ω and a frequency of 500 kHz. With a practical load (R = 8 Ω; L = 200 μH) the noise output current is only 100 nA.
3. Ripple rejection is measured at the output with a source impedance of 0 Ω and a frequency between 100 Hz and 10 kHz. The ripple voltage = 200 mV (RMS value) is applied to the positive supply rail.

* Value to be fixed.

APPLICATION INFORMATION

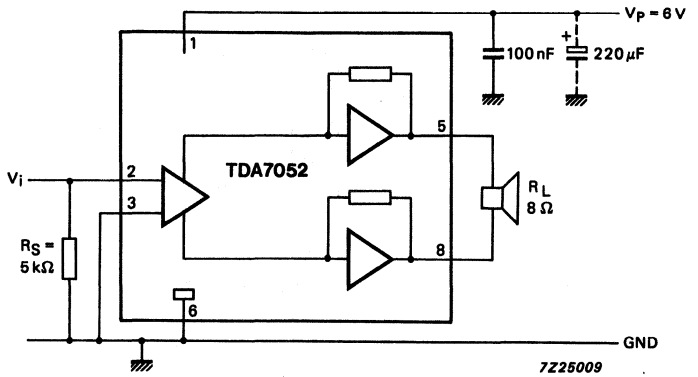


Fig. 3 Application diagram.

2 × 1 W PORTABLE/MAINS-FED STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7053 is an integrated class-B stereo power amplifier in a 16-lead dual-in-line (DIL) plastic package. The device, consisting of two BTL amplifiers, is primarily developed for portable audio applications but may also be used in mains-fed applications.

Features

- No external components
- No switch-ON/OFF clicks
- Good overall stability
- Low power consumption
- Short-circuit-proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	9	16	mA
Output power	$R_L = 8\ \Omega$; $V_P = 6$ V	P_O	–	1.2	–	W
Internal voltage gain		G_V	38	39	40	dB
Total harmonic distortion	$P_O = 0.1$ W	THD	–	0.2	1.0	%

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

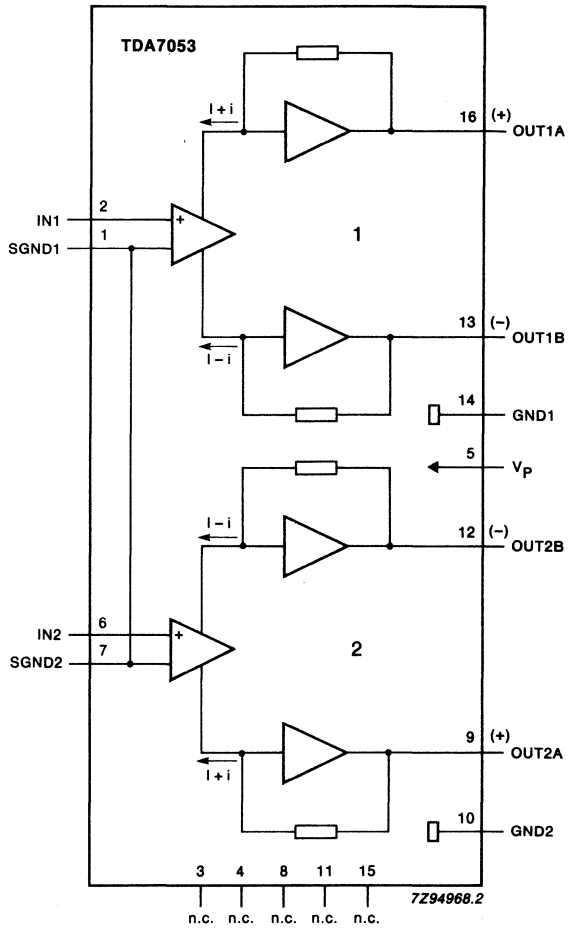


Fig. 1 Block diagram.

PINNING

1.	SGND1	signal ground 1	9.	OUT2A	output 2 (positive)
2.	IN1	input 1	10.	GND2	power ground 2
3.	n.c.	not connected	11.	n.c.	not connected
4.	n.c.	not connected	12.	OUT2B	output 2 (negative)
5.	V_P	supply voltage	13.	OUT1B	output 1 (negative)
6.	IN2	input 2	14.	GND1	power ground 1
7.	SGND2	signal ground 2	15.	n.c.	not connected
8.	n.c.	not connected	16.	OUT1A	output 1 (positive)

Note

The information contained within the parentheses refer to the polarity of the loudspeaker terminal to which the output must be connected.

FUNCTIONAL DESCRIPTION

The TDA7053 is a stereo output amplifier, with an internal gain of 39 dB, which is primarily for use in portable audio applications but may also be used in mains-fed applications. The current trends in portable audio application design is to reduce the number of batteries which results in a reduction of output power when using conventional output stages. The TDA7053 overcomes this problem by using the Bridge-Tied-Load (BTL) principle and is capable of delivering 1.2 W into an 8 Ω load (V_P = 6 V). The load can be short-circuited under all input conditions.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_P	–	18	V
Non-repetitive peak output current		I_{OSM}	–	1.5	A
Total power dissipation		P_{tot}	see Fig. 2		
Crystal temperature		T_c	–	+150	°C
Storage temperature range		T_{stg}	–65	+150	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	50	K/W

Power dissipation

Assuming: $V_P = 6$ V and $R_L = 8\ \Omega$:

The maximum sinewave dissipation is 1.8 W, therefore $T_{amb(max.)} = 150 - (50 \times 1.8) = 60$ °C.

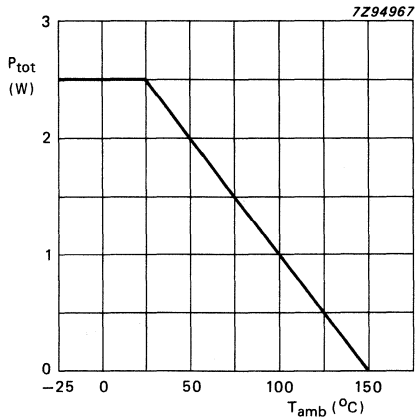


Fig. 2 Power derating curve.

CHARACTERISTICS

V_P = 6 V; R_L = 8 Ω; T_{amb} = 25 °C; unless otherwise specified; measured from test circuit, Fig. 7.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$; note 1	I_{tot}	–	9	16	mA
Input bias current		I_{bias}	–	100	300	nA
Supply voltage ripple rejection	note 2	SVRR	40	50	–	dB
Input impedance		Z_I	–	100	–	kΩ
DC output offset voltage	note 3	ΔV_{13-16}	–	–	100	mV
		ΔV_{12-9}	–	–	100	mV
Noise output voltage (RMS value)	note 4	$V_{no(rms)}$	–	150	300	μV
	note 5	$V_{no(rms)}$	–	60	–	μV
Output power	THD = 10%	P_O	–	1.2	–	W
Total harmonic distortion	P_O = 0.1 W	THD	–	0.2	1.0	%
Internal voltage gain		G_V	38	39	40	dB
Channel balance		ΔG_V	–	–	1	dB
Channel separation	note 3	α	40	–	–	dB
Frequency response		f	–	0.02 to 20	–	kHz

Notes to the characteristics

1. With a practical load the total quiescent current depends on the offset voltage.
2. Ripple rejection measured at the output with R_S = 0 Ω and f = 100 Hz to 10 kHz. The ripple voltage (200 mV) is applied to the positive supply rail.
3. R_S = 5 kΩ.
4. The noise output voltage (RMS value) is measured with R_S = 5 kΩ, unweighted and a bandwidth of 60 Hz to 15 kHz.
5. The noise output voltage (RMS value) is measured with R_S = 0 Ω and f = 500 kHz with 5 kHz bandwidth. If R_L = 8 Ω and L_L = 200 μH the noise output current is only 100 nA.

APPLICATION INFORMATION

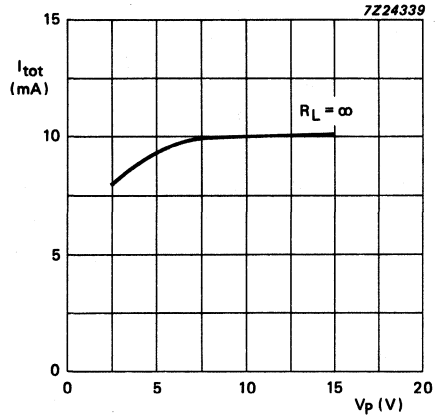


Fig. 3 Quiescent current as a function of voltage supply (V_P); T_{amb} = 60 °C.

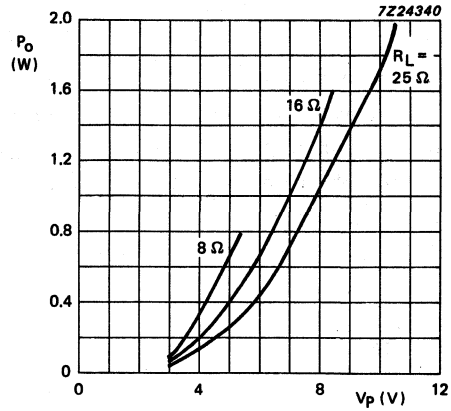
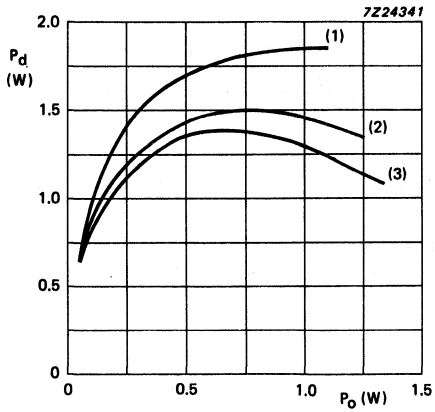
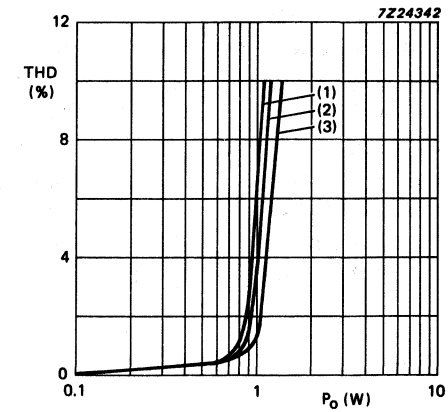


Fig. 4 Output power as a function of voltage supply (V_P); THD = 10%; f = 1 kHz; T_{amb} = 60 °C.



(1) V_P = 6.0 V; R_L = 8 Ω
(2) V_P = 7.5 V; R_L = 16 Ω
(3) V_P = 9.0 V; R_L = 25 Ω

Fig. 5 Power dissipation as a function of output power; f = 1 kHz; T_{amb} = 60 °C.



(1) V_P = 6.0 V; R_L = 8 Ω
(2) V_P = 7.5 V; R_L = 16 Ω
(3) V_P = 9.0 V; R_L = 25 Ω

Fig. 6 Total harmonic distortion as a function of output power; f = 1 kHz; T_{amb} = 60 °C.

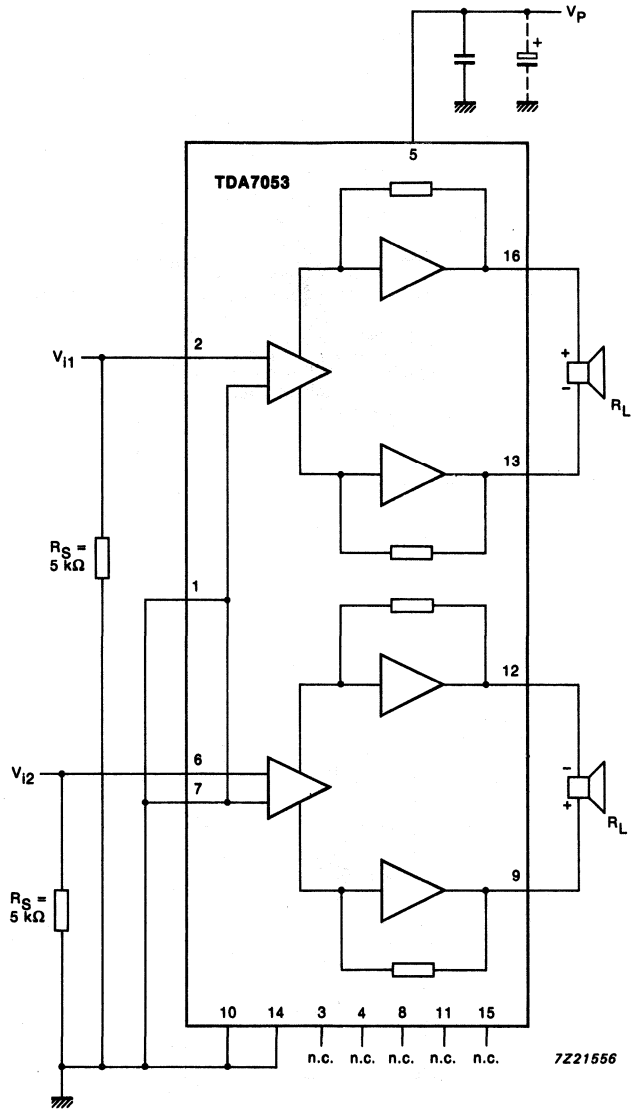


Fig. 7 Test and application circuit diagram.

APPLICATION INFORMATION (continued)

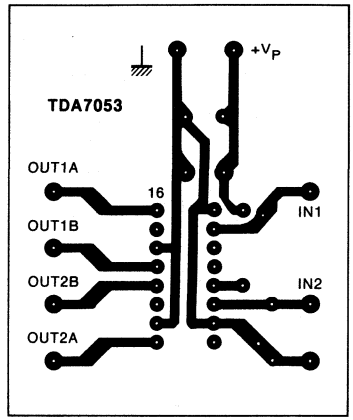


Fig. 8 Printed-circuit board, track side.

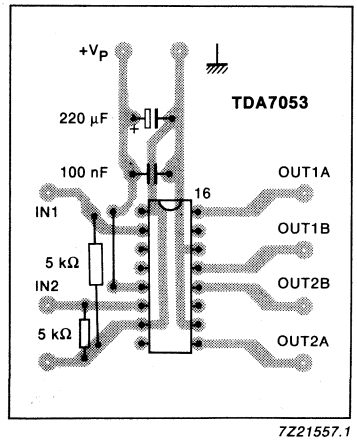


Fig. 9 Printed-circuit board, component side.

LOW POWER FREQUENCY SYNTHESIZER (LOPSY)

GENERAL DESCRIPTION

The TDD1742T is a low power, high-performance frequency synthesizer in local oxidation CMOS (LOCMOS) technology. The device is designed for use in channelized VHF/UHF applications especially portable and mobile radios.

The circuit incorporates many of the features of the HEF4750V (frequency synthesizer) and HEF4751 (universal divider), including a high-gain phase comparator together with an on-chip sample-and-hold capacitor and phase modulator.

A multiplexed or bus-structured programming sequence allows interface to a microcontroller or external memory (ROM/PROM); power is applied to the memory only when it is required for programming via additional on-chip circuitry.

Operation is possible with a minimum supply voltage of 7 V and a maximum input frequency of 8,5 MHz.

Encapsulation in a 28-lead mini-pack enables the construction of small, low power consumption synthesizers with low noise performance and high side-band attenuation.

Features

- On-chip sample-and-hold capacitor
- Low power consumption
- High-gain phase comparator with low levels of noise and spurious outputs
- Auxiliary digital phase comparator for fast locking
- On-chip phase modulator
- Simple interfacing to external memory
- Microcontroller compatible
- Power-on reset circuitry

QUICK REFERENCE DATA

Supply voltage ranges			
pin 14	$V_{DD1} = V_{14-6}$	7 to 10	V
pin 8	$V_{DD2} = V_{8-6}$	4,5 to 5	V
pin 1	$V_{DD3} = V_{1-6}$	7 to 10	V
Supply current (at T_{amb} = 25 °C; $V_{DD1} = V_{DD3}$ = 7,4 V; V_{DD2} = 5 V)			
pin 14 (phase modulator OFF)	$I_{DD1} = I_{14}$	max. 1,5	mA
pin 8	$I_{DD2} = I_8$	max. 100	μA

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

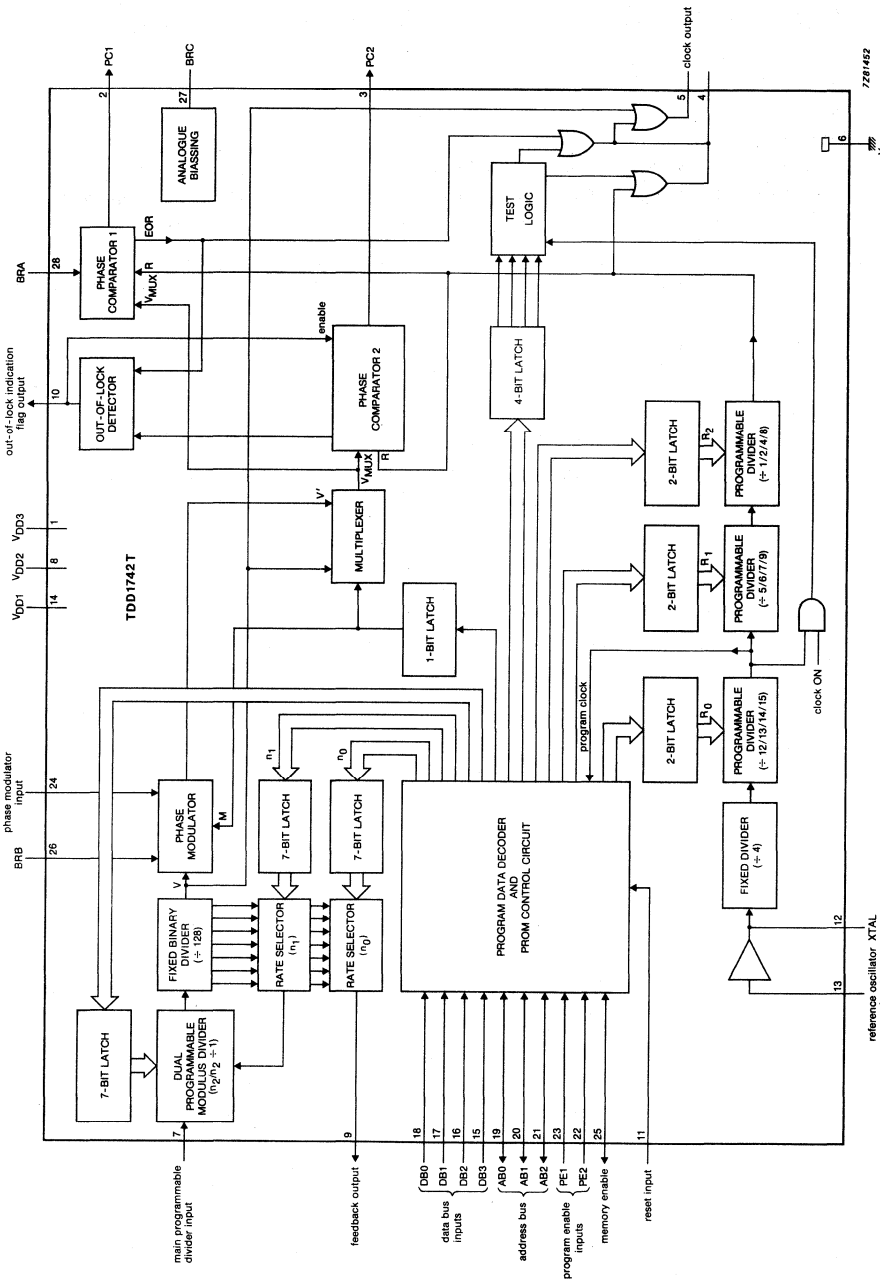


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

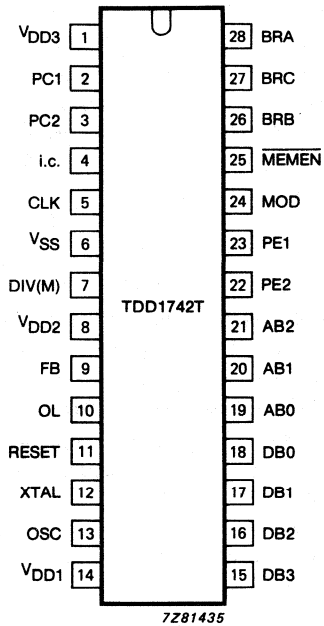


Fig. 2 Pinning diagram.

Pin functions

pin no.	mnemonic	description
1	V_{DD3}	**Power Supply 3:** analogue supply voltage (7 to 10 V).
2	PC1	**Phase Comparator 1:** high-gain analogue phase comparator output which is used when the system is in-lock to give low levels of noise and spurious outputs.
3	PC2	**Phase Comparator 2:** low-gain digital phase comparator 3-state output which enables the achievement of fast lock times when the system is initially out-of-lock. Phase comparator 2 is inhibited when the phase is within the locking range of phase comparator 1.
4	i.c.	**internally connected** (must be left floating).
5	CLK	**Clock:** clock output.
6	V_{SS}	**Ground:** circuit earth potential.
7	DIV(M)	**Divider:** input to the main programmable divider (8,5 MHz max.), usually from prescaler.
8	V_{DD2}	**Power Supply 2:** supply voltage for TTL-compatible stages (+ 5 V ± 10%).
9	FB	**Feedback:** feedback output to control the modulus of the external prescaler.
10	OL	**Out-of-lock:** out-of-lock indication flag output. This output is HIGH when phase comparator 2 is in operation (when the system is out-of-lock).
11	RESET	**Power-on-Reset:** Following power up an initial pulse is applied to this input pin to set the internal counters.

Pin functions (continued)

pin no.	mnemonic	description
12	XTAL	**Crystal:** output to external crystal to form the oscillator circuit in combination with the OSC input. Alternatively this pin may be used as a buffer output.
13	OSC	**Oscillator:** input to reference oscillator which together with the XTAL output and an external crystal is used to generate the reference frequency. Alternatively to OSC input may be used as a buffer amplifier for an external reference oscillator.
14	V_{DD1}	**Power Supply 1:** digital supply voltage (7 to 10 V).
15-18	DB3-DB0	**Data Bus:** Data Bus inputs (TTL compatible).
19-21	AB0-AB2	**Address Bus:** TTL compatible bidirectional address bus. Provides address output to an external memory or input from microcontroller. The outputs are 3-state with internal pull-downs.
22	PE2	**Program Enable 2:** TTL compatible inputs to initiate the programming cycle or strobe the internal data latches.
23	PE1	**Program Enable 1:**
24	MOD	**Modulator:** high impedance linear phase modulator input, which applies a voltage controlled delay to the programmable divider output to the phase comparator.
25	$\overline{\text{MEMEN}}$	**Memory Enable:** mode control and memory enable bidirectional pin. If pin 25 is LOW at general reset the TDD1742T is set to the microcontroller mode; if pin 25 is HIGH at general reset the TDD1742T is set to the memory mode and the ROM/PROM is enabled.
26	BRB	**Bias Resistor B:** current mirror which acts as gain control for the phase modulator.
27	BRC	**Bias Resistor C:** current mirror pin which provides analogue biassing.
28	BRA	**Bias Resistor A:** current mirror pin which acts as gain control for phase comparator 1.

FUNCTIONAL DESCRIPTION

Reference oscillator chain

The reference oscillator chain comprises a crystal oscillator and dividers to give the required frequency to drive the phase comparators.
The oscillator stage is a single inverter connected between pin 12 (XTAL) and pin 13 (OSC). Satisfactory operation is achieved with crystals up to 9 MHz. Alternatively, the OSC input may be used as a buffer amplifier for an external reference oscillator.
The reference divider chain comprises a fixed divide by 4-stage followed by three cascaded programmable dividers of ratios ÷ 12/13/14/15, ÷ 5/6/7/9 and ÷ 1/2/4/8. The output of the last stage is applied as one input (R) to the two phase comparators. Thus a number of division ratios between 240 and 4320 are possible which provides all the required VHF and UHF channel spacings with reference crystals in a 1 to 9 MHz range.

Main programmable divider

The main programmable divider is a rate feedback binary divider. As shown in figure 1 it comprises a fixed 7-bit binary divider (÷ 128) and two rate selectors (n_1 and n_0). One rate selector controls a 7-bit fully programmable dual modulus divider (÷ $n_2/n_2 + 1$) and the other controls the external dual modulus prescaler (÷ A/A + 1).

The overall division rate (N) is given by:

$$N = (128\, n_2 + n_1)\, A + n_0$$

Where:

$$0 \leqslant n_0 \leqslant 127$$
$$0 \leqslant n_1 \leqslant 127$$
$$1 \leqslant n_2 \leqslant 127.$$

The output from the programmable divider is fed to the phase comparators via the phase modulator and the multiplexer. The phase modulator is bypassed if not selected.

Phase comparison

The TDD1742T contains 2 phase comparators which act in close co-operation. Phase comparator 1 is the main comparator. It is designed to have a high-gain analogue output, 4500 volts/cycle at 10 kHz (typ.). This enables a low noise performance to be achieved. However, the output of phase comparator 1 will saturate at high or low levels for very small phase excursions.
Phase comparator 2 is an auxiliary comparator with a wide range, which enables faster lock times to be achieved than otherwise would be possible. This digital phase comparator has a linear $\pm 2\pi$ radians phase range, which corresponds to a gain of $\frac{V_{DD}}{2}$ volts/cycle.

To avoid degrading the noise performance of the system by the relatively low gain of phase comparator 2, once a small phase error has been achieved an internal switch disconnects phase comparator 2, leaving only phase comparator 1 connected. Thus the low noise properties of phase comparator 1 are obtained once phase-lock has been achieved.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Phase comparator 1 (see Fig. 3)

Phase comparator 1 is comprised of a linear ramp generator and a sample and hold circuit.

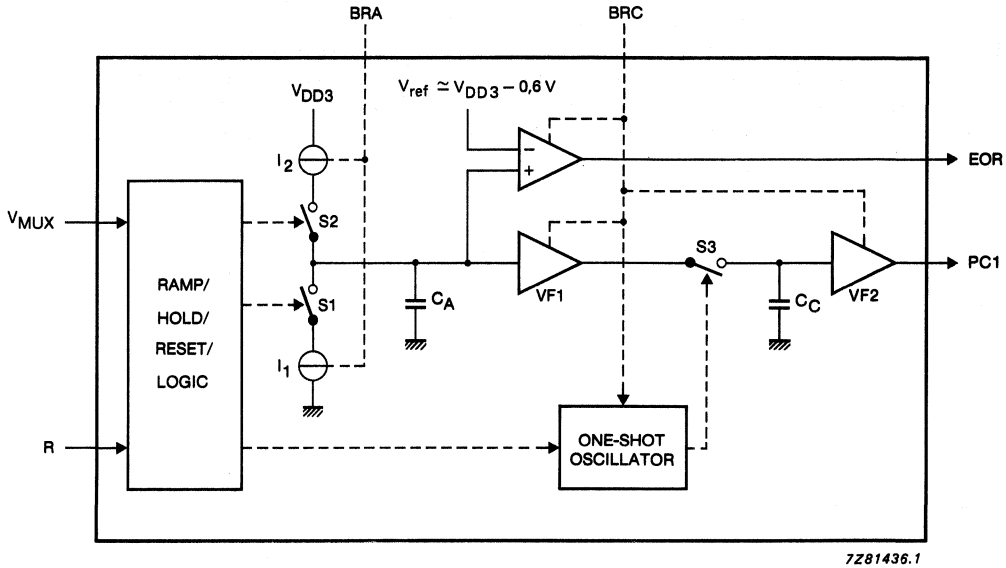


Fig. 3 Simplified block diagram of phase comparator 1.

A negative-going transition at the V_{MUX} input causes the hold capacitor C_A to be discharged via switch S1 and constant current source I_1.
A positive-going transition at the V_{MUX} input causes the hold capacitor C_A to be charged via switch S2 and constant current source I_2, which produces a linear ramp.
A negative-going transition at the R input terminates the linear ramp.
Capacitor C_A holds the voltage that the ramp has attained, and is buffered by the voltage follower VF1. After the output of VF1 is stable (2 μs), the sample switch S3 is closed for approximately 1 μs by the one-shot oscillator. This enables the capacitor C_C to charge to the voltage level of VF1 and in turn buffered by voltage follower VF2 made available at output PC1.
The construction and small duty cycle of the sample switch S3 provides a low hold step, resulting in a minimum side-band level.
If the linear ramp terminates before a negative-going transition at the R input is present, an end of ramp (EOR) signal is produced, generating in turn an out-of-lock (OL) signal. OL enables phase comparator 2 via the out-of-lock detector.

These actions are illustrated in the waveforms of Fig. 4 and Fig. 5.

The gain of phase comparator 1 as measured at PC1 is given by:

$$\text{PC gain} \simeq \frac{446\, I_{BRA}}{F_R}$$

Where:

I_{BRA} is in μA
F_R is the phase comparator reference frequency in kHz

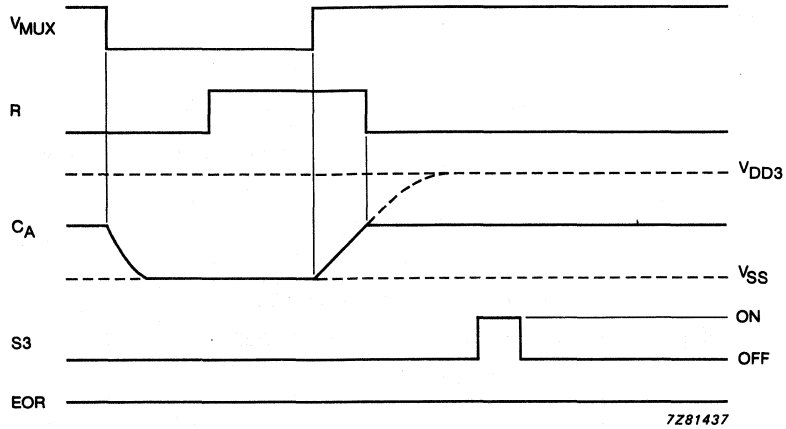


Fig. 4 Waveforms of phase comparator 1; in-lock condition.

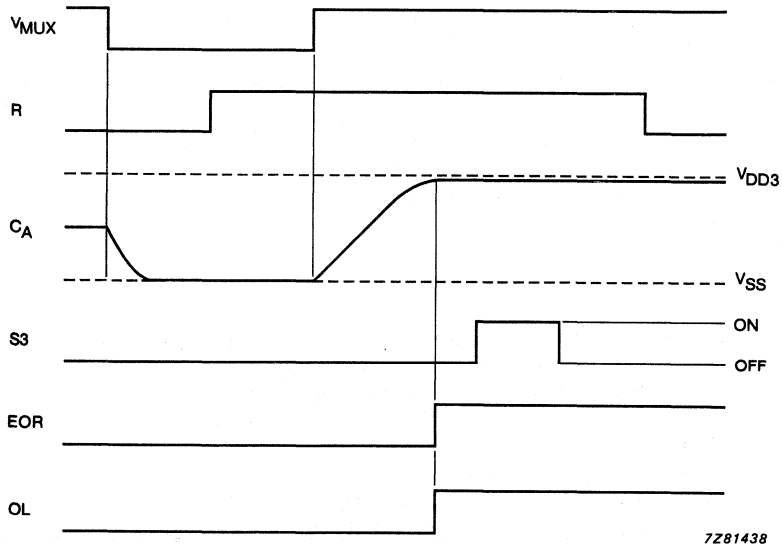


Fig. 5 Waveforms of phase comparator 1; out-of-lock condition.

When V_{MUX} leads R the output signal at pin 2 (PC1) is proportional to the phase difference (in-lock condition) or HIGH (out-of-lock condition).
When R leads V_{MUX} the output signal at pin 2 (PC1) remains LOW.

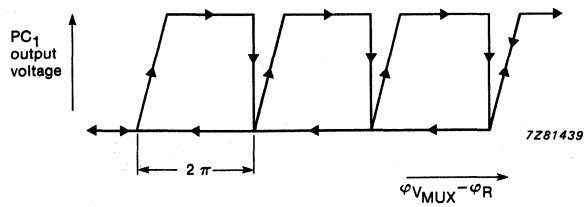


Fig. 6 Phase characteristic of output PC1.

FUNCTIONAL DESCRIPTION (continued)

Phase comparator 2 (see Fig. 7)

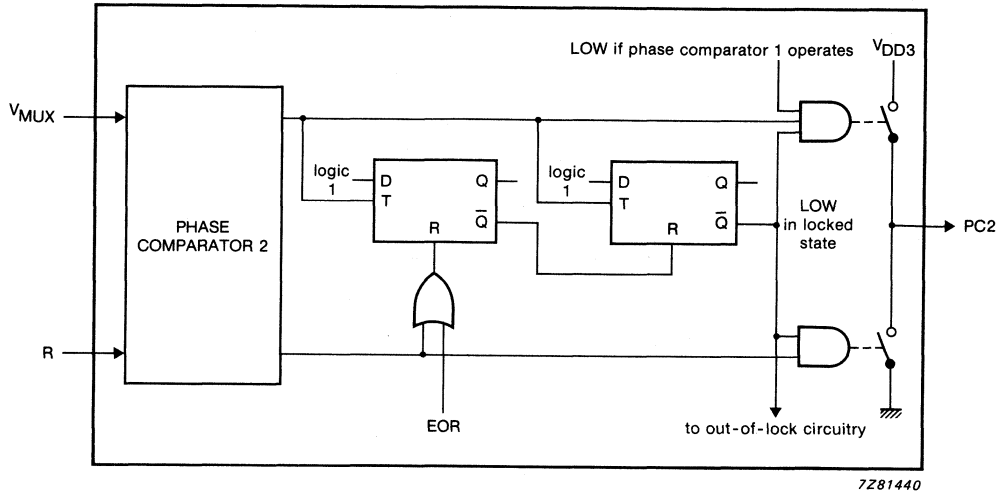


Fig. 7 Simplified block diagram of phase comparator 2.

The digital phase comparator (PC2) has three stable states:

- Reset
- V_{MUX} leads R
- R leads V_{MUX}

Table 1 Phase comparator 2: stable states and corresponding output levels

state	V_{MUX} leads R	R leads V_{MUX}
reset	0	0
V_{MUX} leads R	1	0
R leads V_{MUX}	0	1

Transition from one state to another takes place on command of either an active V_{MUX}-edge or an active R-edge as shown in Fig. 8.

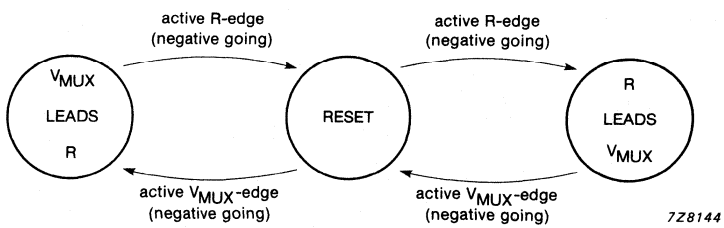


Fig. 8 Transition of state; phase comparator 2.

The output of phase comparator 2 produces positive or negative going pulses with variable width, dependent on the phase relationship of R and V_{MUX}.
The average output voltage is a linear function of the phase difference. Output at pin 3 (PC2) remains in the high impedance OFF-state in the region in which phase comparator 1 operates

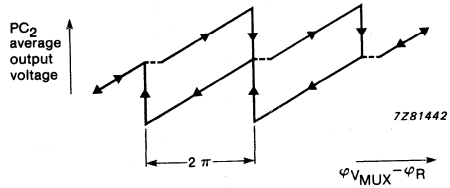


Fig. 9 Phase characteristic of output PC2.

To reach the reset state of phase comparator 2 it is necessary to apply:

- $2V_{MUX}$ + R*
  or
- 2R + V_{MUX}

Thus to achieve the R leads V_{MUX} state 2R must be applied; to achieve the V_{MUX1} leads R state $2V_{MUX}$ must be applied.

DEVELOPMENT DATA

Out-of-lock function

There are several situations when the system goes from the locked to the out-of-lock state (OL output goes HIGH):

- V_{MUX} leads R, however out of the range of phase comparator 1
- R leads V_{MUX}
- R-pulse is missing
- V_{MUX}-pulse is missing

In the first three situations the locked state can be reset by applying two successive cycles within the range of phase comparator 1.
In the fourth situation the locked state can be reset by applying a V_{MUX} pulse followed by two successive cycles within the range of phase comparator 1.

Phase modulator (see Fig. 10)

The linear phase modulator applies a voltage controlled delay to the signal from the programmable divider to the phase comparator input. The gain of the phase modulator is adjustable via an external bias resistor (BRB) which is connected between pin 26 and ground.
The time delay introduced into the V path to the phase modulator is:

$$\frac{909}{I_{BRB}} \text{ ns/volt of input applied to pin 24 (MOD)}$$

When a positive-going transition appears at the V-input, the D type flip-flop produces a HIGH V' level and causes capacitor C_B to produce a positive-going ramp via switch S1 and constant current source I_1 starting at the V_{SS} potential. When the ramp has reached a value equal to the modulation input voltage (at MOD), the comparator resets the D type flip-flop, which terminates the V pulse. C_B now discharges to V_{SS} via switch S1 and constant current source I_2 and the circuit returns to the start position. Because the trailing edge of the V' pulse is the active edge for the phase comparators, a linear phase modulation is achieved. The associated waveforms are shown in Fig. 11. The phase modulator can be switched OFF, via the programming logic, to avoid superfluous dissipation. To achieve, this the M signal must be programmed to logic 0. The V pulse will then be connected via switch S2 to V_{MUX}.

* This means apply two successive active V_{MUX} edges followed by one active R edge.

FUNCTIONAL DESCRIPTION (continued)

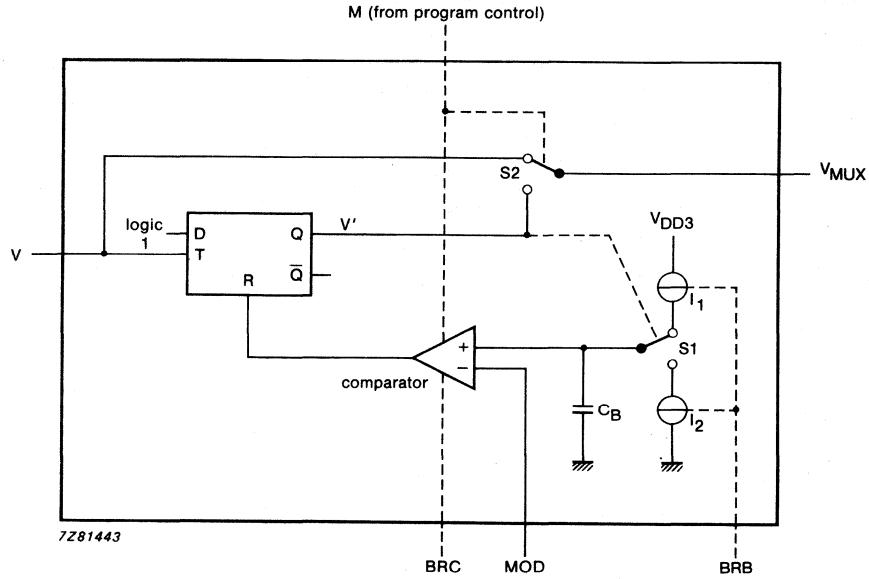


Fig. 10 Simplified block diagram of the phase modulator.

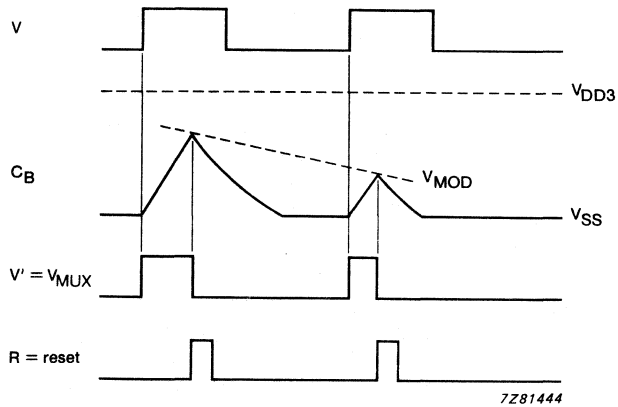


Fig. 11 Phase modulator waveforms; M = 1.

Program control

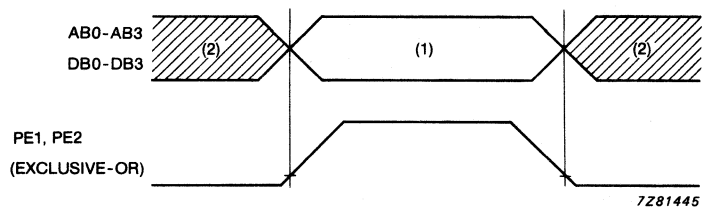
A multiplexed or bus structured sequence allows the TDD1742T to be interfaced to a microcontroller or a PROM.
The device is fully programmable in terms of:

- 6 bits to define the reference divider ratio
- 21 bits to define the main divider ratio
- 1 bit to switch the modulator
- 4 bits to determine the test status

Thus the TDD1742T is programmed with a total of 32 bits which are organized as eight 4-bit words. The address bus is 3 bits wide and the data bus is 4 bits wide. Both buses are TTL compatible. The data words are described in detail in Tables 3 to 7.

Microcontroller mode

If pin 25 ($\overline{\text{MEMEN}}$) is LOW at general reset, the device is set to the micro-controller mode. In this mode a 7-bit word, comprised of 3 address bits (AB0 to AB2) and 4 data bits (DB0 to DB3), may be strobed into the TDD1742T when the program enable pins PE1 and PE2 are set to opposite state (EXCLUSIVE -OR condition; see Fig. 12 and Table 2). One frame of 8 words is necessary to completely program the TDD1742T. Incoming data is not clocked into the internal counter latches until after the receipt of data corresponding to address 111. Upon subsequent reprogramming it is not necessary to change all eight words but a reprogramming sequence must always finish with the data corresponding to address 111.



(1) Address and data valid.
(2) Address and data not valid.

Fig. 12 Waveforms for program enable function; microcontroller mode.

Table 2 Truth table for program enable function; microcontroller mode

PE1	PE2	load
0	0	NO
1	0	YES
0	1	YES
1	1	NO

Program control (continued)

Memory mode (PROM)

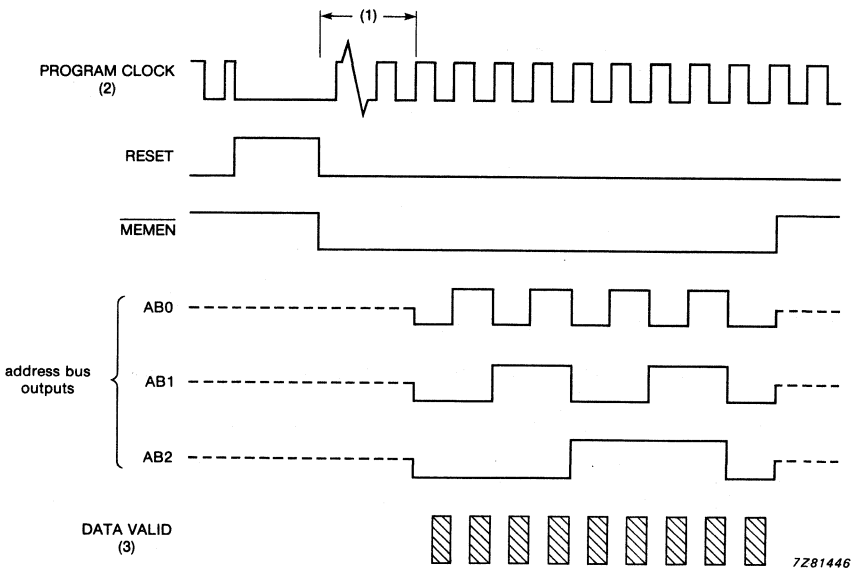
If pin 25 ($\overline{\text{MEMEN}}$) is HIGH at general reset, TDD1742T is set to the memory mode and a programming cycle is initiated. Subsequent reprogramming is performed by applying a pulse to program enable PE1 (pin 23) or PE2 (pin 22). If PE1 is LOW, programming will occur on the LOW-to-HIGH transition of PE2. If PE1 is HIGH, programming will occur on the HIGH-to-LOW transition of PE2. PE1 and PE2 are interchangeable. Reprogramming will also occur by applying a pulse to RESET (pin 11).

At the start of a programming sequence pin 25 goes LOW and may be used to apply power to the memory via an external driver. After a settling time the address bus outputs 000 followed by the remaining seven addresses. During the second half of each address period data, from the memory is latched into the TDD1742T so that the access time of the PROM is not critical.

Note

The program clock is derived from the reference divider chain and its frequency equals $f_{OSC}/4R_0$.

After the full 32 bits have been read the address returns to address 000 before going 3-state. This step transfers data from the internal data latches to the appropriate divider latches. Pin 25 now returns to a high impedance state and power is removed from the memory. Fig. 13 shows the timing for a reset initiated programming sequence; the timing is similar for program enable initiated sequence.



(1) Delay time for PROM settling.
(2) The program clock is derived from the reference divider chain.
(3) Data is valid during the shaded period.

Fig. 13 Timing diagram for TDD1742T PROM control.

Data memory maps

Table 3 Bit programming of the eight 4-bit words

address			data			
AB2	AB1	AB0	DB3	DB2	DB1	DB0
0	0	0	see Table 4			
0	0	1	$n_0 3$	$n_0 2$	$n_0 1$	$n_0 0$
0	1	0	$R_0 0$	$n_0 6$	$n_0 5$	$n_0 4$
0	1	1	$n_1 3$	$n_1 2$	$n_1 1$	$n_1 0$
1	0	0	$R_0 1$	$n_1 6$	$n_1 5$	$n_1 4$
1	0	1	$n_2 3$	$n_2 2$	$n_2 1$	$n_2 0$
1	1	0	M	$n_2 6$	$n_2 5$	$n_2 4$
1	1	1	$R_2 1$	$R_2 0$	$R_1 1$	$R_1 0$

In Table 3

n_0, n_1 and n_2 comprises the main programmable divider.

$n_0 0$ is the LSB of n_0, $n_0 6$ the MSB and so forth.

If M is 1 the modular is ON.

Table 4 Memory map for address 000

DB3	DB2	DB1	DB0	program clock to output CLK	mode
0	0	X	X	yes	idle
0	1	0	0	no	idle
all other combinations				not defined	not defined

Where

X = don't care.

For optimum performance (minimum crosstalk) 0100 should be programmed into address 000.

Memory maps (continued)

Table 5 Reference divider control; part 1

$R_0$1	$R_0$0	division ratio
0	0	12
0	1	13
1	0	14
1	1	15

In Table 5:

$R_0$0 and $R_0$1 control the ÷ 12/13/14/15 portion of the reference divider.

Table 6 Reference divider control; part 2

$R_1$1	$R_1$0	division ratio
0	0	9
0	1	5
1	0	6
1	1	7

In Table 6:

$R_1$0 and $R_1$1 control the ÷ 5/6/7/9 portion of the reference divider.

Table 7 Reference divider control; part 3

$R_2$1	$R_2$0	division ratio
0	0	1
0	1	2
1	0	4
1	1	8

In Table 7:

$R_2$0 and $R_2$1 control the ÷ 1/2/4/8 portion of the reference divider.

Current biassing

Current biassing is provided by 3 external bias resistors A, B and C.

Bias Resistor A: is connected between pin 28 (BRA) and ground. The value of the resistor must be such that I_{BRA} = 20 μA, which acts as gain control for analogue phase comparator 1.
Bias Resistor B: is connected between pin 26 (BRB) and ground. The value of the resistor must be such that I_{BRB} = 3 to 25 μA, which acts as gain control for the phase modulator.
Bias Resistor C: is connected between pin 27 (BRC) and ground. The value of the resistor must be such that I_{BRC} = 5 to 30 μA, which provides biassing for the remainder of the analogue circuitry.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges			
pin 14	V_{DD1}	−0,5 to + 15	V
pin 8	V_{DD2}	−0,5 to + 15	V
pin 1	V_{DD3}	−0,5 to + 15	V
Voltage on any input	V_I	−0,5 to V_{DD1} + 0,5	V
Relative supply voltage	V_{DD2}-V_{DD1}	max. 0,5	V
Relative supply voltage	V_{DD3}-V_{DD1}	max. 0,5	V
D.C. current into any input or output	± I	max. 10	mA
Power dissipation per package for T_{amb} = 0 to + 85 °C	P_{tot}	max. 400	mW
Power dissipation per output for T_{amb} = 0 to + 85 °C	P_O	max. 100	mW
Storage temperature range	T_{stg}	−65 to 150	°C
Operating ambient temperature range	T_{amb}	−40 to 85	°C

DEVELOPMENT DATA

D.C. CHARACTERISTICS

$V_{DD1} = V_{DD3} = 7{,}4$ V; $V_{DD2} = 5$ V; $V_{SS} = 0$ V; $T_{amb} = 25\ ^{o}C$ unless otherwise specified; for definitions see note 1.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage					
pin 14	V_{DD1}	7	–	10	V
pin 8	V_{DD2}	4,5	–	5	V
pin 1	V_{DD3}	7	–	10	V
Supply current					
pin 14 (phase modulator OFF)	I_{DD1}	–	–	1,5	mA
pin 8	I_{DD2}	–	–	100	μA
pin 1 (phase modulator OFF)	I_{DD3}	–	–	1,5	mA
Input leakage current (notes 2 and 3)					
logic inputs, MOD	$\pm I_{LI}$	–	–	300	nA
Output leakage current (notes 2 and 3) at ½ V_{DD}					
PC2 high impedance OFF state	$\pm I_{LO}$	–	–	50	nA
$\overline{\text{MEMEN}}$ high impedance state	$\pm I_{LO}$	–	–	1,6	μA
I/O current					
AB0 to AB2 high impedance state	$I_{I/O}$	5	–	30	μA
Logic input voltage LOW					
CMOS inputs; CMOS I/Os	V_{IL}	–	–	$0{,}3V_{DD1}$	V
TTL inputs; TTL I/Os	V_{IL}	–	–	0,8	V
Logic input voltage HIGH					
CMOS inputs; CMOS I/Os	V_{IH}	$0{,}7V_{DD1}$	–	–	V
TTL inputs; TTL I/Os	V_{IH}	2	–	–	V
Logic output voltage LOW (note 2)					
at $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	50	mV
Logic output voltage HIGH (note 2)					
at $\lvert I_O \rvert < 1$ μA	V_{OH}	V_{DD1}-50	–	–	mV

parameter	symbol	min.	typ.	max.	unit
Logic output voltage LOW (note 2)					
$\overline{\text{MEMEN}}$ at I_{OL} = 4 mA	V_{OL}	–	–	1	V
PC2 at I_{OL} = 1,5 mA	V_{OL}	–	–	0,5	V
CLK; OL at I_{OL} = 1 mA	V_{OL}	–	–	0,5	V
XTAL at I_{OL} = 3 mA	V_{OL}	–	–	0,5	V
FB at I_{OL} = 1 mA	V_{OL}	–	–	0,5	V
AB0; AB1; AB2 at I_{OL} = 0,2 mA	V_{OL}	–	–	0,4	V
Logic output voltage HIGH (notes 2 and 3)					
PC2 at $-I_{OH}$ = 1,5 mA	V_{OH}	$V_{DD1}-0,5$	–	–	V
CLK; OL at $-I_{OH}$ = 1 mA	V_{OH}	$V_{DD1}-0,5$	–	–	V
XTAL at $-I_{OH}$ = 3 mA	V_{OH}	$V_{DD1}-1$	–	–	V
FB at $-I_{OH}$ = 1 mA	V_{OH}	$V_{DD2}-1$	–	–	V
AB0; AB1 at I_{OH} = 0,2 mA	V_{OH}	2,4	–	–	V
AB2 at I_{OH} = 0,8 mA	V_{OH}	2,4	–	–	V
Output PC1					
sink current (notes 2, 3 and Fig. 15)	I_O	1	–	–	mA
source current (notes 2, 3 and Fig. 16)	$-I_O$	1	–	–	mA
Internal resistance of phase comparator 1 (notes 2 and 3) locked state |output swing| $<$ 200 mV specified output range: $0,5\ V_{DD}-0,5$ V to $0,5\ V_{DD}+0,5$ V	R_i	–	2,0	–	Ω

DEVELOPMENT DATA

A.C. CHARACTERISTICS

A dynamic specification is given for the circuit, built-up with external components as shown in Fig. 14, under the following conditions; for definitions see note 1; $V_{DD} = 7{,}4 \pm 0{,}4$ V; $T_{amb} = 25\ ^{o}C$; input transition times $\leqslant 40$ ns; $C_A = C_B = C_C = 10$ nF; R_A chosen so that $I_{RA} = 20\ \mu A \pm 1\ \mu A$; R_B chosen so that $I_{RB} = 3$ to 25 μA; R_C chosen so that $I_{RC} = 5$ to 30 μA; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Main programmable divider (DIV(M); pin 7)					
input frequency all divider ratios (square wave input)	$f_{DIV(M)}$	8,5	–	–	MHz
Reference divider					
input frequency all divider ratios (square wave input)	$f_{DIV(R)}$	9	–	–	MHz
Oscillator frequency (OSC; pin 13)	f_{OSC}	9	12	–	MHz
Input capacitance					
DIV(M); OSC	C_I	–	–	3	pF
DB0 to DB3; PE1; PE2; AB0 to AB2	C_I	–	–	5	pF
Propagation delay (see Fig. 17)					
Feedback output to external prescaler DIV(M) → FB at $C_L = 10$ pF					
HIGH to LOW*	t_{PHL}	–	35	70	ns
LOW to HIGH*	t_{PLH}	–	35	70	ns
Average power supply current (notes 3 and 4)					
in-lock state	I_{DD1}	–	2	–	mA
	I_{DD2}	–	0,15	–	mA
	I_{DD3}	–	0,45	–	mA

* Measured from 30% point of negative-going edge at DIV(M) to 50% point of either output edge of FB.

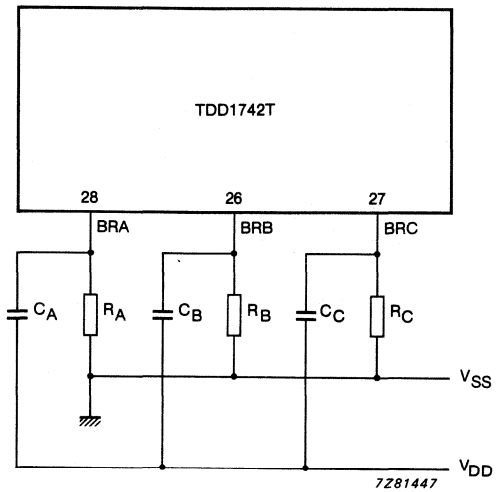


Fig. 14 Test circuit for measuring a.c. characteristics.

DEVELOPMENT DATA

Notes to the characteristics

1. Definitions:
   R_A = external biassing resistor between pins BRA and V_{SS}.
   R_B = external biassing resistor between pins BRB and V_{SS}.
   R_C = external biassing resistor between pins BRC and V_{SS}.
   C_A = decoupling capacitor between pins BRA and V_{DD}.
   C_B = decoupling capacitor between pins BRB and V_{DD}.
   C_C = decoupling capacitor between pins BRC and V_{DD}.
   CMOS logic inputs: RESET, OSC.
   CMOS logic outputs: PC2, CLK, OL, XTAL.
   CMOS logic I/O: $\overline{\text{MEMEN}}$.
   TTL logic inputs: DB0 to DB3, PE2, PE1.
   TTL logic output: FB.
   TTL logic I/O: AB0 to AB2.
   Analogue inputs: DIV(M), MOD.
   Analogue output: PC1.
   Analogue biassing pins: BRA, BRB, BRC.
2. All logic inputs at V_{SS} or V_{DD}.
3. R_A connected; its value chosen such that $I_{BRA} = 20\ \mu A$.
   R_B connected; its value chosen such that $I_{BRB} = 20\ \mu A$.
   R_C connected; its value chosen such that $I_{BRC} = 20\ \mu A$.
4. Average power supply current measured at:
   f_{OSC} = 5 MHz, external clock, divider ratio 420;
   $f_{DIV(M)}$ = 2 MHz, divider ratio 168.

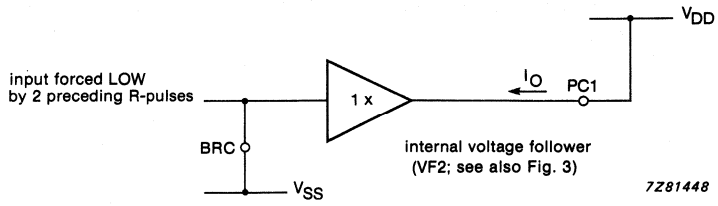


Fig. 15 Equivalent circuit for output PC1 sink current.

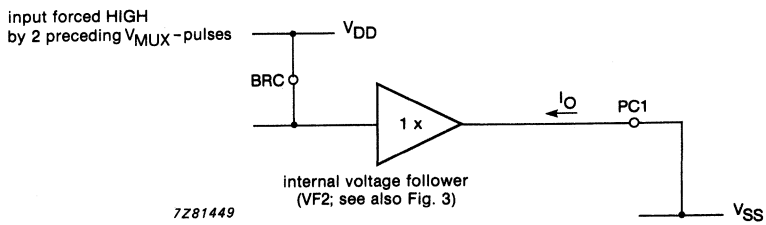


Fig. 16 Equivalent circuit for output PC1 source current.

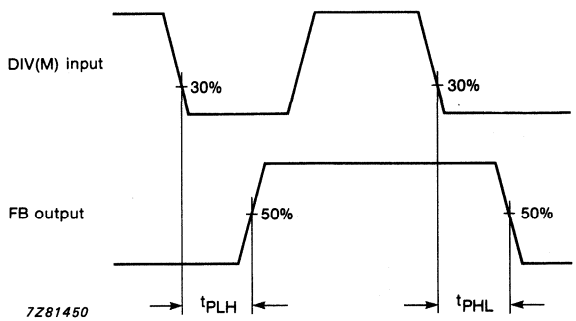


Fig. 17 Waveforms showing propagation delay; DIV (M) → FB.

APPLICATION INFORMATION

Fig. 18 shows a typical application circuit using the TDD1742T in the memory mode with the following design parameters:

Frequency range	150 to 155 MHz
VCO sensitivity	1 MHz/V
Reference frequency	12,5 kHz
Prescaler	÷ 80/81
Reference crystal frequency	5,25 MHz
Reference divider chain	÷ 15; ÷ 7; ÷ 1
Total division ratio	12000 to 12400
Loop bandwidth	300 Hz

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

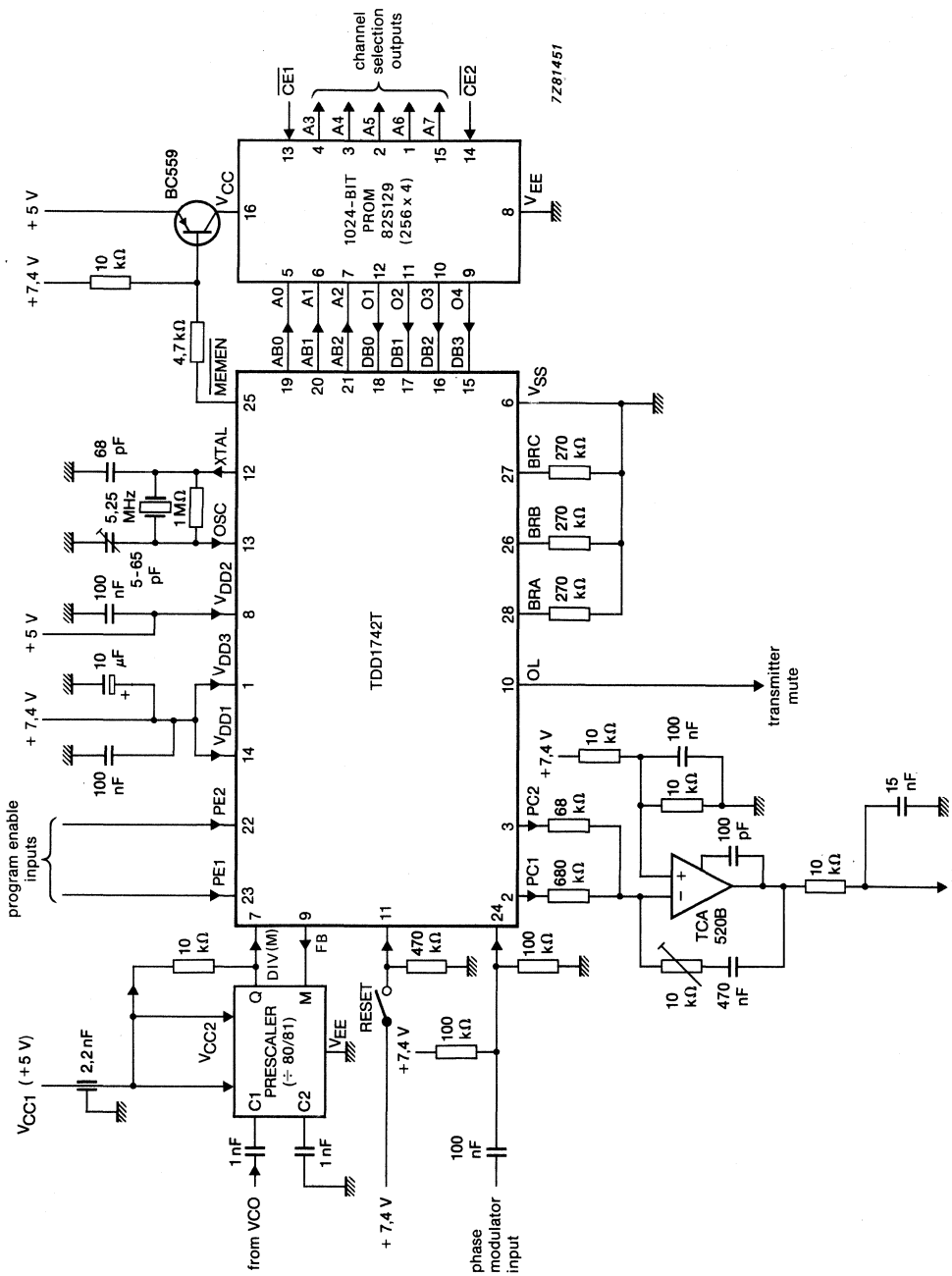


Fig. 18 Typical application circuit using the TDD1742T in memory mode.

VERSATILE TELEPHONE TRANSMISSION CIRCUITS WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1060 and TEA1061 are bipolar integrated circuits performing all speech, and line interface functions required in fully electronic telephone sets. The circuits internally perform electronic switching between dialling and speech.

Features

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical low-impedance inputs for dynamic and magnetic microphones (TEA1060)
- Symmetrical high-impedance inputs for piezoelectric microphone (TEA1061)
- Asymmetrical high-impedance input for electret microphone (TEA1061)
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large amplification setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent (microphone and earpiece amplifiers)
- Gain control adaptable to exchange supply
- DC line voltage adjustment facility

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Line voltage	I_{line} = 15 mA	V_{LN}	4.25	4.45	4.65	V
Line current operating range (pin 1)		I_{line}	10	–	140	mA
Internal supply current						
power down input LOW		I_{CC}	–	0.96	1.3	mA
power down input HIGH		I_{CC}	82	55	–	μA
Supply voltage for peripherals	I_{line} = 15 mA; MUTE input HIGH					
	I_P = 1.2 mA	V_{CC}	2.8	3.05	–	V
	I_P = 1.7 mA	V_{CC}	2.5	–	–	V
Voltage gain range						
microphone amplifier						
TEA1060		G_v	44	–	60	dB
TEA1061		G_v	30	–	46	dB
receiving amplifier		G_v	17	–	39	dB
Line loss compensation						
gain control range		ΔG_v	5.5	5.9	6.3	dB
Exchange supply voltage range		V_{exch}	24	–	60	V
Exchange feeding bridge resistance range		R_{exch}	400	–	1000	Ω
Operating ambient temperature range		T_{amb}	−25	–	+75	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

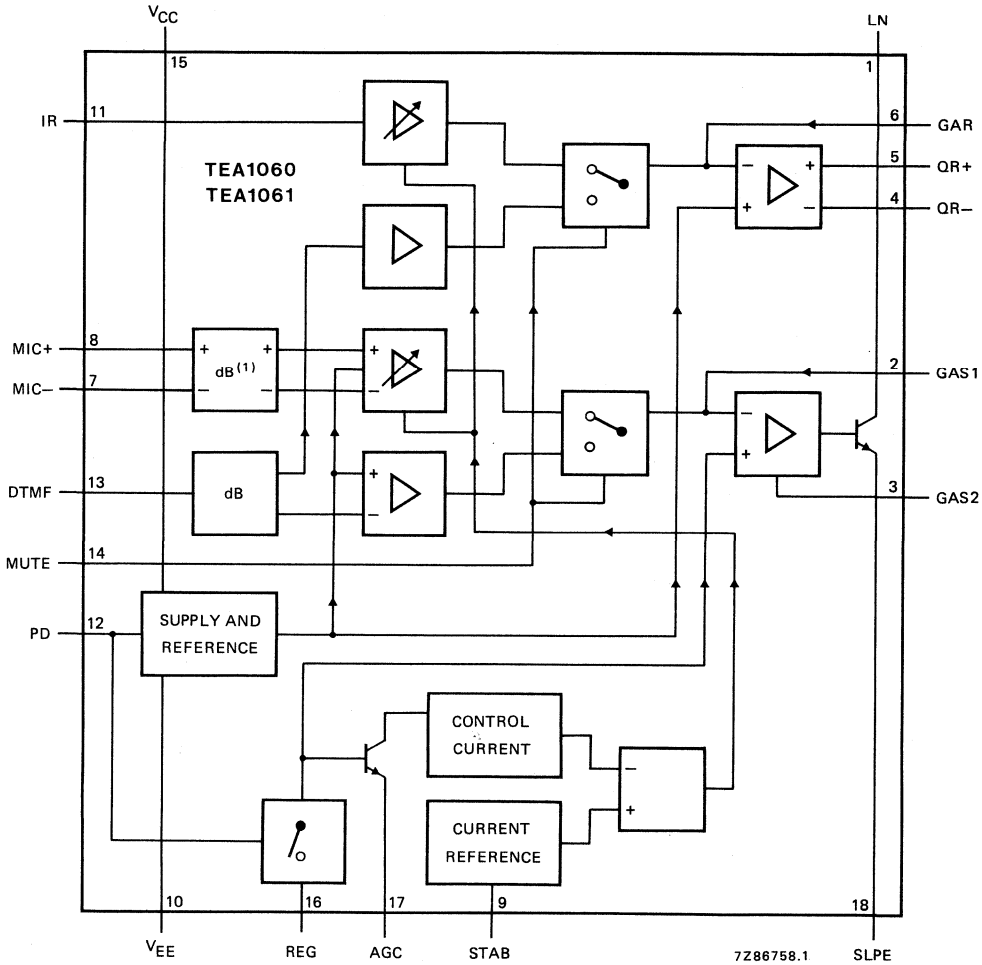


Fig.1 Block diagram.

The blocks marked "dB" are attenuators. The block marked (1) is only present in the TEA1061.

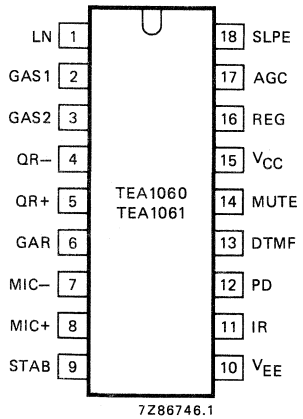


Fig.2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (DC resistance) adjustment

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripheral circuits are usually supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g. dialling and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3.6 kΩ between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the DC resistance of the subscriber line (R_{line}) and the DC voltage on the subscriber set (see Fig.4).

If the line current (I_{line}) exceeds the current I_{CC} + 0.5 mA required by the circuit itself (I_{CC} ca. 1 mA), plus the current I_P required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.
The voltage regulator adjusts the average voltage on LN to:
$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0.5 \times 10^{-3} A - I_P) \times R9$.

V_{ref} being an internally generated temperature compensated reference voltage of 4.2 V and R9 being an external resistor connected between SLPE and V_{EE}. The preferred value of R9 is 20 Ω. Changing R9 will have influence on microphone gain, DTMF gain, gain control characteristics, side tone and maximum output swing on LN.
Under normal conditions $I_{SLPE} \gg I_{CC}$ + 0.5 mA + I_P. The static behaviour of the circuit then equals a 4.2 V voltage regulator diode with an internal resistance R9. In the audio frequency range the dynamic impedance equals R1. The internal reference voltage can be adjusted by means of an external resistor R_{VA}. This resistor connected between pins 1 and 16 (LN and REG) will decrease the internal reference voltage. R_{VA} connected between pins 16 and 18 (REG and SLPE) will increase the internal reference voltage.

Supply: V_{CC}, LN, SLPE, REG and STAB (continued)

The current Ip available from V_{CC} for supplying peripheral circuits depends on external components and on the line current. Fig.5 shows this current for $V_{CC} > 2.2$ V and for $V_{CC} > 3$ V, of which 3 V is the minimum supply voltage for most CMOS circuits including a diode voltage drop for an enable diode. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven.

Microphone inputs MIC+ and MIC− and gain adjustment connections GAS1 and GAS2

The TEA1060 and TEA1061 have symmetrical microphone inputs.
The TEA1060 is intended for low-sensitivity low-impedance dynamic or magnetic microphones. Its input impedance is 8.2 kΩ (2 x 4.1 kΩ) and its voltage amplification is typ. 52 dB.
The TEA1061 is intended for a piezoelectric microphone or an electret microphone with built-in FET source follower. Its input impedance is 40.8 kΩ (2 x 20.4 kΩ) and its voltage amplification is typ. 38 dB.
The arrangements with the microphone types mentioned are shown in Fig.6.

The gain of the microphone amplifier in both types can be adjusted over a range of + and −8 dB to suit the sensitivity of the transducer used. The gain is proportional to external resistor R7 connected between GAS1 and GAS2.

An external capacitor (C6) of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 x C6.

Mute input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier, a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typ. 25.5 dB and varies with R7 in the same way as the gain of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR−. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig.7). The gain from IR to QR+ is typ. 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB and differential drive becomes possible.
This feature can be used in case the earpiece impedance exceeds 450 Ω (high-impedance dynamic, magnetic or piezoelectric earpieces).

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and RMS value is higher.

The gain of the receiving amplifier can be adjusted over a range of + and −8 dB to suit the sensitivity of the transducer used. The gain is proportional to external resistor R4 connected from GAR to QR+.

Two external capacitors C4 = 100 pF and C7 = 10 x C4 = 1 nF are necessary to ensure stability.
A larger value of C4 may be chosen to obtain a first-order low-pass filter. The "cut-off" frequency corresponds with the time constant R4 x C4.

Automatic gain control input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 6 dB. This corresponds with a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig.8 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range. If automatic line loss compensation is not required AGC may be left open. The amplifiers then all give their maximum gain as specified.

Power-down input PD

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, as a consequence it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input during the time of the loop break, which reduces the supply current from typ. 1 mA to typ. 55 μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall.
When this facility is not required PD may be left open.

DEVELOPMENT DATA

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the antiside-tone network consisting of $R1//Z_{line}$, R2, R3, R8 and Z_{bal} (see Fig.11). Maximum compensation is obtained when the following conditions are fulfilled:

$$a)\ R9.R2 = R1[R3 + (R8//Z_{bal})]$$

$$b)\ [Z_{bal}/(Z_{bal} + R8)] = [Z_{line}/(Z_{line} + R1)]$$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) will always be fulfilled provided that $|R8//Z_{bal}| \ll R3$.

To obtain optimum side-tone-suppression, condition (b) has to be fulfilled resulting in:

$$Z_{bal} = (R8/R1)Z_{line} = k.Z_{line}$$

where k is a scale factor; $k = (R8/R1)$

Scale factor k (value of R8) must be chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| \ll R3$
- $|Z_{bal} + R8| \gg R9$

In practice Z_{line} varies strongly with line length and cable type; consequently an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal} equals the average line impedance.

The anti-side-tone network as used in the standard application (Fig.11) attenuates the signal from the line with 32 dB. The attenuation is nearly flat over the audio-frequency range.
Instead of the above described special bridge, the conventional Wheatstone bridge configuration can be used as an alternative anti-side tone circuit. Both bridges can be used with either a resistive set impedance or with a complex set impedance.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

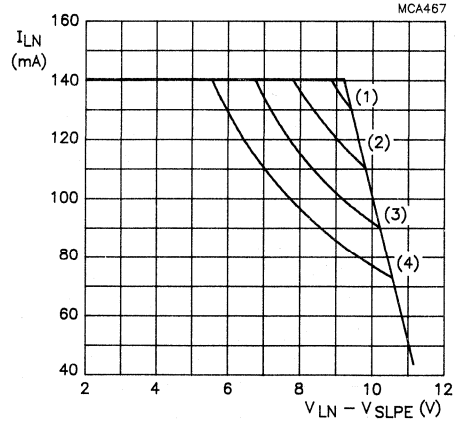
parameter	conditions	symbol	min.	max.	unit
Positive continuous line voltage		V_{LN}	–	12	V
Repetitive line voltage during switch-on or line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage for a 1 ms pulse per 5 s	R10 = 13 Ω; R9 = 20 Ω; (see Fig.11)	V_{LN}	–	28	V
Line current TEA1060 (1)	R9 = 20 Ω	I_{line}	–	140	mA
Line current TEA1061 (1)	R9 = 20 Ω	I_{line}	–	140	mA
Voltage on all other pins		V_i	–	$V_{CC}+0.7$	V
		$-V_i$	–	0.7	V
Total power dissipation (2)		P_{tot}	–	769	mW
Storage temperature range		T_{stg}	−40	+125	°C
Operating ambient temperature range		T_{amb}	−25	+75	°C
Junction temperature		T_j	–	+125	°C

1. Mostly dependent on the maximum required T_{amb} and the voltage between LN and SLPE (see Fig.3).
2. Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

From junction to ambient in free air
TEA1060 and TEA1061

$R_{th\ j\text{-}a}$ = 65 K/W



	T_{amb}	P_{tot}
(1)	45 °C	1231 mW
(2)	55 °C	1077 mW
(3)	65 °C	923 mW
(4)	75 °C	769 mW

Fig.3 TEA1060/1061 safe operating area.

DEVELOPMENT DATA

CHARACTERISTICS

I_{line} = 10 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C, R9 = 20 Ω; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 15)						
Voltage drop over circuit	I_{line} = 5 mA	V_{LN}	3.95	4.25	4.55	V
	I_{line} = 15 mA	V_{LN}	4.25	4.45	4.65	V
	I_{line} = 100 mA	V_{LN}	5.4	6.1	6.7	V
	I_{line} = 140 mA	V_{LN}	–	–	7.5	V
Variation with temperature	I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	−4	−2	0	mV/K
Voltage drop over circuit	I_{line} = 15 mA $R_{VA} = R_{1\text{-}16}$ = 68 kΩ	V_{LN}	3.5	3.8	4.05	V
	$R_{VA} = R_{16\text{-}18}$ = 39 kΩ	V_{LN}	4.7	5.0	5.3	V
Supply current	PD = LOW; V_{CC} = 2.8 V	I_{CC}	–	0.96	1.30	mA
	PD = HIGH; V_{CC} = 2.8 V	I_{CC}	–	55	82	μA
Supply voltage available for peripheral circuits	I_{line} = 15 mA; MUTE = HIGH					
	I_P = 0 mA	V_{CC}	3.5	3.75	–	V
	I_P = 1.2 mA	V_{CC}	2.8	3.05	–	V
Microphone inputs MIC+ and MIC− (pins 7 and 8)						
Input impedance						
TEA1060		$\lvert Z_i \rvert$	3.3	4.1	4.9	kΩ
TEA1061		$\lvert Z_i \rvert$	16.5	20.4	24.5	kΩ
Common-mode rejection ratio						
TEA1060		k_{CMR}	–	82	–	dB
Voltage gain	I_{line} = 15 mA; R7 = 68 kΩ					
TEA1060		G_v	51	52	53	dB
TEA1061		G_v	37	38	39	dB
Variation with frequency referred to 800 Hz	f = 300 and 3400 kHz	ΔG_{vf}	−0.5	±0.2	+0.5	dB
Variation with temperature referred to +25 °C	I_{line} = 50 mA; T_{amb} = −25 and +75 °C	ΔG_{vT}	–	±0.2	–	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Dual-tone multi-frequency input DTMF (pin 13)						
Input impedance		$\|Z_i\|$	16.8	20.7	24.6	kΩ
Voltage gain	I_{line} = 15 mA; R7 = 68 kΩ	G_v	24.5	25.5	26.5	dB
Variation with frequency referred to 800 Hz	f = 300 and 3400 kHz	ΔG_{vf}	−0.5	±0.2	+0.5	dB
Variation with temperature referred to 800 Hz	I_{line} = 50 mA; T_{amb} = −25 and +75 °C	ΔG_{vT}	−	±0.2	−	dB
Gain adjustment GAS1 and GAS2 (pins 2 and 3)						
Gain variation with R7 connected between pins 2 and 3; transmitting amplifier		ΔG_v	−8	−	+8	dB
Transmitting amplifier output LN (pin 1)						
Output voltage	I_{line} = 15 mA; d_{tot} = 2%	$V_{LN(rms)}$	1.9	2.3	−	V
	d_{tot} = 10%	$V_{LN(rms)}$	−	2.6	−	V
Noise output voltage	I_{line} = 15 mA; R7 = 68 kΩ; pins 7 and 8 open circuit psophometrically weighted (P53 curve)	$V_{no(rms)}$	−	−70	−	dBmp
Receiving amplifier input IR (pin 11)						
Input impedance		$\|Z_i\|$	17	21	25	kΩ
Receiving amplifier outputs QR+ and QR− (pins 4 and 5)						
Output impedance; single-ended		$\|Z_o\|$	−	4	−	Ω
Voltage gain from pin 11 to pin 4 or 5	I_{line} = 15 mA; R4 = 100 kΩ					
single-ended	R_L = 300 Ω	G_v	24	25	26	dB
differential	R_L = 600 Ω	G_v	30	31	32	dB

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Variation with frequency referred to 800 Hz	f = 300 and 3400 Hz	ΔG_{vf}	−0.5	±0.2	+0.5	dB
Variation with temperature referred to 800 Hz	I_{line} = 15 mA; T_{amb} = −25 and +75 °C	ΔG_{vT}	–	±0.2	–	dB
Output voltage	I_P = 0 mA; d_{tot} = 2%;					
sine-wave drive	R4 = 100 kΩ					
single-ended	R_L = 150 Ω	$V_{o(rms)}$	0.3	0.38	–	V
single-ended	R_L = 450 Ω	$V_{o(rms)}$	0.4	0.52	–	V
differential	C_L = 47 nF					
R_{series} = 100 Ω	f = 3400 Hz	$V_{o(rms)}$	0.8	1.0	–	V
Noise output voltage	I_{line} = 15 mA; R4 = 100 kΩ; pin 11 open circuit psophometrically weighted (P53 curve)					
single-ended	R_L = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential	R_L = 600 Ω	$V_{no(rms)}$	–	100	–	μV
Gain adjustment GAR (pin 6)						
Gain variation with R4 connected between pins 6 and 5; receiving amplifier		ΔG_v	−8	–	+8	dB
MUTE input (pin 14)						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{MUTE}	–	8	15	μA
Reduction of voltage gain from MIC+ and MIC− to LN	MUTE = HIGH	ΔG_v	–	70	–	dB
Voltage gain from DTMF to QR+ or QR−	MUTE = HIGH R4 = 100 kΩ					
single-ended load	R_L = 300 Ω	G_v	−21	−19	−17	dB
Power-down input PD (pin 12)						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{PD}	–	5	10	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Automatic gain control input AGC (pin 17)						
Controlling the gain from IR to QR+/QR− and the gain from MIC+/MIC− to LN; R6 = 110 kΩ (connected between pins 17 and 10)						
Gain control range	I_{line} = 70 mA	$-\Delta G_v$	5.5	5.9	6.3	dB
Highest line current for maximum gain		I_{line}	–	23	–	mA
Lowest line current for lowest gain		I_{line}	–	61	–	mA
Reduction of gain between I_{line} = 15 mA and I_{line} = 35 mA		$-\Delta G_v$	1.0	1.5	2.0	dB

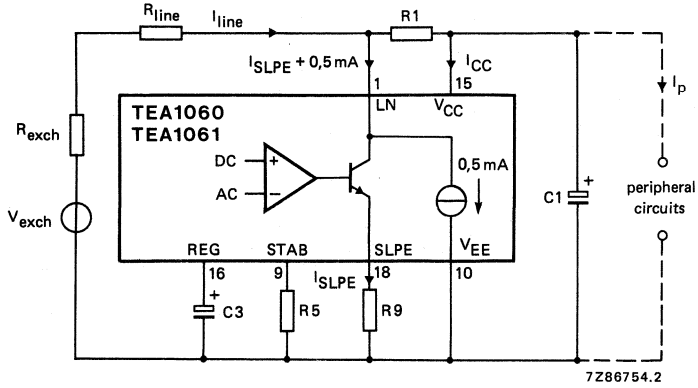
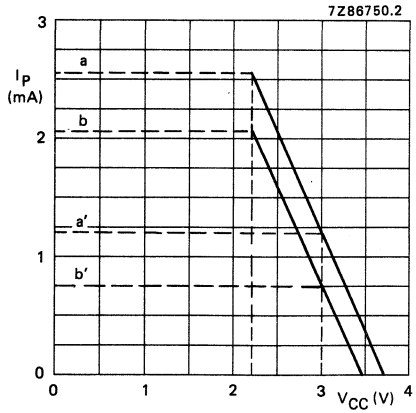


Fig.4 Supply arrangement.

DEVELOPMENT DATA



I_{line} = 15 mA at
V_{LN} = 4.45 V;
R1 = 620 Ω, R9 = 20 Ω

Fig.5 Maximum current Ip available from V_{CC} for external (peripheral) circuitry with $V_{CC} > 2.2$ V and $V_{CC} > 3$ V. Curves (a) and (a') are valid when the receiving amplifier is not driven or when MUTE = HIGH. Curves (b) and (b') are valid when MUTE = LOW and the receiving amplifier is driven. $V_{o(rms)}$ = 150 mV, R_L = 150 Ω (asymmetrical).

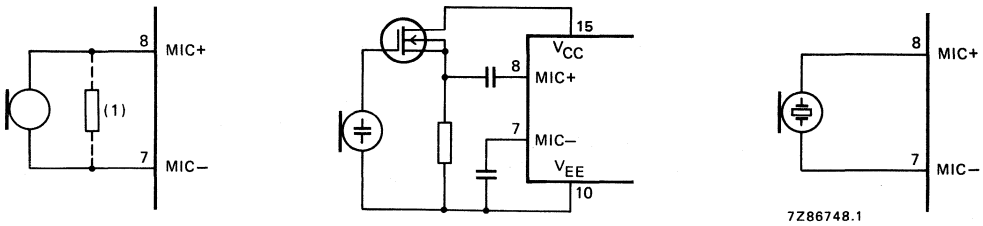


Fig.6 Alternative microphone arrangements: (a) magnetic or dynamic microphone for TEA1060, the resistor marked (1) may be connected to lower the terminating impedance, (b) electret microphone and (c) piezoelectric microphone for TEA1061.

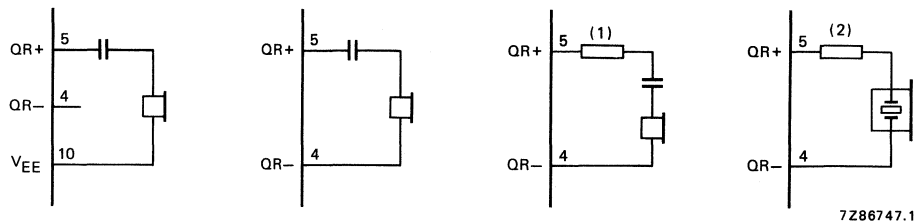


Fig.7 Alternative receiver arrangements: (a) dynamic earpiece with less than 450 Ω impedance, (b) dynamic earpiece with more than 450 Ω impedance, (c) magnetic earpiece. The resistor marked (1) may be connected to prevent distortion [inductive load (d)] piezoelectric earpiece. The resistor marked (2) is required to increase the phase margin (capacitive load).

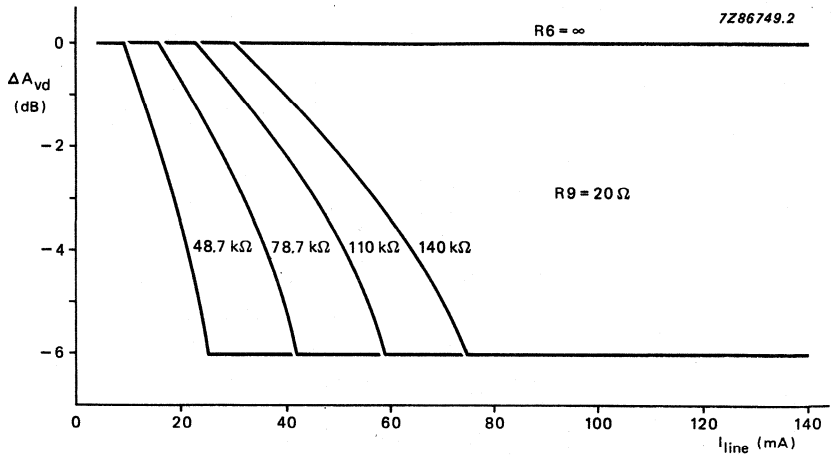


Fig.8 Variation of gain with line current with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}; R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	24	61.9	48.7	X	X
	36	100	78.7	68	60.4
	48	140	110	93.1	82
	60	X	X	120	102

DEVELOPMENT DATA

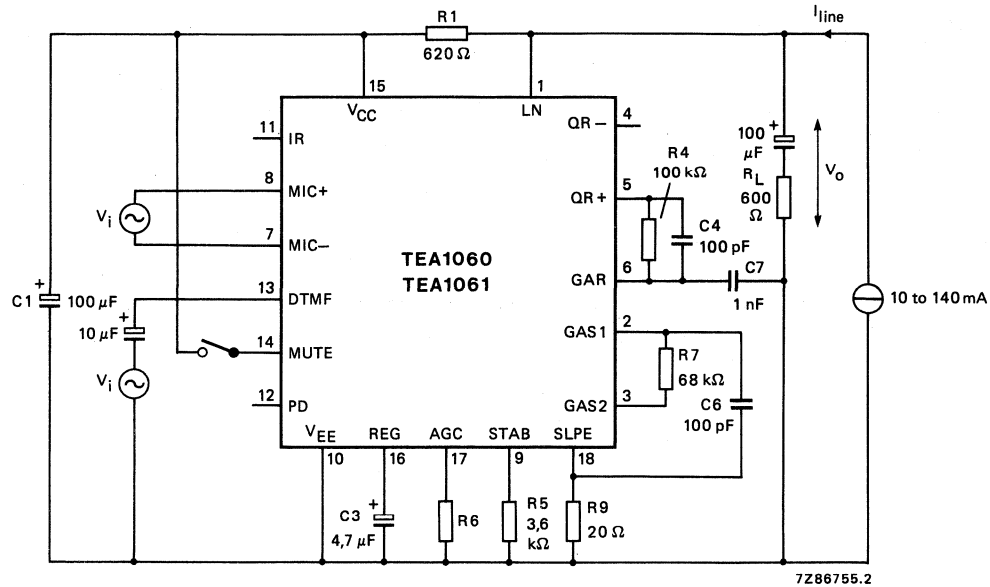


Fig.9 Test circuit for defining voltage gain of MIC+, MIC– and DTMF inputs. Voltage gain is defined as; $G_V = 20 \log |V_o/V_i|$. For measuring the gain from MIC+ and MIC– the MUTE input should be LOW or open circuit. For measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open circuit.

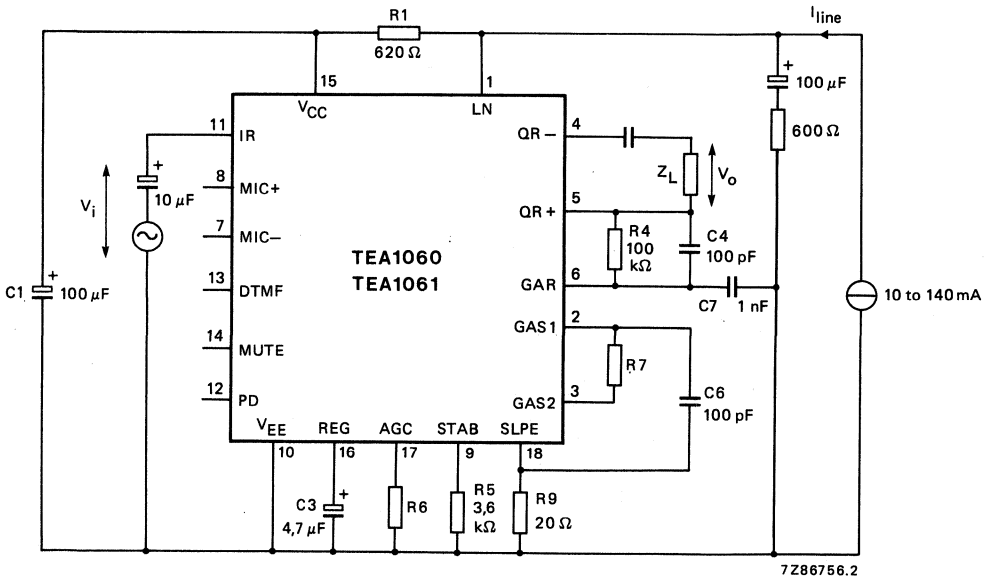


Fig.10 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as; $G_V = 20 \log |V_o/V_i|$.

DEVELOPMENT DATA

APPLICATION INFORMATION

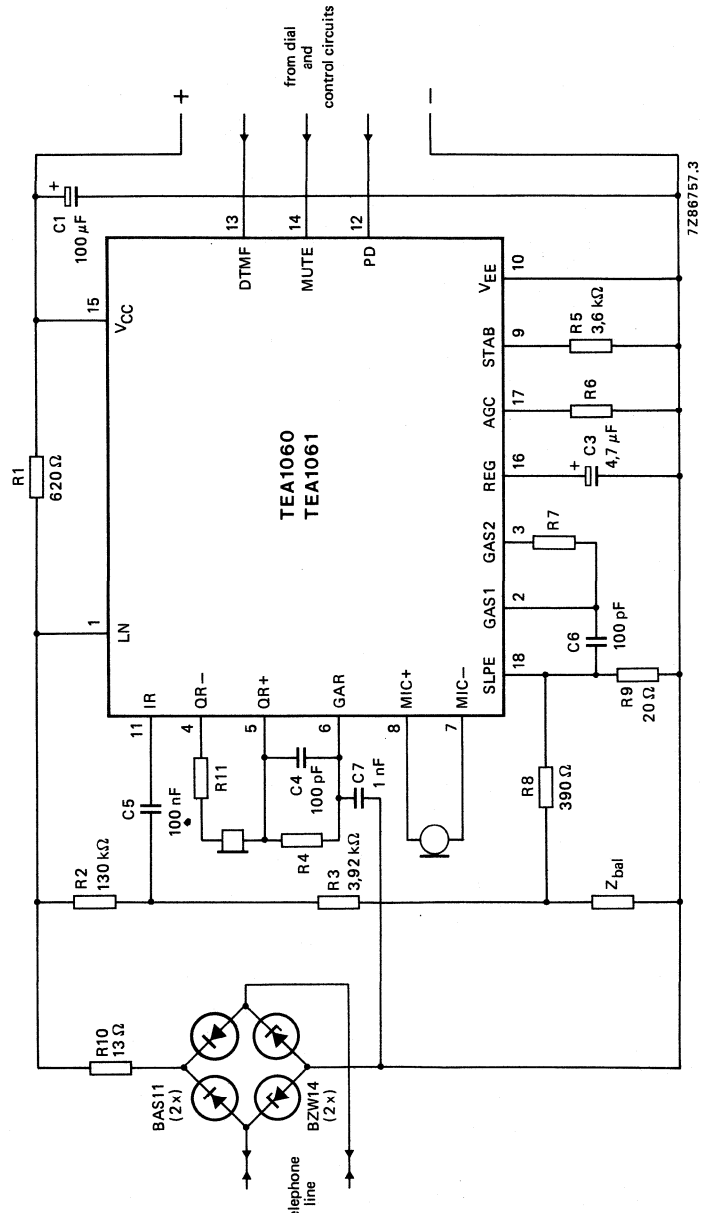


Fig.11 Typical application of the TEA1060 or TEA1061, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

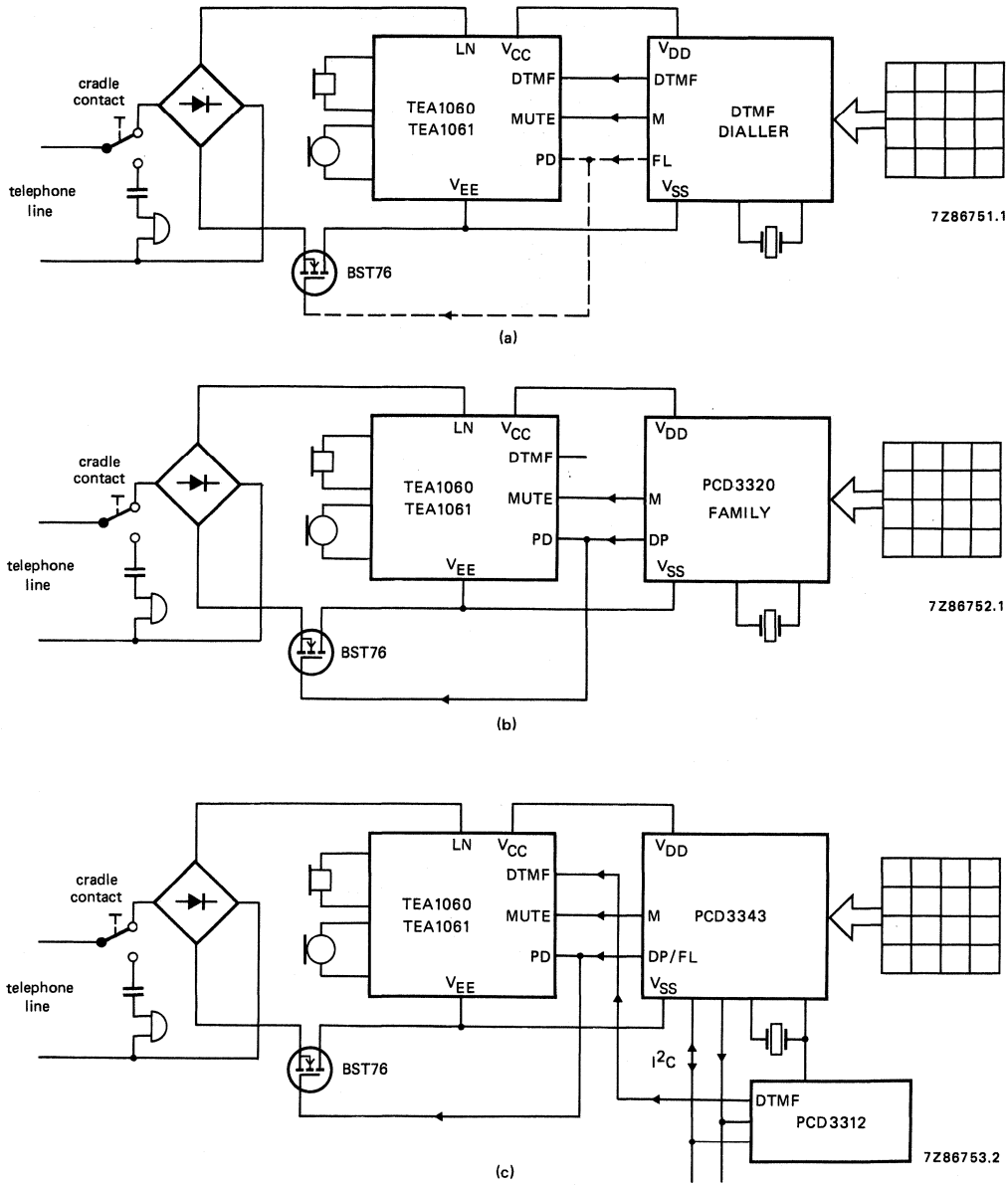


Fig.12 Typical applications of the TEA1060 or TEA1061 (simplified): (a) DTMF set with a CMOS DTMF dialling circuit, the dashed lines show an optional flash (register recall by timed loop break); (b) Pulse dial set with the one of the PCD3320 family of CMOS interrupted current-loop dialling circuits; (c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C-bus.

LOW VOLTAGE TELEPHONE TRANSMISSION CIRCUIT WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1062 is a bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech. The circuit is able to operate down to a DC line voltage of 1.6 V (with reduced performance) to facilitate the use of more telephone sets in parallel.

Features

- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable static resistance
- Provides supply with limited current for external circuitry
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezoelectric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Receiving amplifier for various types of earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line current dependent line loss facility for microphone and earpiece amplifiers
- Gain control adaptable to exchange supply
- DC line voltage adjustment capability

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Line voltage	I_{line} = 15 mA	V_{LN}	3.55	4.0	4.25	V
Line current operating range	normal operation					
TEA1062		I_{line}	11	–	140	mA
TEA1062T		I_{line}	11	–	140	mA
	with reduced performance	I_{line}	1	–	11	mA
Internal supply current		I_{CC}	–	0.9	–	mA
Supply voltage for peripherals	I_{line} = 15 mA; Ip = 1.2 mA mute input HIGH	V_{CC}	2.2	2.7	–	V
	I_{line} = 15 mA; Ip = 0 mA mute input HIGH	V_{CC}	–	3.4	–	V
Voltage gain range						
microphone amplifier		G_v	44	–	52	dB
receiving amplifier		G_v	20	–	31	dB
Line loss compensation gain control range		ΔG_v	–	5.8	–	dB
Exchange supply voltage range		V_{exch}	36	–	60	V
Exchange feeding bridge resistance range		R_{exch}	0.4	–	1	kΩ
Operating ambient temperature range		T_{amb}	−25	–	+75	°C

PACKAGE OUTLINES

TEA1062 : 16-lead DIL; plastic (SOT38).
TEA1062T: 16-lead mini-pack; plastic (SO16; SOT109A).

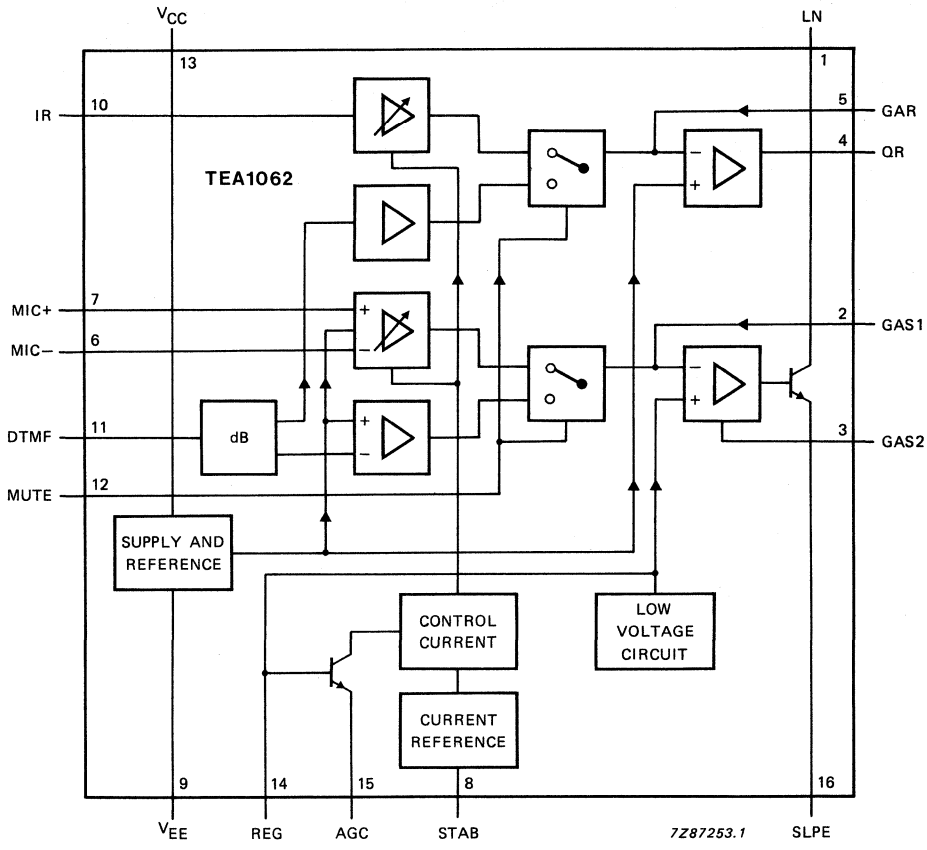


Fig.1 Block diagram.

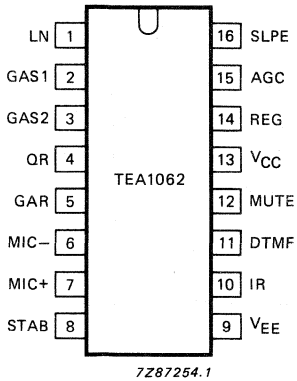


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR	non-inverting output, receiving amplifier
5	GAR	gain adjustment; receiving amplifier
6	MIC−	inverting microphone input
7	MIC+	non-inverting microphone input
8	STAB	current stabilizer
9	V_{EE}	negative line terminal
10	IR	receiving amplifier input
11	DTMF	dual-tone multi-frequency input
12	MUTE	mute input
13	V_{CC}	positive supply decoupling
14	REG	voltage regulator decoupling
15	AGC	automatic gain control input
16	SLPE	slope (DC resistance) adjustment

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

Power for the TEA1062 and its peripheral circuits is usually obtained from the telephone line. The IC supply voltage is derived from the line via a dropping resistor and regulated by the TEA1062. The supply voltage V_{CC} may also be used to supply external circuits e.g. dialling and control circuits.

Decoupling of the supply voltage is performed by a capacitor between V_{CC} and V_{EE} while the internal voltage regulator is decoupled by a capacitor between REG and V_{EE}.

The DC current drawn by the device will vary in accordance with varying values of the exchange voltage (V_{exch}), the feeding bridge resistance (R_{exch}) and the DC resistance of the telephone line (R_{line}).

The TEA1062 has an internal current stabilizer operating at a level determined by a 3.6 kΩ resistor connected between STAB and V_{EE} (see Fig.8). When the line current (I_{line}) is more than 0.5 mA greater than the sum of the IC supply current (I_{CC}) and the current drawn by the peripheral circuitry connected to V_{CC} (I_P) the excess current is shunted to V_{EE} via LN.

The regulated voltage on the line terminal (V_{LN}) can be calculated as:

$$V_{LN} = V_{ref} + I_{SLPE} \times R9 \text{ or;}$$

$$V_{LN} = V_{ref} + [(I_{line} - I_{CC} - 0.5 \times 10^{-3}\ A) - I_P] \times R9$$

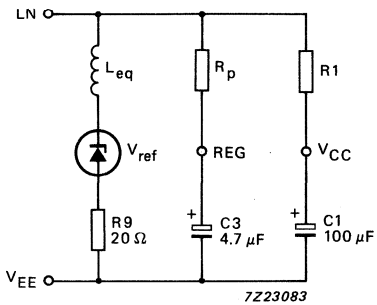
where: V_{ref} is an internally generated temperature compensated reference voltage of 3.7 V and R9 is an external resistor connected between SLPE and V_{EE}. In normal use the value of R9 would be 20 Ω. Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics, side-tone level, maximum output swing on LN and the DC characteristics (especially at the lower voltages).

Under normal conditions, when $I_{SLPE} \geqslant I_{CC} + 0.5$ mA + I_P, the static behaviour of the circuit is that of a 3.7 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1. Fig.3 shows the equivalent impedance of the circuit.

FUNCTIONAL DESCRIPTION (continued)

At line currents below 9 mA the internal reference voltage is automatically adjusted to a lower value (typically 1.6 V at 1 mA). This means that more sets can be operated in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. With line currents below 9 mA the circuit has limited sending and receiving levels. The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor when connected between LN and REG will decrease the internal reference voltage and when connected between REG and SLPE will increase the internal reference voltage.

Current (I_P) available from V_{CC} for peripheral circuits depends on the external components used. Fig.9 shows this current for $V_{CC} > 2.2$ V. If MUTE is LOW when the receiving amplifier is driven the available current is further reduced. Current availability can be increased by connecting the supply IC (TEA1081) in parallel with R1, as shown in Fig.16 (c), or, by increasing the DC line voltage by means of an external resistor (R_{VA}) connected between REG and SLPE.



R_P = 16.2 kΩ
L_{eq} = C3 x R9 x R_P

Fig.3 Equivalent impedance circuit.

Microphone inputs (MIC+ and MIC−) and gain pins (GAS1 and GAS2)

The TEA1062 has symmetrical inputs. Its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage gain is typically 52 dB (when R7 = 68 kΩ, see Fig.13). Dynamic, magnetic, piezoelectric or electret (with built-in FET source followers) can be used. Microphone arrangements are illustrated in Fig.10.

The gain of the microphone amplifier can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer in use. The gain is proportional to the value of R7 which is connected between GAS1 and GAS2. Stability is ensured by the external capacitors, C6 connected between GAS1 and SLPE and C8 connected between GAS1 and V_{EE}. The value of C6 is 100 pF but this may be increased to obtain a first-order low-pass filter. The value of C8 is 10 times the value of C6. The cut-off frequency corresponds to the time constant R7 x C6.

Mute input (MUTE)

When MUTE is HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when MUTE is LOW or open-circuit. MUTE switching causes only negligible clicking on the line and earpiece output. If the number of parallel sets in use causes a drop in line current to below 6 mA the speech amplifiers remain active independent to the DC level applied to the MUTE input.

Dual-tone multi-frequency input (DTMF)

When the DTMF input is enabled dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the microphone gain. The signalling tones can be heard in the earpiece at a low level (confidence tone).

DEVELOPMENT DATA

Receiving Amplifier (IR, QR and GAR)

The receiving amplifier has one input (IR) and a non-inverting output (QR). Earpiece arrangements are illustrated in Fig.11. The IR to QR gain is typically 31 dB (when R4 = 100 kΩ). It can be adjusted between 20 and 31 dB to match the sensitivity of the transducer in use. The gain is set with the value of R4 which is connected between GAR and QR. The overall receive gain, between LN and QR, is calculated by substracting the anti-sidetone network attenuation (32 dB) from the amplifier gain. Two external capacitors, C4 and C7, ensure stability. C4 is normally 100 pF and C7 is 10 times the value of C4. The value of C4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant R4 x C4.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.

Automatic gain control input (AGC)

Automatic line loss compensation is achieved by connecting a resistor (R6) between AGC and V_{EE}. The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 5.8 dB which corresponds to a line length of 5 km for a 0.5 mm diameter twisted pair copper cable with a DC resistance of 176 Ω/km and average attenuation of 1.2 dB/km. Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig.12 and Table 1). The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line loss compensation is required the AGC may be left open-circuit. The amplifiers, in this condition, will give their maximum specified gain.

FUNCTIONAL DESCRIPTION (continued)

Side-tone suppression

The anti-sidetone network, $R1//Z_{line}$, R2, R3, R8, R9 and Z_{bal}, (see Fig.4) suppresses the transmitted signal in the earpiece. Compensation is maximum when the following conditions are fulfilled:

(a) $R9 \times R2 = R1\,[R3 + (R8//Z_{bal})]$;

(b) $[Z_{bal}/(Z_{bal} + R8)] = [Z_{line}/(Z_{line} + R1)]$

If fixed values are chosen for R1, R2, R3 and R9 then condition (a) will always be fulfilled when $|R8/Z_{bal}| \ll R3$. To obtain optimum side-tone suppression condition (b) has to be fulfilled which results in:

$Z_{bal} = (R8/R1)Z_{line} = k.Z_{line}$ where k is a scale factor; $k = (R8/R1)$

The scale factor (k), dependent on the value of R8, is chosen to meet the following criteria:

(a) Compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}

(b) $|Z_{bal}//R8| \ll R3$ fulfilling condition (a) and thus ensuring correct anti-sidetone bridge operation

(c) $|Z_{bal} + R8| \gg R9$ to avoid influencing the transmitter gain

In practice Z_{line} varies considerably with the line type and length. The value chosen for Z_{bal} should therefore be for an average line length thus giving optimum setting for short or long lines.

Example

The balance impedance Z_{bal} at which the optimum suppression is present can be calculated by:

Suppose $Z_{line} = 210\ \Omega + (1265\ \Omega//140\ nF)$ representing a 5 km line of 0.5 mm diameter, copper, twisted pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).
When k = 0.64 then R8 = 390 Ω, $Z_{bal} = 130\ \Omega + (820\ \Omega//220\ nF)$.

The anti-sidetone network for the TEA1060 family shown in Fig.4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. Fig.5 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances.

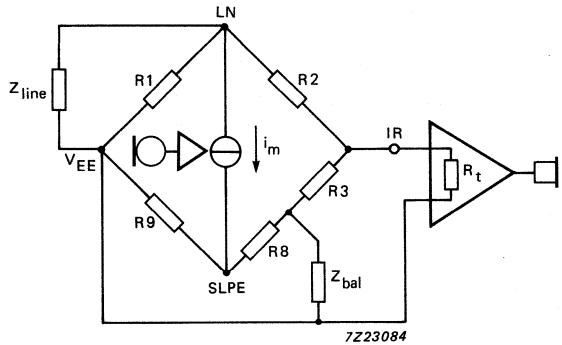


Fig.4 Equivalent circuit of TEA1060 anti-sidetone bridge.

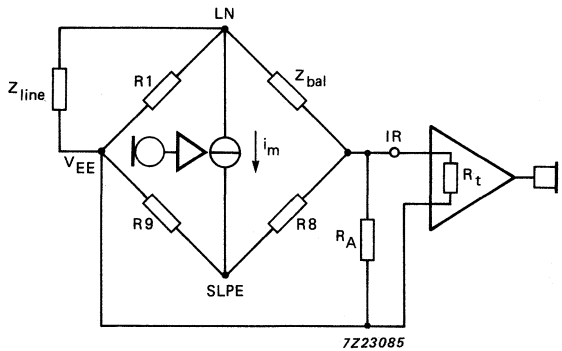


Fig.5 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

More information can be found in the Designer guide.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

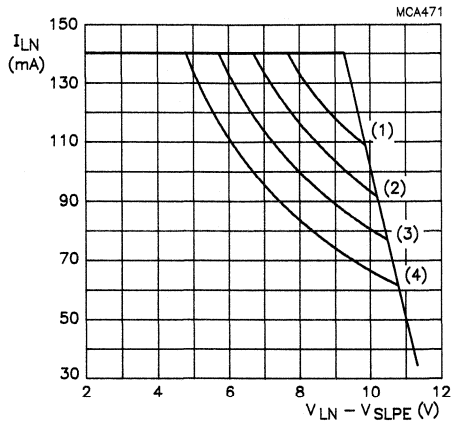
parameter	conditions	symbol	min.	max.	unit
Positive continuous line voltage		V_{LN}	–	12	V
Repetitive line voltage during switch-on or line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage for a 1 ms pulse/5 s	R10 = 13 Ω; R9 = 20 Ω; (see Fig.15)	V_{LN}	–	28	V
Line current TEA1062 (1)	R9 = 20 Ω	I_{line}	–	140	mA
Line current TEA1062T (1)	R9 = 20 Ω	I_{line}	–	140	mA
Voltage on all other pins		V_i	–	V_{CC} +0.7	V
		$-V_i$	–	0.7	V
Total power dissipation (2)	R9 = 20 Ω				
TEA1062		P_{tot}	–	666	mW
TEA1062T		P_{tot}	–	454	mW
Storage temperature range		T_{stg}	–40	+125	°C
Operating ambient temperature range		T_{amb}	–25	+75	°C
Junction temperature		T_j	–	+125	°C

1. Mostly dependent on the maximum required T_{amb} and the voltage between LN and SLPE (see Figs 6 and 7).
2. Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

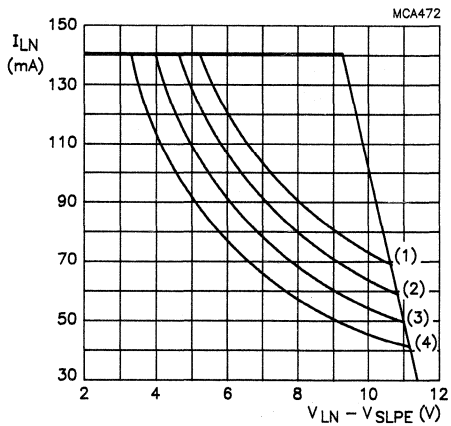
From junction to ambient in free air

TEA1062	$R_{th\ j\text{-}a}$	=	75 K/W
TEA1062T mounted on glassy epoxy board 28.5 x 19.1 x 1.5 mm	$R_{th\ j\text{-}a}$	=	110 K/W



	T_{amb}	P_{tot}
(1)	45 °C	1068 mW
(2)	55 °C	934 mW
(3)	65 °C	800 mW
(4)	75 °C	666 mW

Fig.6 TEA1062 safe operating area.



	T_{amb}	P_{tot}
(1)	45 °C	727 mW
(2)	55 °C	636 mW
(3)	65 °C	545 mW
(4)	75 °C	454 mW

Fig.7 TEA1062T safe operating area.

DEVELOPMENT DATA

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply; LN and V_{CC} (pins 1 and 13)						
Voltage drop over circuit, between LN and V_{EE}	MIC inputs open					
	I_{line} = 1 mA	V_{LN}	–	1.6	–	V
	I_{line} = 4 mA	V_{LN}	–	1.9	–	V
	I_{line} = 15 mA	V_{LN}	3.55	4.0	4.25	V
	I_{line} = 100 mA	V_{LN}	4.9	5.7	6.5	V
	I_{line} = 140 mA	V_{LN}	–	–	7.5	V
Variation with temperature	I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	–	–0.3	–	mV/K
Voltage drop over circuit, between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA R_{VA} (LN to REG) = 68 kΩ		–	3.5	–	V
	I_{line} = 15 mA R_{VA} (REG to SLPE) = 39 kΩ		–	4.5	–	V
Supply current	V_{CC} = 2.8 V	I_{CC}	–	0.9	1.35	mA
Supply voltage available for peripheral circuitry	I_{line} = 15 mA MUTE = HIGH					
	I_P = 1.2 mA	V_{CC}	2.2	2.7	–	V
	I_P = 0 mA	V_{CC}	–	3.4	–	V
Microphone inputs MIC+ and MIC– (pins 6 and 7)						
Input impedance (differential) between MIC– and MIC+		$\lvert Z_i \rvert$	–	64	–	kΩ
Input impedance (single-ended) MIC– or MIC+ to V_{EE}		$\lvert Z_i \rvert$	–	32	–	kΩ
Common mode rejection ratio		k_{CMR}	–	82	–	dB
Voltage gain MIC+ or MIC– to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	50.5	52.0	53.5	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	–	±0.2	–	dB
Gain variation with temperature at –25 °C and +75 °C	w.r.t 25 °C without R6; I_{line} = 50 mA	ΔG_{vT}	–	±0.2	–	dB

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Dual-tone multi-frequency input DTMF (pin 11)						
Input impedance		$\|Z_i\|$	–	20.7	–	kΩ
Voltage gain from DTMF to LN	I_{line} = 15 mA R7 = 68 kΩ	G_v	24.0	25.5	27.0	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	–	±0.2	–	dB
Gain variation with temperature at –25 °C and +75 °C	w.r.t. 25 °C I_{line} = 50 mA	ΔG_{vT}	–	±0.2	–	dB
Gain adjustment GAS1 and GAS2 (pins 2 and 3)						
Gain variation of the transmitting amplifier by varying R_7 between GAS1 and GAS2		ΔG_v	–8	–	0	dB
Sending amplifier output LN (pin 1)						
Output voltage	I_{line} = 15 mA THD = 10%	$V_{LN(rms)}$	1.7	2.3	–	V
	I_{line} = 4 mA; THD = 10%	$V_{LN(rms)}$	–	0.8	–	V
Noise output voltage	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	–69	–	dBmp
Receiving amplifier input IR (pin 10)						
Input impedance		$\|Z_i\|$	–	21	–	kΩ
Receiving amplifier output QR (pin 4)						
Output impedance		$\|Z_o\|$	–	4	–	Ω
Voltage gain from IR to QR	I_{line} = 15 mA; R_L (from pin 9 to pin 4) = 300 Ω	G_v	29.5	31	32.5	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	–	±0.2	–	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Receiving amplifier output QR (pin 4) (continued)						
Gain variation with temperature at −25 °C and +75 °C	w.r.t. 25 °C without R6; I_{line} = 50 mA	ΔG_{vT}	–	±0.2	–	dB
Output voltage	sinewave drive; Ip = 0 mA; THD = 2%; R4 = 100 kΩ; I_{line} = 15 mA					
	R_L = 150 Ω	$V_{o(rms)}$	0.22	0.33	–	V
	R_L = 450 Ω	$V_{o(rms)}$	0.3	0.48	–	V
Output voltage	THD = 10% R4 = 100 kΩ; R_L = 150 Ω I_{line} = 4 mA	$V_{o(rms)}$	–	15	–	mV
Noise output voltage	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted; (P53 curve)					
	R_L = 300 Ω	$V_{no(rms)}$	–	50	–	μV
Gain adjustment GAR (pin 5)						
Gain variation of receiving amplifier achievable by varying R_4 between GAR and QR		ΔG_v	−11	–	0	dB
Mute input (pin 12)						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{MUTE}	–	8	15	μA
Reduction of gain MIC+ or MIC− to LN	MUTE = HIGH	ΔG_v	–	70	–	dB
Voltage gain from DTMF to QR	MUTE = HIGH; R4 = 100 kΩ; R_L = 300 Ω	G_v	–	−19	–	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Automatic gain control input AGC (pin 15)						
Controlling the gain from IR to QR and the gain from MIC+/MIC− to LN; R_6 between AGC and V_{EE}	R6 = 110 kΩ					
Gain control range	I_{line} = 70 mA	ΔG_v	−	−5.8	−	dB
Highest line current for maximum gain		I_{line}	−	23	−	mA
Minimum line current for minimum gain		I_{line}	−	61	−	mA

DEVELOPMENT DATA

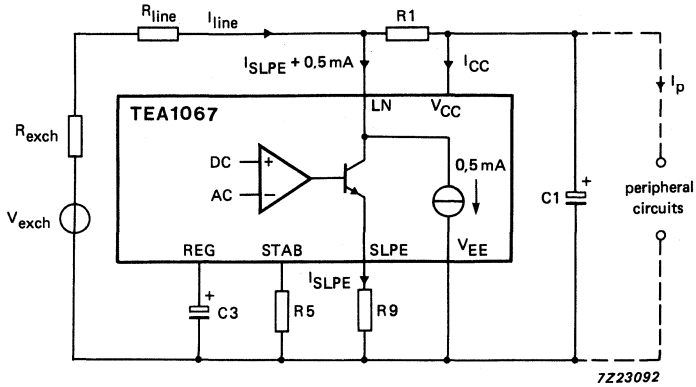
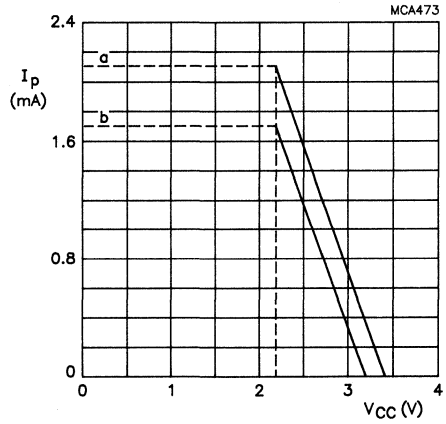
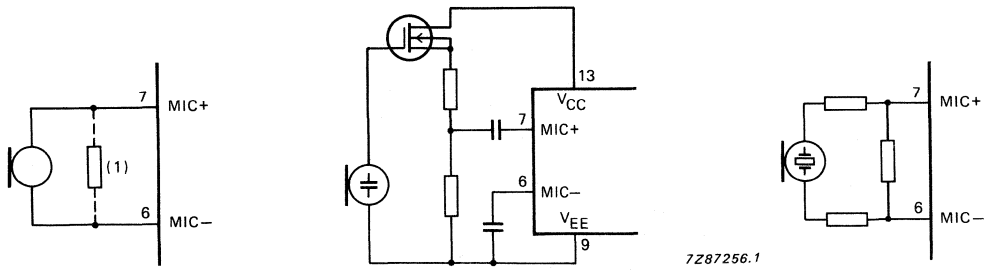


Fig.8 Supply arrangement.



(a) I_P = 2.1 mA
(b) I_P = 1.7 mA
I_{line} = 15 mA at V_{LN} = 4 V
R1 = 620 Ω and R9 = 20 Ω

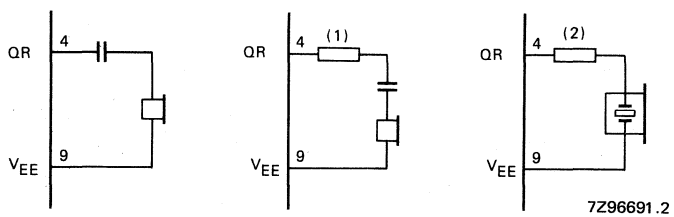
Fig.9 Typical current I_P available from V_{CC} for peripheral circuitry with $V_{CC} >= 2.2$ V. Curve (a) is valid when the receiving amplifier is not driven or when MUTE = HIGH. Curve (b) is valid when MUTE = LOW and the receiving amplifier is driven; $V_{o(rms)}$ = 150 mV, R_L = 150 Ω.
The supply possibilities can be increased simply by setting the voltage drop over the circuit V_{LN} to a higher value by means of resistor R_{VA} connected between REG and SLPE.



(a) (b) (c)

(a) Magnetic or dynamic microphone. The resistor marked (1) may be connected to decrease the terminating impedance.
(b) Electret microphone.
(c) Piezoelectric microphone.

Fig.10 Alternative microphone arrangements.



(a) (b) (c)

(a) Dynamic earpiece.
(b) Magnetic earpiece. The resistor marked (1) may be connected to prevent distortion (inductive load).
(c) Piezoelectric earpiece. The resistor marked (2) is required to increase the phase margin (capacitive load).

Fig.11 Alternative receiver arrangements.

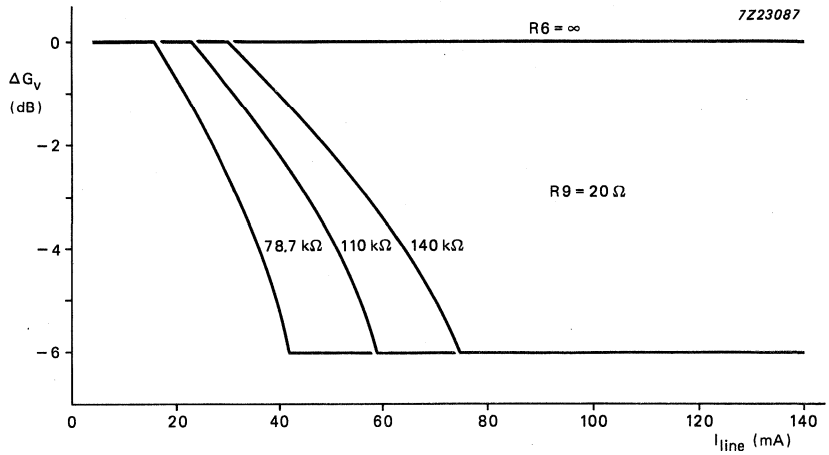


Fig.12 Variation of gain with line current, with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	36	100	78.7	X	X
	48	140	110	93.1	82
	60	X	X	120	102

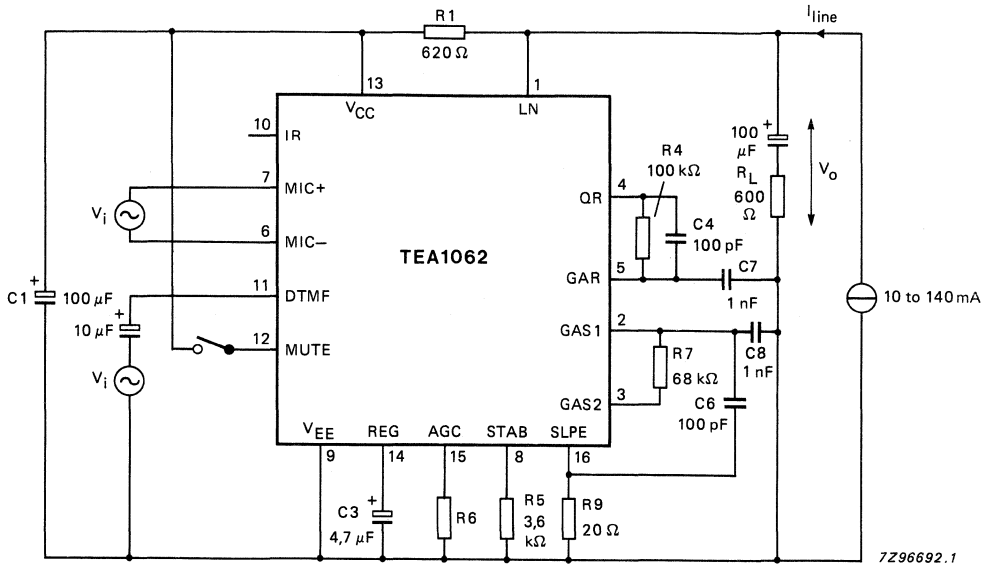


Fig.13 Test circuit for defining voltage gain of MIC+, MIC– and DTMF inputs. Voltage gain is defined as; $G_v = 20 \log |V_o/V_i|$. For measuring the gain from MIC+ and MIC– the MUTE input should be LOW or open circuit, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open circuit.

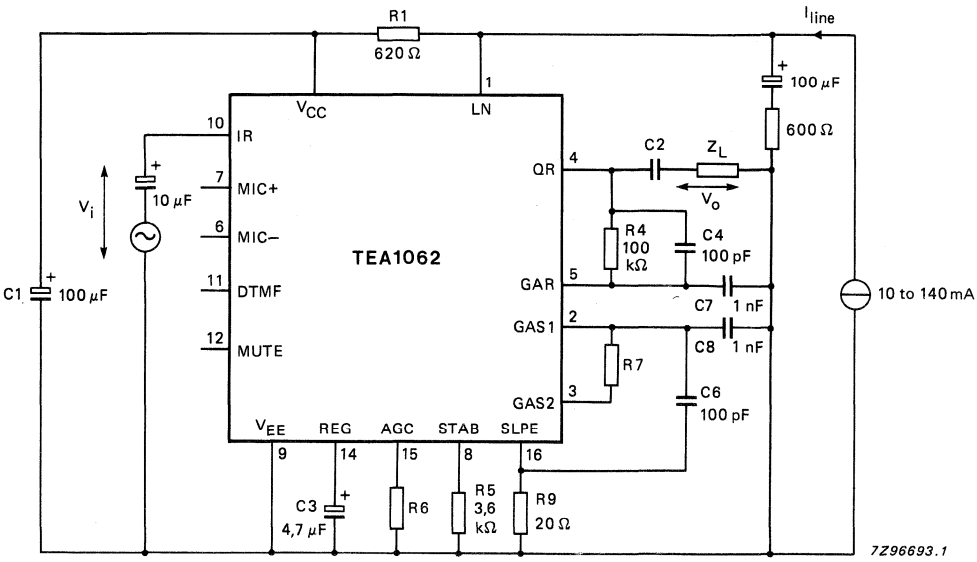


Fig.14 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as; $G_v = 20 \log |V_o/V_i|$.

DEVELOPMENT DATA

APPLICATION INFORMATION

Further information can be found in Application note ETT/AN 89008.

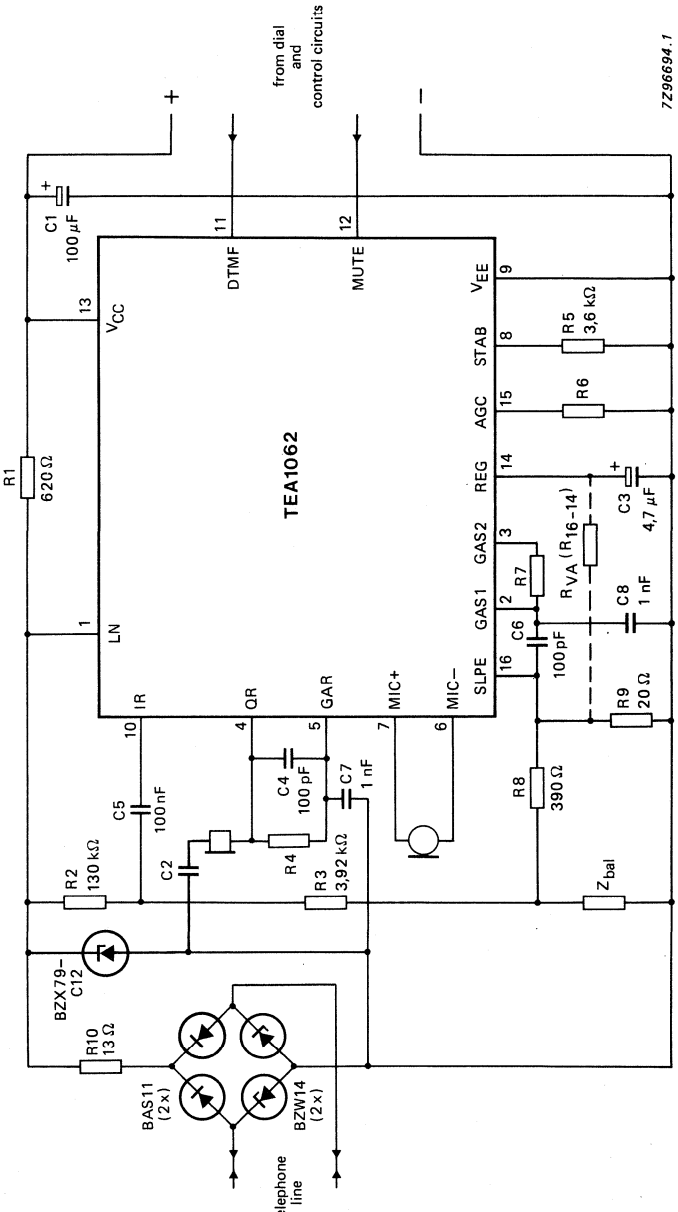


Fig.15 Typical application of the TEA1062, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left, the zener diode and R_{10} limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.
The DC line voltage can be set to a higher value by the resistor R_{VA}(REG to SLPE).

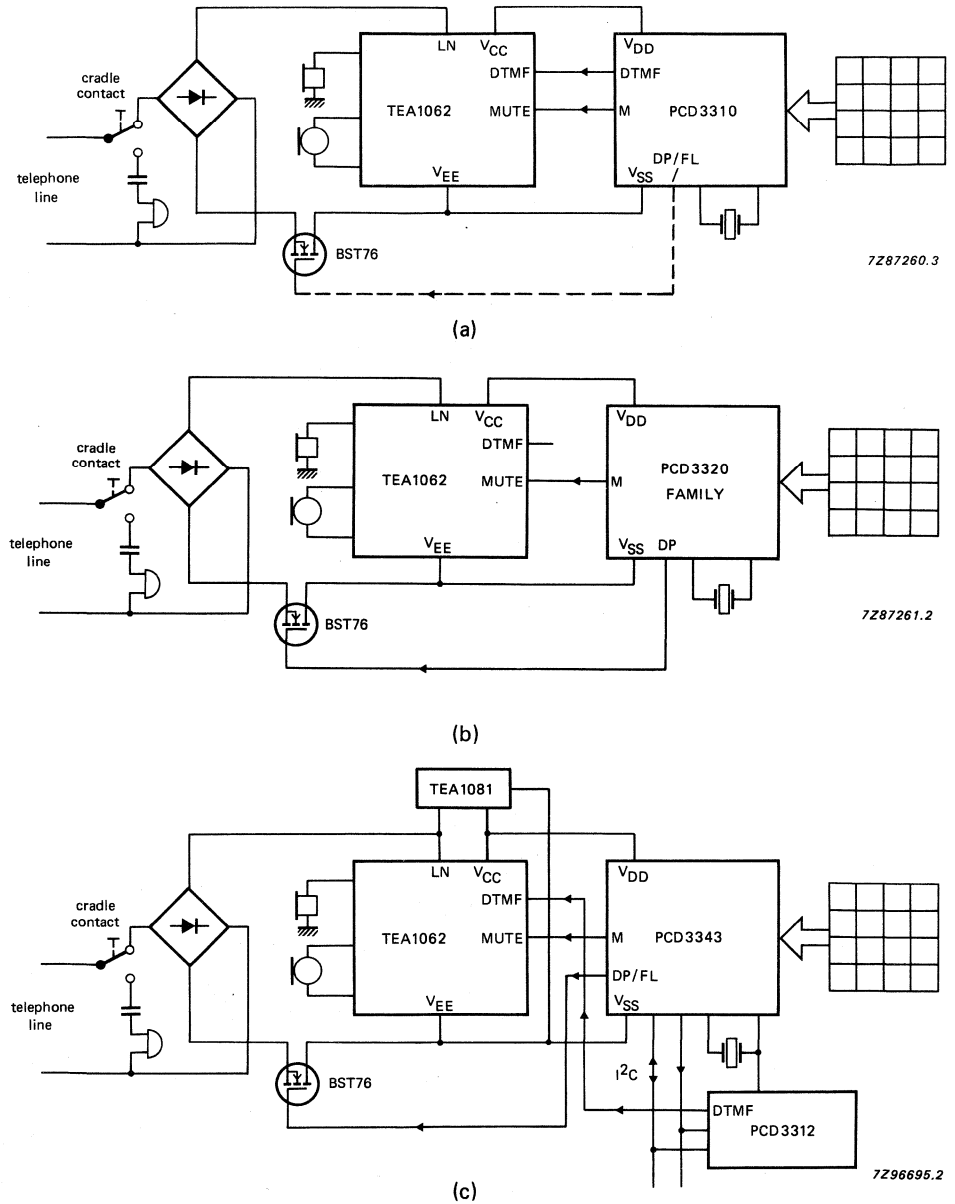


Fig.16 Typical applications of the TEA1062 (simplified).

(a) DTMF-Pulse set with CMOS-bilingual dialling circuit PCD3310. The dashed lines show an optional flash (register recall by timed loop break).
(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.
(c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS controller and the PCD3312 CMOS DTMF generator with I^2C-bus. Supply is provided by the TEA1081 supply circuit.

LOW VOLTAGE VERSATILE TELEPHONE TRANSMISSION CIRCUIT WITH DIALLER INTERFACE AND TRANSMIT LEVEL DYNAMIC LIMITING

GENERAL DESCRIPTION

The TEA1063 is a bipolar integrated circuit that performs all the speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech and has a powerful DC supply for peripheral circuits. The IC operates at line voltages down to 1.6 V DC (with reduced performance) to facilitate the use of more telephone sets connected in parallel. The transmit signal on the line is dynamically limited (speech-controlled) to prevent distortion at high transmit levels of both the sending signal and the sidetone.

Features

- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with low voltage drop and adjustable static resistance
- DC line voltage adjustment facility
- Provides a supply for external circuits in two options:
  unregulated supply, regulated line voltage;
  stabilized supply, line voltage varies with supply current
- Dynamic limiting (speech-controlled) in transmit direction prevents distortion of line signal and sidetone
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphones
- DTMF signal input
- Confidence tone in the earpiece during DTMF dialling
- Mute input for disabling speech during pulse or DTMF dialling
- Power-down input for improved performance during pulse dial or register recall (flash)
- Receiving amplifier for magnetic, dynamic or piezo-electric earpieces
- Large amplification setting ranges on microphone and earpiece amplifiers
- Line loss compensation (line current dependent) for microphone and earpiece amplifiers (not used for DTMF amplifier)
- Gain control curve adaptable to exchange supply
- Automatic disabling of the DTMF amplifier in extremely-low voltage conditions

PACKAGE OUTLINES

TEA1063 : 20-lead DIL; plastic (SOT146).
TEA1063T: 20-lead mini-pack; plastic (SO20; SOT163A).

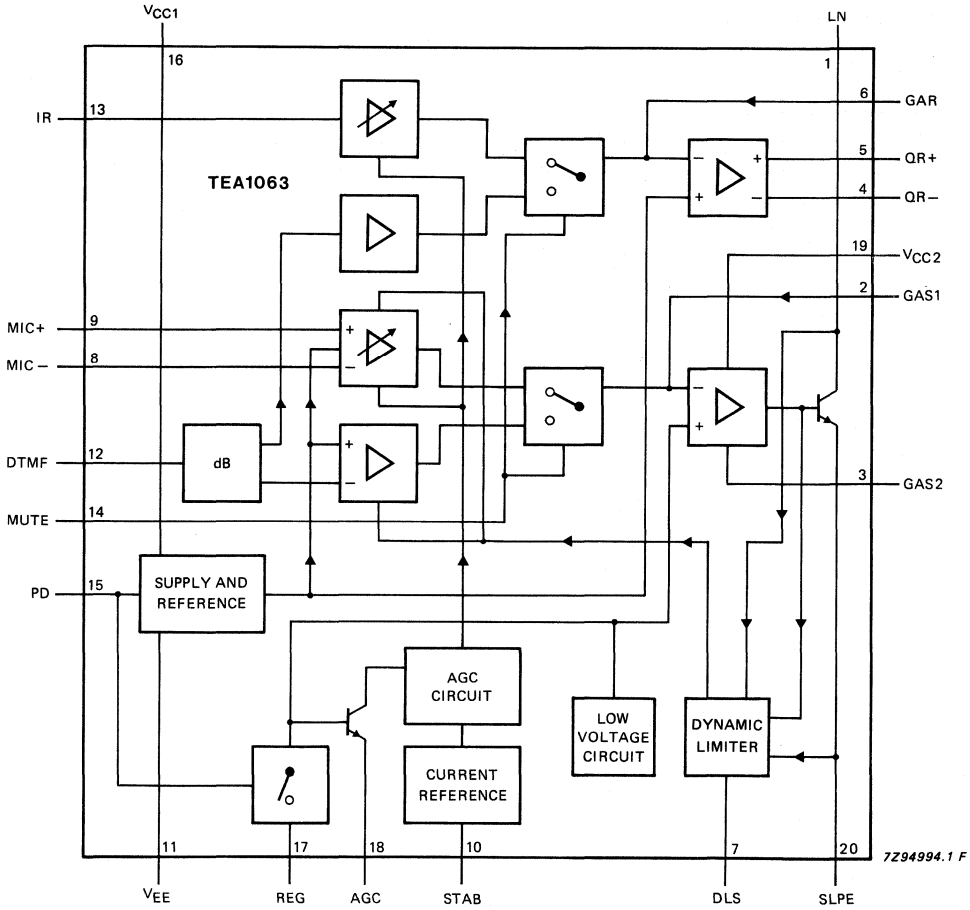


Fig. 1 Block diagram.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Operating ambient temperature range		T_{amb}	−25	–	+75	°C
Line current operating range:						
normal operation		I_{line}	11	–	140*	mA
with reduced performance		I_{line}	2	–	11	mA
Internal supply current:						
power-down input LOW	V_{CC1} = 3.1 V	I_{CC1}	–	1.35	–	mA
power-down input HIGH	V_{CC1} = 3.1 V	I_{CC1}	–	60	–	μA
Voltage gain range:						
microphone amplifier		G_v	47	–	55	dB
receiving amplifier	Single ended	G_v	23	–	42	dB
	Differential	G_v	29	–	48	dB
Line loss compensation:						
gain control range		G_v	–	8.6	–	dB
exchange supply voltage range		V_{exch}	36	–	60	V
exchange feeding bridge resistance range		R_{exch}	400	–	1000	Ω
Maximum output voltage swing on LN (peak-to-peak value)	R15 + R16 = 448 Ω					
	I_{line} = 15 mA					
	I_P = 2 mA	$V_{LN(p-p)}$	–	4.1	–	V
	I_P = 4 mA	$V_{LN(p-p)}$	–	3.25	–	V
Regulated line voltage application						
	R15 = 0 Ω; R16 = 392 Ω					
Supply for peripherals	I_{line} = 15 mA					
	I_P = 1.65 mA	V_p	2.7	–	–	V
	I_P = 1.8 mA; $R_{REG-SLPE}$ = 68.1 kΩ	V_p	3.0	–	–	V
DC line voltage	I_{line} = 15 mA					
	without $R_{REG-SLPE}$	V_{LN}	–	4.0	–	V
	$R_{REG-SLPE}$ = 68.1 kΩ	V_{LN}	–	4.3	–	V
Stabilized supply voltage application						
	R15 = 392 Ω; R16 = 56 Ω					
Supply for peripherals	I_{line} = 15 mA					
	I_P = 0 to 4 mA	$V_{CC2-SLPE}$	3.35	3.6	3.85	V
DC line voltage	I_{line} = 15 mA					
	I_P = 2 mA	V_{LN}	–	4.8	–	V
	I_P = 4 mA	V_{LN}	–	5.5	–	V

* For TEA1063T the maximum line current depends on the heat dissipating qualities of the mounted device.

PINNING

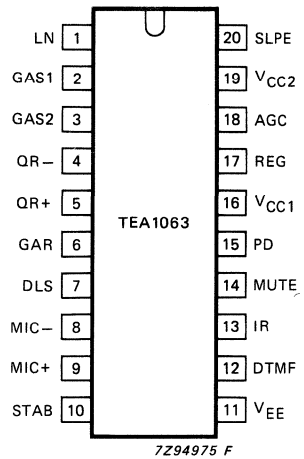


Fig. 2 Pinning diagram.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	DLS	decoupling for transmit amplifier dynamic limiter
8	MIC–	inverting microphone input
9	MIC+	non-inverting microphone input
10	STAB	current stabilizer
11	V_{EE}	negative line terminal
12	DTMF	dual-tone multi-frequency input
13	IR	receiving amplifier input
14	MUTE	mute input
15	PD	power-down input
16	V_{CC1}	internal supply decoupling
17	REG	voltage regulator decoupling
18	AGC	automatic gain control input
19	V_{CC2}	reference voltage with respect to SLPE
20	SLPE	slope adjustment for DC curve/reference for peripheral circuits

FUNCTIONAL DESCRIPTION

Supplies V_{CC1}, V_{CC2}, LN, SLPE, REG and STAB (Fig. 3)

Power for the TEA1063 and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply voltage at V_{CC1} and regulates its voltage drop. The internal supply requires a decoupling capacitor between V_{CC1} and V_{EE}. The internal current stabilizer is set by a 3.6 kΩ resistor between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the subscriber line DC resistance R_{line} and the DC voltage (including polarity guard) on the subscriber set (see Fig. 3).

The internal voltage regulator generates a temperature-compensated reference voltage that is available between V_{CC2} and SLPE [$V_{ref} = V_{CC2\text{-}SLPE}$ = 3.6 V (typ.)]. This internal voltage regulator requires decoupling by a capacitor between REG and V_{EE} (C3).

The reference voltage can be used to:

- regulate directly the line voltage (stabilized $V_{LN\text{-}SLPE} = V_{CC2\text{-}SLPE}$)
- to stabilize the supply voltage for peripherals.

Regulated line voltage

In this application the V_{CC2} pin is connected to the LN pin as shown in Fig. 3. This configuration gives a stabilized voltage across pins LN and SLPE which, applied via the low-pass filter R16, C15, provides a supply to the peripherals that is independent of the line current and depends only on the peripheral supply current.

The value of R16 and the level of the DC voltage $V_{LN\text{-}SLPE}$ determine the supply capabilities. In the basic application R16 = 392 Ω and C15 = 220 μF. The worst-case peripheral supply current as a function of supply voltage is shown in Fig. 4. To increase the supply capabilities, the DC voltage $V_{LN\text{-}SLPE}$ can be increased by using $R_{VA(REG\text{-}SLPE)}$ or by decreasing the value of R16.

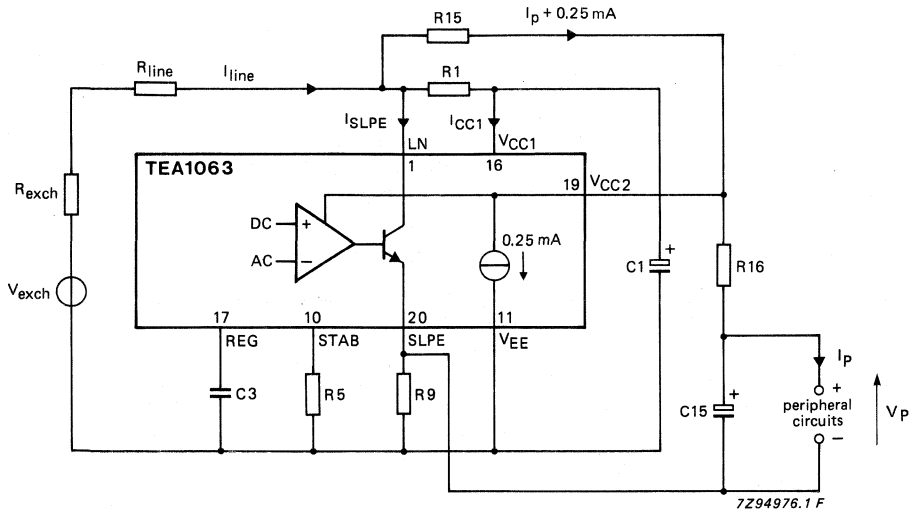


Fig. 3 Application with regulated line voltage (stabilized $V_{LN-SLPE}$). The voltage $V_{LN-SLPE}$ is fixed to V_{ref} = 3.6 ± 0.25 V. Resistor R16 together with the line current determine the supply capabilities and the maximum output swing on the line (no loop damping is necessary). The line voltage V_{LN} = V_{ref} + ([I_{line} − I_{CC1} − 0.25 mA] x R9).

DEVELOPMENT DATA

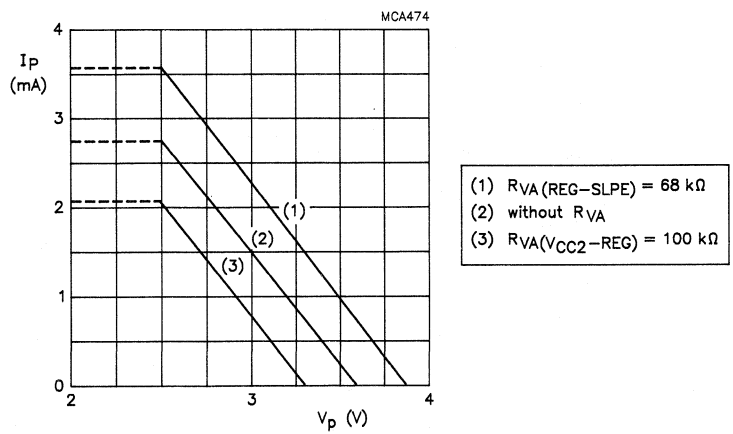


Fig. 4 Minimum supply current for peripherals (I_P) as a function of the peripheral supply voltage (V_P): I_{line} = 15 mA; R16 = 392 Ω; R15 = 0 Ω; valid for MUTE = 0 and 1. Line current has very little influence.

FUNCTIONAL DESCRIPTION (continued)

Regulated line voltage (continued)

The maximum AC output swing on the line at low line currents is influenced by R16 (limited by current) and the maximum output swing on the line at high line currents is influenced by the DC voltage $V_{LN\text{-}SLPE}$ (limited by voltage). In both these situations, the internal dynamic limiter in the sending channel prevents distortion when the microphone input is overdriven. The maximum AC output swing on LN is shown in Fig. 5; practical values for R16 are from 200 to 600 Ω and this influences both the maximum output swing at low line currents and the supply capabilities.

The SLPE pin is the ground reference for peripheral circuits, therefore inputs MUTE, PD and DTMF are also referenced to SLPE.

Active microphones can be supplied between V_{CC1} and V_{EE}. Low-power circuits that provide only MUTE and/or PD inputs to the TEA1063 also can be powered from V_{CC1}. However V_{CC1} cannot be used for circuits that provide DTMF signals to the TEA1063 because V_{CC1} is referred to ground.

If the line current I_{line} exceeds I_{CC1} + 0.25 mA, the voltage converter shunts the excess current to SLPE via LN; where $I_{CC1} \approx 1.35$ mA, the value required by the IC for normal operation.

The DC line voltage on LN is:

$$V_{LN} = V_{LN\text{-}SLPE} + (I_{SLPE} \times R9)$$

$$V_{LN} = V_{ref} + ([I_{line} - I_{CC1} - 0.25 \times 10^{-3}] \times R9)$$

in which

V_{ref} = 3.6 V ± 0.25 V is the internal reference voltage between V_{CC2} and SLPE; its value can be adjusted by external resistor R_{VA}

R9 = external resistor between SLPE and V_{EE} (20 Ω in basic application).

With R9 = 20 Ω, this results in:

V_{LN} = 3.85 ± 0.25 V at I_{line} = 15 mA

V_{LN} = 4.15 ± 0.3 V at I_{line} = 15 mA, $R_{VA(REG\text{-}SLPE)}$ = 68.1 kΩ

V_{LN} = 3.55 ± 0.3 V at I_{line} = 15 mA, $R_{VA(V_{CC2} - REG)}$ = 100 kΩ;

The preferred value for R9 is 20 Ω. Changing R9 influences microphone gain, DTMF gain, the gain control characteristics, sidetone, and the DC characteristics (especially the low voltage characteristics).

In normal conditions, $I_{SLPE} \gg (I_{CC1} + 0.25\ mA)$ and the static behaviour is equivalent to a voltage regulator diode with an internal resistance of R9. In the audio frequency range the dynamic impedance is determined mainly by R1. The equivalent impedance of the circuit in the audio frequency range is shown in Fig. 6.

The internal reference voltage $V_{CC2\text{-}SLPE}$ can be increased by external resistor $R_{VA(REG\text{-}SLPE)}$ connected between REG and SLPE or decreased by external resistor $R_{VA(V_{CC2} - REG)}$ connected between V_{CC2} and REG. The supply voltage $V_{CC2\text{-}SLPE}$ is shown as a function of R_{VA} in Fig.7. Changing the reference voltage influences the output swing of both sending and receiving amplifiers.

At line currents below 10 mA (typ.), the DC voltage dropped across the circuit is adjusted to a lower level automatically (approximately 1.6 V at 2 mA). This gives the possibility of operating more telephone sets in parallel with DC line voltages (excluding polarity guard) down to an absolute minimum of 1.6 V. At line currents below 10 mA (typ.), the circuit has limited sending and receiving levels.

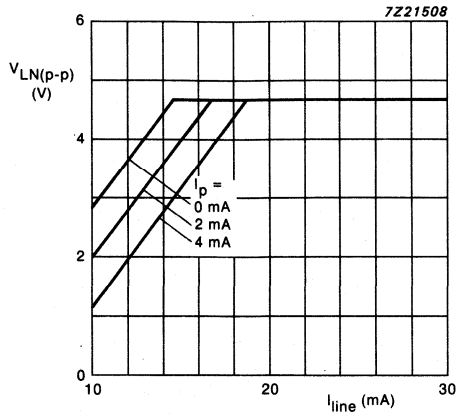


Fig. 5 Maximum AC output swing on the line as a function of line current with peripheral supply current as a parameter: R15 = 0 Ω; R16 = 392 Ω.

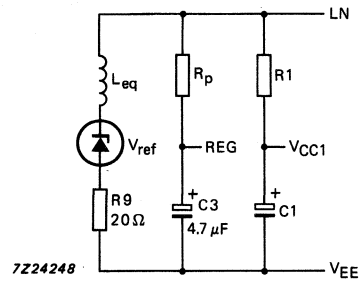


Fig. 6 Equivalent impedance between LN and V_{EE} in the application with stabilized $V_{LN-SLPE}$:
R15 = 0 Ω
L_{eq} = C3 x R9 x R_P
R_P = 15 kΩ.

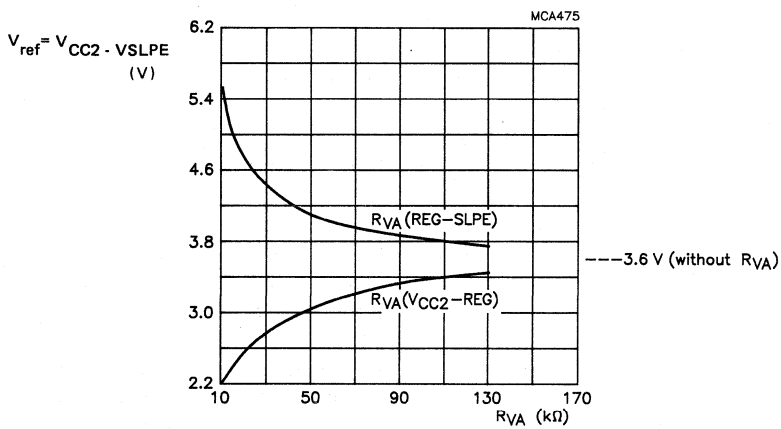


Fig. 7 Internal reference voltage $V_{CC2-SLPE}$ as a function of resistor $R_{VA(REG-SLPE)}$ for line currents between 11 and 140 mA.

In the stabilized peripheral supply voltage application;

$$V_{LN} = V_{CC2-SLPE} + ([I_P + 0.25 \times 10^{-3}] \times R15) + ([I_{line} - I_{CC1} - 0.25\ mA] \times R9)\ V$$

In the regulated line voltage application (R15 = 0 Ω) ;

$$V_{LN} = V_{CC2-SLPE} + ([I_{line} - I_{CC1} - 0.25\ mA] \times R9)\ V$$

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Stabilized peripheral supply voltage

The configuration shown in Fig. 8 provides a stabilized voltage across pins V_{CC2} and SPLE for peripheral circuits (such as dialling and control circuits); the DC voltage V_{LN} now varies with the peripheral supply current.

The $V_{CC2-SLPE}$ supply must be decoupled by capacitor C15. For stable loop operation, resistor R16 ($\approx 50\ \Omega$) is connected between V_{CC2} and SLPE in series with C15. The voltage regulator control loop is completed by resistor R15 between LN and V_{CC2}.

For sets with an impedance of 600 Ω, practical values are: R15 = 200 to 600 Ω; C15 = 220 μF; C3 = 470 nF. The ratio $R15/R16 \leqslant 8$ is for stable loop operation with sufficient phase margin, and $R15/R16 \geqslant 6$ is for satisfactory set impedance in the audio frequency range.

For sets with complex impedance, the value of C3 and the ratio R15/R16 are different.

The peripheral supply capability depends mainly on the available line current, the required AC output swing on the line, the maximum permitted DC voltage on the line and the values of external components (especially R15). With R15 = 392 Ω and R16 = 56 Ω (basic application) the maximum possible AC output swing on the line as a function of line current is as shown in Fig. 9, the curve parameter is the peripheral supply current (Ip). Different values for R15 (from 200 to 600 Ω) maintaining $6 < R15/R16 < 8$ give different results.

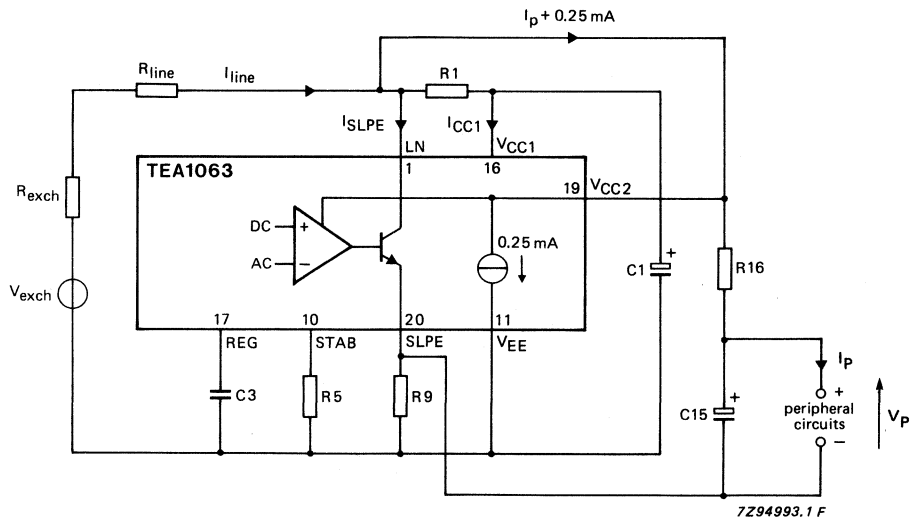


Fig. 8 Application with stabilized supply voltage for peripheral circuits: R15 = 392 Ω; R16 = 56 Ω.

The DC line voltage on LN is

$$V_{LN} = V_{LN\text{-}SLPE} + (I_{SLPE} \times R9).$$

Therefore

$$V_{LN} = V_{ref} + ([I_p + 0.25 \times 10^{-3}] \times R15) + ([I_{line} - I_{CC1} - 0.25 \times 10^{-3}] \times R9)$$

in which:

V_{ref} is the internal reference voltage between V_{CC2} and SLPE (the value of V_{ref} can be adjusted by an external resistor, R_{VA}). V_{ref} = 3.6 V (typ.) without R_{VA}

I_p is the supply current used by peripheral circuits

R15 is an external resistor between LN and V_{CC2} (392 Ω in the basic application)

R9 is an external resistor between SLPE and V_{EE} (20 Ω in the basic application)

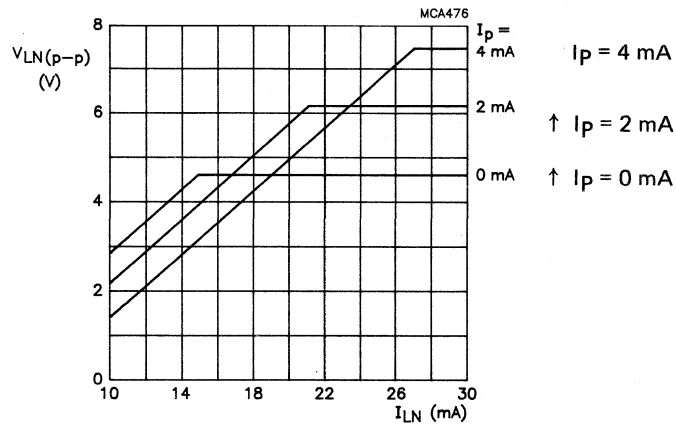


Fig. 9 Maximum output swing on line as a function of line current with the peripheral supply current as a parameter; R15 = 392 Ω; R16 = 56 Ω. As different values of R15 and R16 are allowed, different curves would then apply.

The DC voltage $V_{LN\text{-}SLPE}$ as a function of I_P with R15 as a parameter is shown in Fig. 10. In the audio frequency range, the dynamic impedance is determined mainly by R1. The equivalent impedance in the audio range of the circuit (Fig. 8) is shown in Fig. 11.

FUNCTIONAL DESCRIPTION (continued)

Stabilized peripheral supply voltage (continued)

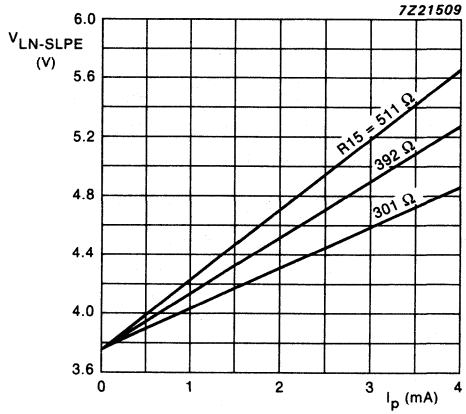
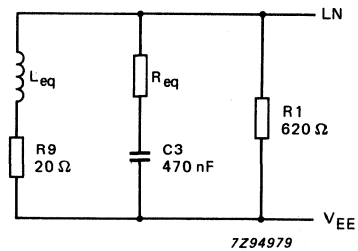


Fig. 10 Curves showing the typical voltage drop between LN and SLPE as a function of the supply current for peripherals with R15 as a parameter: $V_{CC2-SLPE}$ = 3.6 V (R_{VA} not connected). $V_{CC2-SLPE}$ can be adjusted between approximately 2.6 and 5 V by changing the value of R_{VA}, this results in a parallel-shift of the curves.
The total voltage drop $V_{LN} \approx V_{LN-SLPE} + ([I_{line} - I_{CC1} - 0.25\ mA] \times R9)$



$$R_{eq} = R_P \left(\frac{R15}{R16} + 1\right)$$

$$L_{eq} = C3 \times R9 \times R_{eq}$$
with R_P = 15 kΩ

Fig. 11 Equivalent impedance between LN and V_{EE} at f > 300 Hz in the application with stabilized supply voltage for peripheral circuits.

Microphone inputs MIC+ and MIC− and gain pins GAS1 and GAS2

The TEA1063 has symmetrical microphone inputs, its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage amplification is typ. 55 dB with R7 = 68 kΩ. Either dynamic, magnetic or piezo-electric microphones can be used, or an electret microphone with a built-in FET buffer. Arrangements for the microphone types are shown in Fig. 12.

The gain of the microphone amplifier is proportional to external resistor R7 connected between GAS1 and GAS2 and with this it can be adjusted between 47 dB and 55 dB to suit the sensitivity of the transducer.

An external 100 pF capacitor (C6) is required between GAS1 and SLPE to ensure stability. A larger value of C6 may be chosen to obtain a first-order low-pass filter with a cut-off frequency corresponding to the time constant R7 x C6.

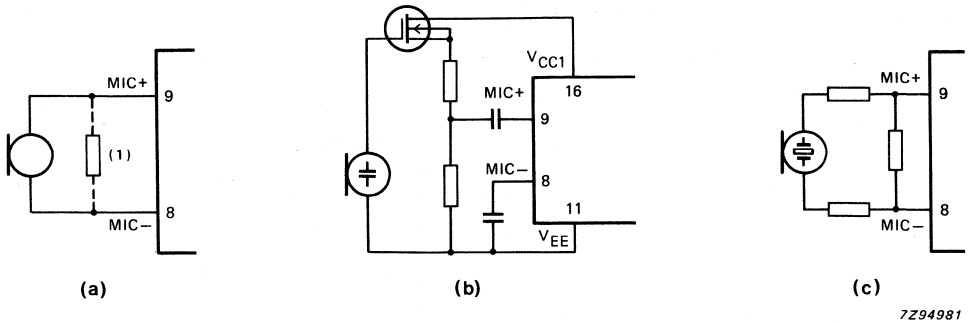


Fig. 12 Microphone arrangements: a) magnetic or dynamic microphone, the resistor (1) may be connected to reduce the terminating impedance, or for sensitive types a resistive attenuator can be used to prevent overloading the microphone inputs; b) electret microphone; c) piezo-electric microphone.

Dynamic limiter (sending) pin DLS

To prevent distortion of the transmitted signal, the gain of the microphone amplifier is reduced rapidly when peaks of the signal on the line exceed an internally-determined threshold. The time in which gain reduction is effected (attack time) is very short. The circuit stays in the gain-reduced condition until the peaks of the sending signal remain below the threshold level. The microphone gain then returns to normal after a time determined by the capacitor connected to DLS (release time).

The internal threshold adapts automatically to the DC voltage setting of the circuit (voltage $V_{LN-SLPE}$). This means that the maximum output swing on the line will be higher if the DC voltage dropped across the circuit is increased.

Fig. 13 shows the maximum possible output swing on the line as a function of the DC voltage drop ($V_{LN-SLPE}$) with $I_{line} - I_P$ as a parameter.

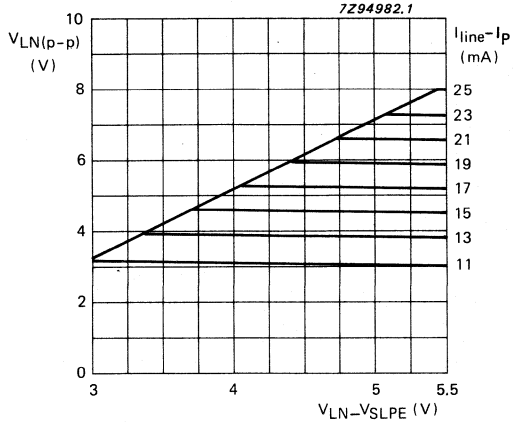


Fig. 13 Maximum output swing on line as a function of the DC voltage drop $V_{LN-SLPE}$ with $I_{line} - I_P$ as a parameter: R15 = 392 Ω; R16 = 56 Ω; or R15 = 0 Ω and R16 = 392 + 56 = 448 Ω.

The internal threshold level is lowered automatically if the DC current in the transmit output stage is insufficient. This prevents distortion of the sending signal in applications using parallel-connected telephones or telephones operating over long lines, for example.

Dynamic limiting also considerably improves sidetone performance in over-drive conditions (less distortion; limited sidetone level).

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Receiving amplifier IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, QR+ (non-inverting) and QR− (inverting). These outputs may be used for single-ended or differential drive, depending on the type and sensitivity of the earpiece used (see Fig. 14). Gain from IR to QR+ is typically 34 dB with R4 = 100 kΩ, sufficient for low-impedance magnetic or dynamic earpieces which are suitable for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB. Differential drive can be used when the earpiece impedance exceeds 450 Ω as with high-impedance dynamic, magnetic or piezo-electric earpieces.

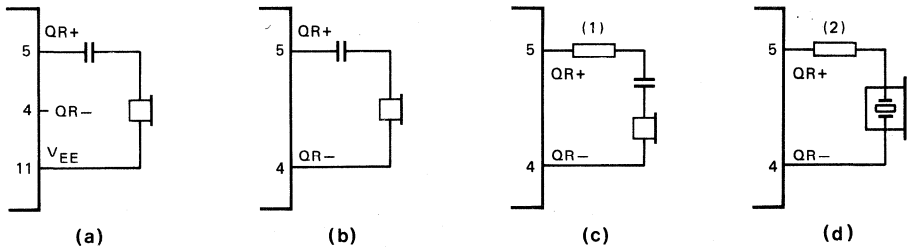


Fig. 14 Alternative receiver arrangements: a) dynamic earpiece with an impedance less than 450 Ω; b) dynamic earpiece with an impedance more than 450 Ω; c) magnetic earpiece with an impedance more than 450 Ω, resistor (1) may be connected to prevent distortion (inductive load); d) piezo-electric earpiece, resistor (2) is required to increase the phase margin (stability with capacitive load).

The output voltage of the receiving amplifier is specified for continuous-wave drive. Fig. 15 shows the maximum output swing of the receiving amplifier as a function of the DC voltage drop (V_{LN}). The maximum output voltage will be higher under speech conditions, where the ratio of the peak to the RMS value is higher.

The gain of the receiving amplifier can be adjusted to suit the sensitivity of the transducer used. The adjustment range is between 23 dB and 42 dB with single-ended drive and between 29 dB and 48 dB with differential drive. The gain is proportional to the external resistor R4 connected between GAR and QR+. The overall gain between LN and QR+ can be found by subtracting the attenuation of the anti-sidetone network (32 dB) from the amplifier gain.

Two external capacitors (C4 = 100 pF and C7 = 10 x C4 = 1 nF) ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R4 x C4. The relationship C7 = 10 x C4 must be maintained.

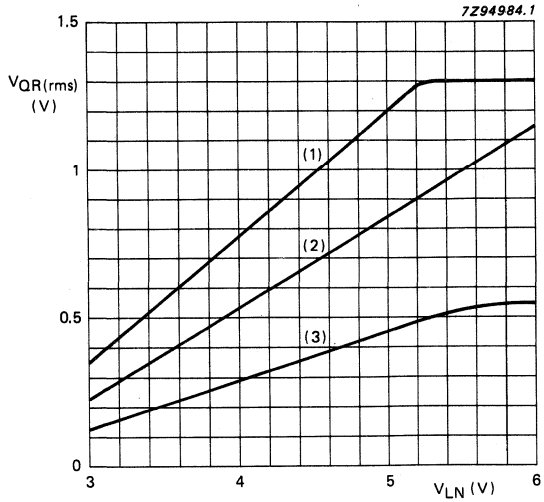


Fig. 15 Maximum output swing of the receiving amplifier as a function of DC voltage drop V_{LN} with the load at the receiver output as parameter:
valid for both supply options;
THD = 2%; I_{line} = 15 mA.
Curve (1) is for a differential load of 47 nF (series resistance = 100 Ω); f = 3400 Hz.
Curve (2) is for a differential load of 450 Ω; f = 1 kHz.
Curve (3) is for a single-ended load of 150 Ω; f = 1 kHz.

Automatic gain control input AGC

Automatic compensation of line loss is obtained by connecting a resistor (R6) between AGC and V_{EE}. This automatic gain control varies the gain of the microphone amplifier and receiving amplifier in accordance with the DC line current. The control range is 9 dB; this corresponds to a 5 km line of 0.4 mm diameter copper twisted-pair cable (DC resistance = 280 Ω/km, average attenuation = 1.8 dB/km). The DTMF gain is not affected by this feature.

The value of R6 must be chosen with reference to the exchange supply voltage and its feeding bridge resistance (see Fig. 16 and Table 1). Different values of R6 give the same line current ratios at the start and the end of the control range. If automatic line-loss compensation is not required the AGC pin can be left open, the amplifiers then give their maximum adjusted gain.

DEVELOPMENT DATA

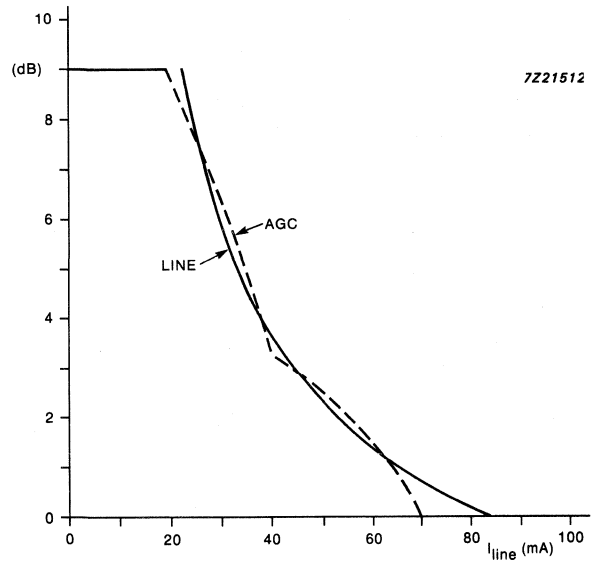


Fig. 16 Variation of amplification as a function of line current with R6 as a parameter; R9 = 20 Ω.

* Value to be fixed.

FUNCTIONAL DESCRIPTION (continued)

Automatic gain control input AGC (continued)

Table 1 Values of R6 giving optimum line-loss compensation at various values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

		R_{exch} (Ω)				
		400	500	600	800	1000
		R6 (kΩ)				
V_{exch} (V)	36	41.2 K	37.5 K	32.4 K	X	X
	48	56.2 K	51 kΩ	47.5 K	40.2 K	X
	60	X	X	59 K	52.3 K	46.4 K

MUTE input (see notes 1 and 2)

MUTE = HIGH enables the DTMF input and inhibits the microphone and receiving amplifier inputs.

MUTE = LOW or open-circuit disables the DTMF input and enables the microphone and receiving amplifier inputs.

Switching MUTE gives negligible clicks at the telephone outputs and on the line.

The MUTE function is operational down to V_{LN} = 2.8 V (V_{CC1} = 2.1 V). It is not possible to enable the DTMF amplifier for $V_{LN} < 2.8$ V, in this way the optimum performance of the speech amplifiers is guaranteed under extremely low voltage conditions (parallel operation). The speech amplifiers can be disabled by means of the MUTE function down to V_{LN} = 1.6 V.

Dual-tone multi-frequency input DTMF (see note 1)

When the DTMF input is enabled, dialling tones may be sent on to the line. The voltage gain between DTMF-SLPE and LN-V_{EE} is typ. 29 dB less than the gain of the microphone amplifier and varies with R7 in the same way as the gain of the microphone amplifier. This means that the tone level at the DTMF input has to be adjusted after setting the gain of the microphone amplifier.
With R7 = 68 kΩ the gain is typically 26 dB.

The signalling tones can be heard in the earpiece at a low level (confidence tone).

Power-down input PD (see notes 1 and 2)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted; as a consequence it provides no supply for the transmission circuit connected to V_{CC1} or for the peripherals between V_{CC2} and SLPE.
These supply gaps are bridged by the charges in the capacitors C1 and C15. The requirements on these capacitors are eased by applying a HIGH level to the PD input during the time of the loop break. This reduces the internal supply current I_{CC1} from (typ.) 1.3 mA to (typ.) 60 μA and switches off the voltage regulator to prevent discharge via LN and V_{CC2}.

A HIGH level at PD also internally disconnects the capacitor at REG so that the voltage stabilizer has no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall.

When the power-down facility is not required, the PD pin can be left open-circuit or connected to SLPE.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-sidetone network comprising $R1//Z_{line}$, R2, R3, R8, R9 and Z_{bal} (see Fig. 17). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9 \times R2 = R1 \times (R3 + [R8//Z_{bal}])$

b) $(Z_{bal}/[Z_{bal} + R8]) = (Z_{line}/[Z_{line} + R1])$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) is always fulfilled provided $|R8//Z_{bal}| \ll R3$.

To obtain optimum sidetone suppression, condition b) has to be fulfilled, resulting in:

$$Z_{bal} = (R8/R1) \times Z_{line} = k \times Z_{line}$$

where k is a scale factor; $k = (R8/R1)$.

The scale factor k (value of R8) is chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal};
- $|Z_{bal}//R8| \ll R3$ to fulfill condition a) and thus ensure correct anti-sidetone bridge operation;
- $|Z_{bal} + R8| \gg R9$ to avoid influencing the transmit gain.

In practice Z_{line} varies considerably with the line length and line type. Therefore the value chosen for Z_{bal} should be for an average line length giving satisfactory sidetone suppression with short and long lines. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

Example

The line impedance for which optimum suppression is to be obtained can be represented by 210 Ω + (1265 Ω // 140 nF). This represents a 5 km line of 0.5 mm diameter copper twisted-pair cable matched with 600 Ω (176 Ω/km; 38 nF/km).

With k = 0.64 this results in: R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω // 220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig. 17 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range.

Alternatively a conventional Wheatstone bridge can be used as an anti-sidetone circuit (Fig. 18). Both bridge types can be used with either resistive or complex set impedances. (More information on the balancing of anti-sidetone bridges can be obtained in our publication 'Versatile speech transmission ICs for electronic telephone sets', order number 9398 341 10011.)

Notes

1. The reference used for the MUTE, DTMF and PD inputs is SLPE.
2. A LOW level for any of these pins is defined by connection to SLPE, a HIGH level is defined as a voltage greater than V_{SLPE} + 1.5 V and smaller than V_{CC1} + 0.4 V.

Side-tone suppression (continued)

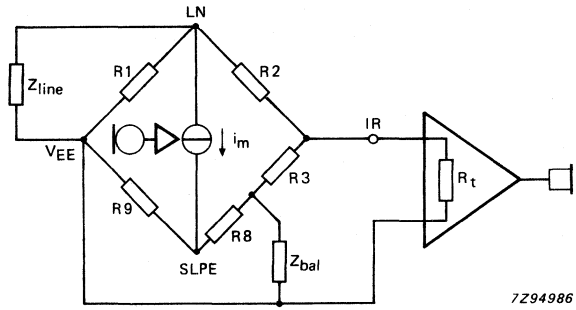


Fig. 17 Equivalent circuit of TEA1060 family anti-side-tone bridge.

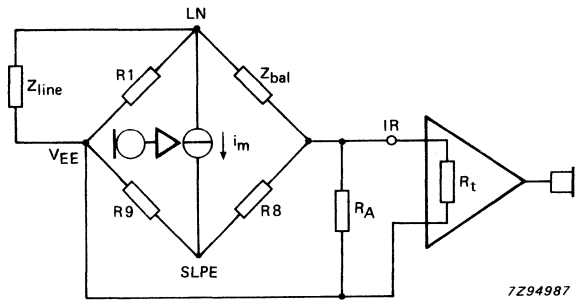


Fig. 18 Equivalent circuit of an anti-sidetone network in the Wheatstone bridge configuration.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive line voltage continuous		V_{LN}	–	12	V
Repetitive line voltage during switch-on or line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage; one 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω (Fig. 23)	V_{LN}	–	28	V
Line current TEA1063 (1)		I_{line}	–	140	mA
Line current TEA1063T (1)		I_{line}	–	140	mA
Input voltage on pins other than LN and V_{CC2}		V_i	$V_{EE}-0.7$	$V_{CC1}+0.7$	V
Total power dissipation (2)	R_9 = 20 Ω				
TEA1063		P_{tot}	–	715	mW
TEA1063T		P_{tot}	–	550	mW
Storage temperature range		T_{stg}	−40	+125	°C
Operating ambient temperature range		T_{amb}	−25	+75	°C
Junction temperature		T_j	–	+125	°C

1. The value depends mostly on the maximum required T_{amb} and on the voltage between LN and SLPE (see Figs 19 and 20) to determine the current as a function of the required voltage and temperature.
2. Calculated for maximum T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

From junction to ambient in free air

TEA1063	$R_{th\ j\text{-}a}$	typ.	70	K/W
TEA1063T mounted on glass epoxy boards 41 x 19 x 1.5 mm	$R_{th\ j\text{-}a}$	typ.	90	K/W

DEVELOPMENT DATA

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; R_l = 600 Ω; tested in the circuit of Fig. 21 or 22); unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies LN, V_{CC1}, V_{CC2} (pins 1, 16, 19)						
Reference DC voltage between V_{CC2} and SLPE	I_{line} = 15 mA I_P = 0; 4 mA					
R_{VA} not connected		$V_{CC2-SLPE}$	3.35	3.6	3.85	V
Variation with temperature	I_{line} = 15 mA	$\frac{\Delta V_{CC2-SLPE}}{\Delta T}$	−2	−1	1	mV/K
Variation with line current referred to 15 mA	I_{line} = 100 mA	$\Delta V_{CC2-SLPE}$	−	40	−	mV
With R_{VA} connected						
between REG and SLPE	R_{VA} = 68.1 kΩ	$V_{CC2-SLPE}$	3.6	3.9	4.2	V
between REG and LN	R_{VA} = 100 kΩ	$V_{CC2-SLPE}$	3.0	3.3	3.6	V
DC line voltage:						
voltage drop between LN and V_{EE}	MIC−, MIC+ inputs open; R15 = 392 Ω; without R_{VA}					
at I_{line} = 15 mA	I_P = 0 mA	V_{LN}	3.7	4.0	4.3	V
	I_P = 2 mA	V_{LN}	4.5	4.8	5.1	V
	I_P = 4 mA	V_{LN}	5.2	5.5	5.8	V
at I_{line} = 100 mA	I_P = 2 mA	V_{LN}	−	6.5	7.1	V
at I_{line} = 140 mA	I_P = 2 mA	V_{LN}	−	7.25	8.1	V
Voltage drop under low current conditions	I_P = 0 mA					
	I_{line} = 2 mA	V_{LN}	−	1.8	−	V
	I_{line} = 4 mA	V_{LN}	1.8	2.1	2.4	V
	I_{line} = 7 mA	V_{LN}	2.5	2.8	3.1	V
	I_{line} = 11 mA	V_{LN}	3.6	3.9	4.2	V
Internal supply current I_{CC1}:						
current into pin V_{CC1}	V_{CC1} = 3.1 V					
	PD = LOW	I_{CC1}	−	1.35	1.65	mA
	PD = HIGH	I_{CC1}	−	60	90	μA
Microphone inputs MIC−, MIC+ (pins 8, 9)						
Input impedance:						
differential		Z_i	51	64	77	kΩ
single-ended		Z_i	25.5	32.0	38.5	kΩ

parameter	conditions	symbol	min.	typ.	max.	unit
Common mode rejection ratio		CMRR	–	82	–	dB
Voltage gain (see Fig. 21)	I_{line} = 15 mA; R7 = 68 kΩ	G_v	54	55	56	dB
Variation of G_v with frequency, referred to 0.8 kHz	f = 300 and 3400 Hz	ΔG_{vf}	−0.5	±0.15	+0.5	dB
Variation of G_v with temperature, referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 and +75 °C	ΔG_{vT}	–	±0.2	–	dB
DTMF input (pin 12)						
Input impedance		Z_i	16.1	20.0	23.9	kΩ
Voltage gain (see Fig. 21)	I_{line} = 15 mA; R7 = 68 kΩ	G_v	25	26	27	dB
Variation of G_v with frequency, referred to 0.8 kHz	f = 300 and 3400 Hz	ΔG_{vf}	−0.5	±0.1	+0.5	dB
	f = 697 and 1633 Hz	ΔG_{vf}	−0.2	±0.05	+0.2	dB
Variation of G_v with temperature, referred to 25 °C	I_{line} = 50 mA; T_{amb} = −25 and +75 °C	ΔG_{vT}	–	±0.2	–	dB
Gain adjustment inputs GAS1, GAS2 (pins 2, 3)						
Transmitting amplifier, gain adjustment range		ΔG_v	−8	–	+0	dB
Sending amplifier output LN (pin 1)						
Dynamic limiter						
Output voltage swing (peak-to-peak value)	I_{line} = 15 mA; R7 = 68 kΩ; I_P = 0 mA; $V_{i(rms)}$ = 2.9 mV	$V_{LN(p-p)}$	4.15	4.55	4.95	V
Total harmonic distortion	V_i = 2.9 mV + 10 dB	THD	–	1.0	2.0	%
	V_i = 2.9 mV + 15 dB	THD	–	2.5	10.0	%
Output voltage swing (peak-to-peak value)	V_i = 2.9 mV + 10 dB					
	I_P = 2 mA	$V_{LN(p-p)}$	3.7	3.95	4.25	V
	I_P = 4 mA	$V_{LN(p-p)}$	3.0	3.25	3.5	V
	I_P = 0 mA; I_{line} = 7 mA	$V_{LN(p-p)}$	–	2.0	–	V
	I_P = 0 mA; I_{line} = 5 mA	$V_{LN(p-p)}$	–	1.45	–	V

DEVELOPMENT DATA

CHARACTERISTICS (continued)

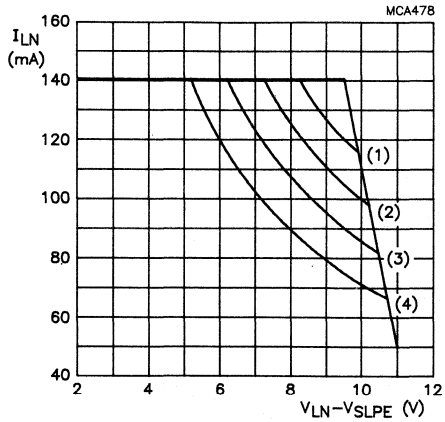
parameter	conditions	symbol	min.	typ.	max.	unit
LN output (continued)						
Dynamic behaviour of limiter	C16 = 470 nF					
attack time, V_{mic} jumps from 2 mV to 40 mV		t_{att}	–	1.5	5.0	ms
release time, V_{mic} falls from 40 mV to 2 mV		t_{rel}	50	150	–	ms
Noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	–70	–	dBmp
Receiving amplifier input IR (pin 13)						
Input impedance		Z_i	16	20	24	kΩ
Receiving amplifier outputs QR– QR+ (pins 4, 5)						
Output impedance	single-ended	Z_o	–	4	–	Ω
Voltage gain	Fig. 22; I_{line} = 15 mA; R4 = 100 kΩ					
single-ended; R_T = 300 Ω		G_v	32,8	33.8	34.8	dB
differential; R_T = 600 Ω		G_v	38.8	39.8	40.8	dB
Variation with frequency, referred to 0.8 kHz	f = 300 and 3400 Hz	ΔG_{vf}	–0.5	±0.25	0.5	dB
Variation with temperature, referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = –25 and +75 °C	ΔG_{vT}	–	± 0.2	–	dB
Output voltage (RMS value)	THD = 2%; sinewave drive; R4 = 100 kΩ; I_{line} = 15 mA					
single-ended; R_T = 150 Ω	I_P = 0 mA	$V_{o(rms)}$	0.21	0.26	–	V
	I_P = 2 mA	$V_{o(rms)}$	0.30	0.40	–	V
differential; R_T = 450 Ω	I_P = 0 mA	$V_{o(rms)}$	0.39	0.49	–	V
	I_P = 2 mA	$V_{o(rms)}$	0.62	0.72	–	V
differential; C_T = 47 nF; (100 Ω series resistor); f = 3400 Hz	I_P = 0 mA	$V_{o(rms)}$	0.59	0.69	–	V
	I_P = 2 mA	$V_{o(rms)}$	0.85	1.05	–	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Output voltage (RMS value)	I_P = 0 mA; THD = 10%; sinewave drive; R4 = 100 kΩ; single-ended; R_T = 150 Ω;					
	I_{line} = 5 mA	$V_{o(rms)}$	–	20	–	mV
	I_{line} = 7 mA	$V_{o(rms)}$	–	100	–	mV
Noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; psophometrically weighted (P53 curve); pin IR open					
	single-ended; R_T = 300 Ω	$V_{no(rms)}$	–	70	–	μV
	differential; R_T = 600 Ω	$V_{no(rms)}$	–	140	–	μV
Noise output voltage (RMS value)	in circuit of Fig. 22; S1 in position 2; single-ended; R_T = 300 Ω					
	R7 = 68 kΩ	$V_{no(rms)}$	–	120	–	μV
	R7 = 24.9 kΩ	$V_{no(rms)}$	–	80	–	μV
Gain adjustment input GAR (pin 6)						
Receiving amplifier, gain adjustment range		ΔG_v	−11	–	+8	dB
MUTE INPUT (pin 14)						
Input voltage HIGH		V_{IH}	1.5 + V_{SLPE}	–	V_{CC1} + 0.4	V
Input voltage LOW		V_{IL}	0	–	0.3 + V_{SLPE}	V
Input current		I_{mute}	–	11	20	μA
Change of microphone amplifier gain at mute-on	MUTE = HIGH	ΔG_v	–	100	–	dB
Voltage gain from input DTMF-SLPE to QR+ output with mute on	MUTE = HIGH; single-ended load; R_L = 300 Ω	G_v	–	−18	–	dB

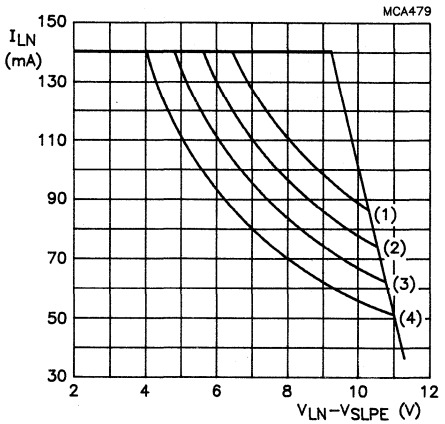
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Power-down input PD (pin 15)						
Input voltage HIGH		V_{IH}	1.5 + V_{SLPE}	–	V_{CC1} + 0.4	V
Input voltage LOW		V_{IL}	0	–	0.3 + V_{SLPE}	V
Input current		I_{PD}	–	5	10	μA
Automatic gain control input AGC (pin 18)						
Controlling the gain from IR (pin 13) to QR+, QR– (pins 4, 5) and the gain from MIC+, MIC– (pins 8, 9) to LN (pin 1)	R6 = 51 kΩ (between pins 18 and 11)					
Gain control range with respect to I_{line} = 15 mA	I_{line} = 73 mA	ΔG_v	–	–8.6	–	dB
Highest line current for maximum gain		I_{line}	–	20	–	mA
Lowest line current for minimum gain		I_{line}	–	70	–	mA



	T_{amb}	P_{tot}
(1)	45 °C	1143 mW
(2)	55 °C	1000 mW
(3)	65 °C	857 mW
(4)	75 °C	714 mW

Fig.19 TEA1063 safe operating area.



	T_{amb}	P_{tot}
(1)	45 °C	888 mW
(2)	55 °C	777 mW
(3)	65 °C	666 mW
(4)	75 °C	555 mW

Fig.20 TEA1063T safe operating area.

DEVELOPMENT DATA

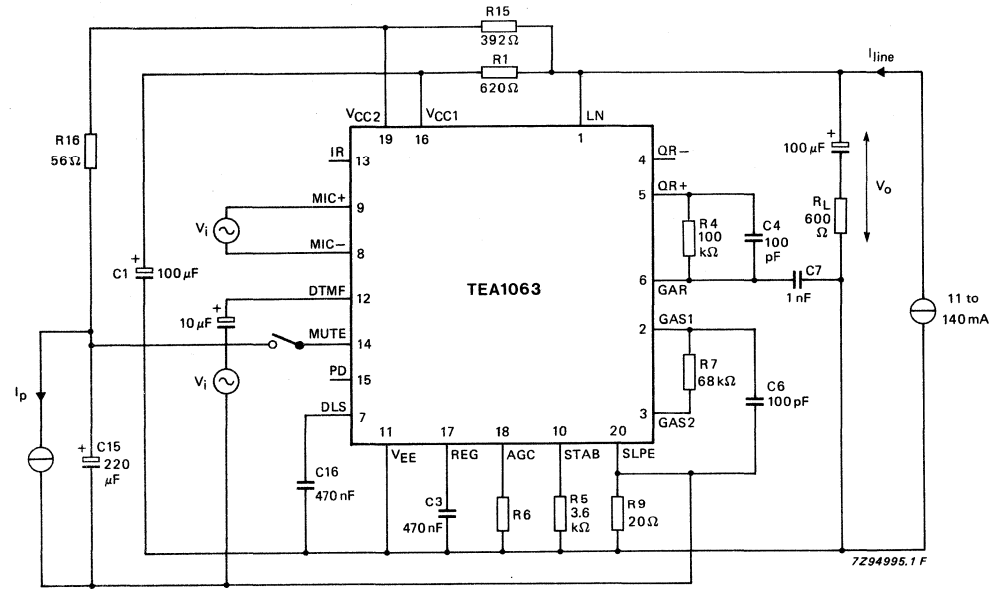


Fig. 21 Test circuit for defining voltage gain of MIC−, MIC+ and DTMF inputs; voltage gain (G_V) is defined as 20 log$|V_O/V_i|$. For measuring the gain from MIC+ and MIC− the MUTE input should be LOW or open-circuit; for measuring the DTMF input, the MUTE input should be HIGH. Inputs not being tested should be open-circuit.

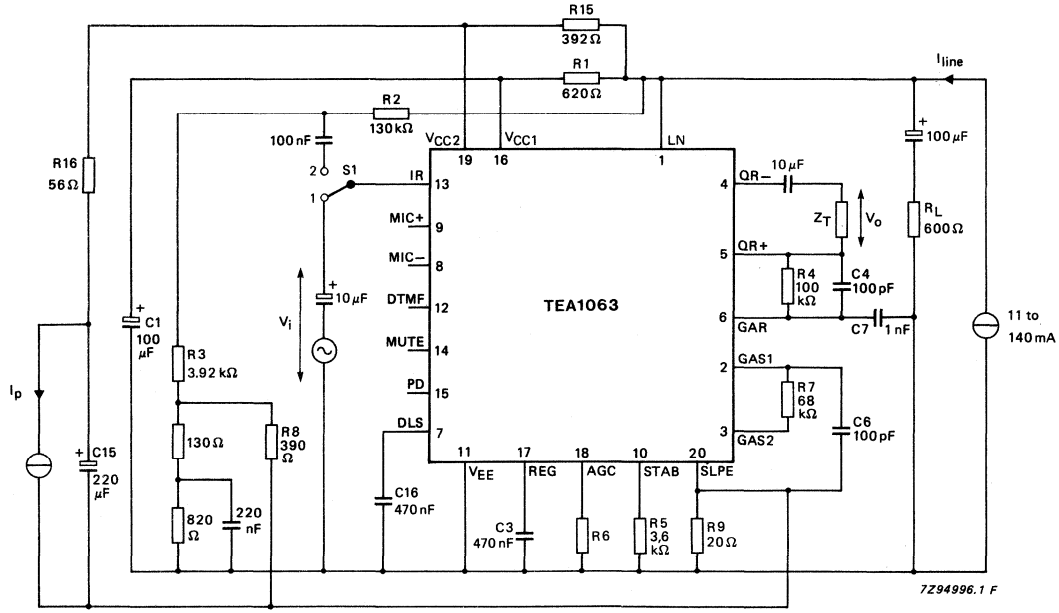


Fig. 22 Test circuit for defining voltage gain of the receiving amplifier, voltage gain (G_V) is defined as 20 log$|V_O/V_i|$ (with S1 in position 1).

APPLICATION INFORMATION

The basic application circuit is shown in Fig. 23 and some typical applications are shown in Figs 24, 25 and 26.

In the basic application, the circuit provides two possibilities for supplies to peripheral circuits:

- regulated line voltage V_{LN} (stabilized $V_{LN-SLPE}$) and unregulated supply voltage for peripheral circuits, the supply voltage is dependent only on the peripheral supply current. This application is comparable to that used for TEA1060/TEA1061, TEA1067 and TEA1068;
- stabilized supply voltage for peripherals ($V_{CC2-SLPE}$), the DC line voltage depends on the current flowing to the peripheral circuits.

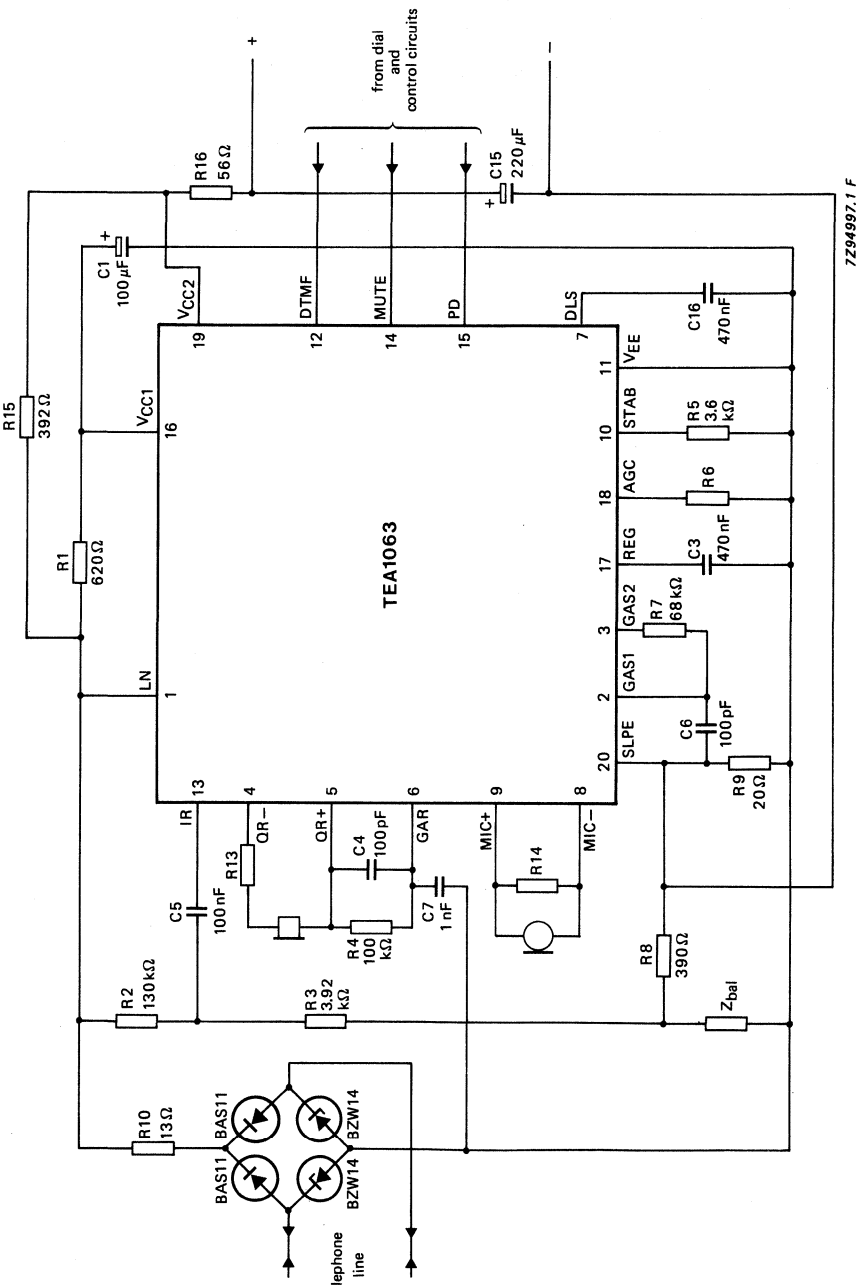


Fig. 23 Basis application of the TEA1063 with stabilized supply for peripherals, shown here with a piezo-electric earpiece and DTMF dialling. The diode bridge and R10 limit the current into, and the voltage across, the circuit during line transients. A different protection arrangement is required for pulse dialling or register recall.

For the basic application giving regulated line voltage the above circuit is changed as follows:

- R15 must be short-circuited;
- the value of R16 is changed to 392 Ω;
- the value of C3 is changed to 4.7 μF.

APPLICATION INFORMATION (continued)

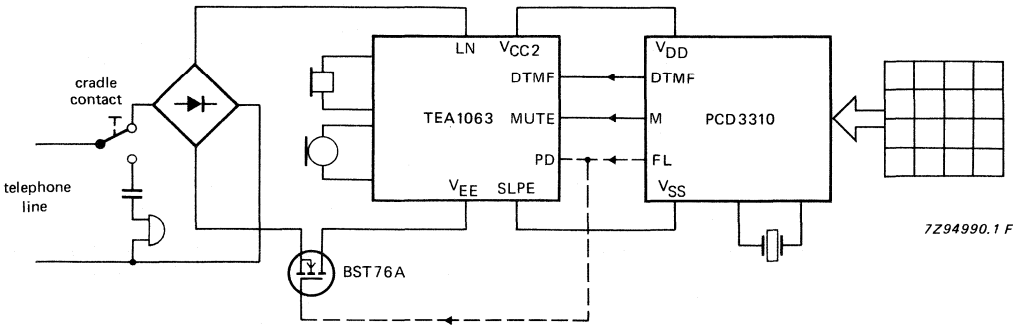


Fig. 24 Typical DTMF-pulse set application circuit (simplified) showing the TEA1063 with the CMOS bilingual dialling circuit PCD3310; the broken line indicates optional flash (register recall by timed loop break).

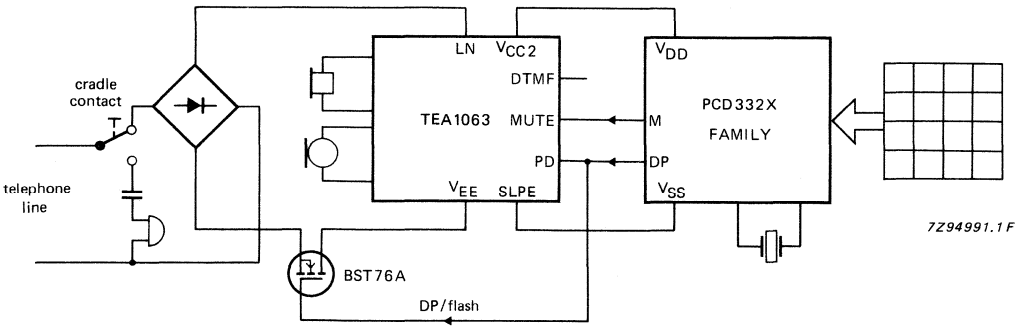


Fig. 25 Typical pulse dial set application circuit (simplified) showing the TEA1063 with one of the PCD332X family of CMOS interrupted current-loop dialling circuits.

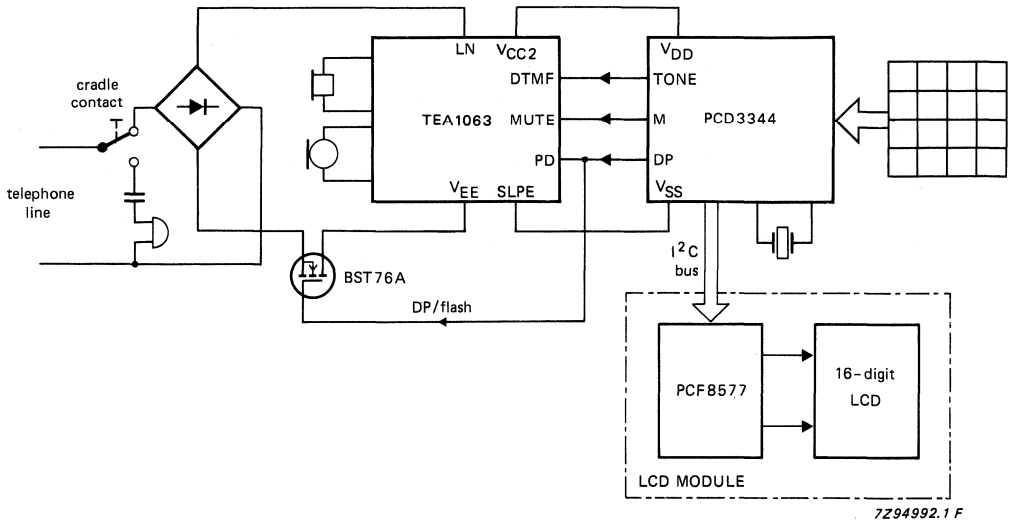


Fig. 26 Typical dual-standard (pulse and DTMF) feature phone application circuit (simplified) showing the TEA1063 and the PCD3344 CMOS telephone microcontroller with on-chip DTMF generator plus I^2C-bus.

LOW VOLTAGE VERSATILE TELEPHONE TRANSMISSION CIRCUIT WITH DIALLER INTERFACE AND TRANSMIT LEVEL DYNAMIC LIMITING

GENERAL DESCRIPTION

The TEA1064A is a bipolar integrated circuit that performs all the speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech and has a powerful DC supply for peripheral circuits. The IC operates at line voltages down to 1.8 V DC (with reduced performance) to facilitate the use of more telephone sets connected in parallel. The transmit signal on the line is dynamically limited (speech-controlled) to prevent distortion at high transmit levels of both the sending signal and the sidetone.

Features

- Low DC line voltage; operates down to 1.8 V (excluding polarity guard)
- Voltage regulator with low voltage drop and adjustable static resistance
- DC line voltage adjustment facility
- Provides a supply for external circuits in two options:
  unregulated supply, regulated line voltage;
  stabilized supply, line voltage varies with supply current
- Dynamic limiting (speech-controlled) in transmit direction prevents distortion of line signal and sidetone
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphones
- DTMF signal input
- Confidence tone in the earpiece during DTMF dialling
- Mute input for disabling speech during pulse or DTMF dialling
- Power-down input for improved performance during pulse dial or register recall (flash)
- Receiving amplifier for magnetic, dynamic or piezo-electric earpieces
- Large amplification setting ranges on microphone and earpiece amplifiers
- Line loss compensation (line current dependent) for microphone and earpiece amplifiers (not used for DTMF amplifier)
- Gain control curve adaptable to exchange supply
- Automatic disabling of the DTMF amplifier in extremely-low voltage conditions
- Microphone MUTE function available with switch

PACKAGE OUTLINES

TEA1064A : 20-lead DIL; plastic (SOT146).
TEA1064AT: 20-lead mini-pack; plastic (SO20; SOT163A).

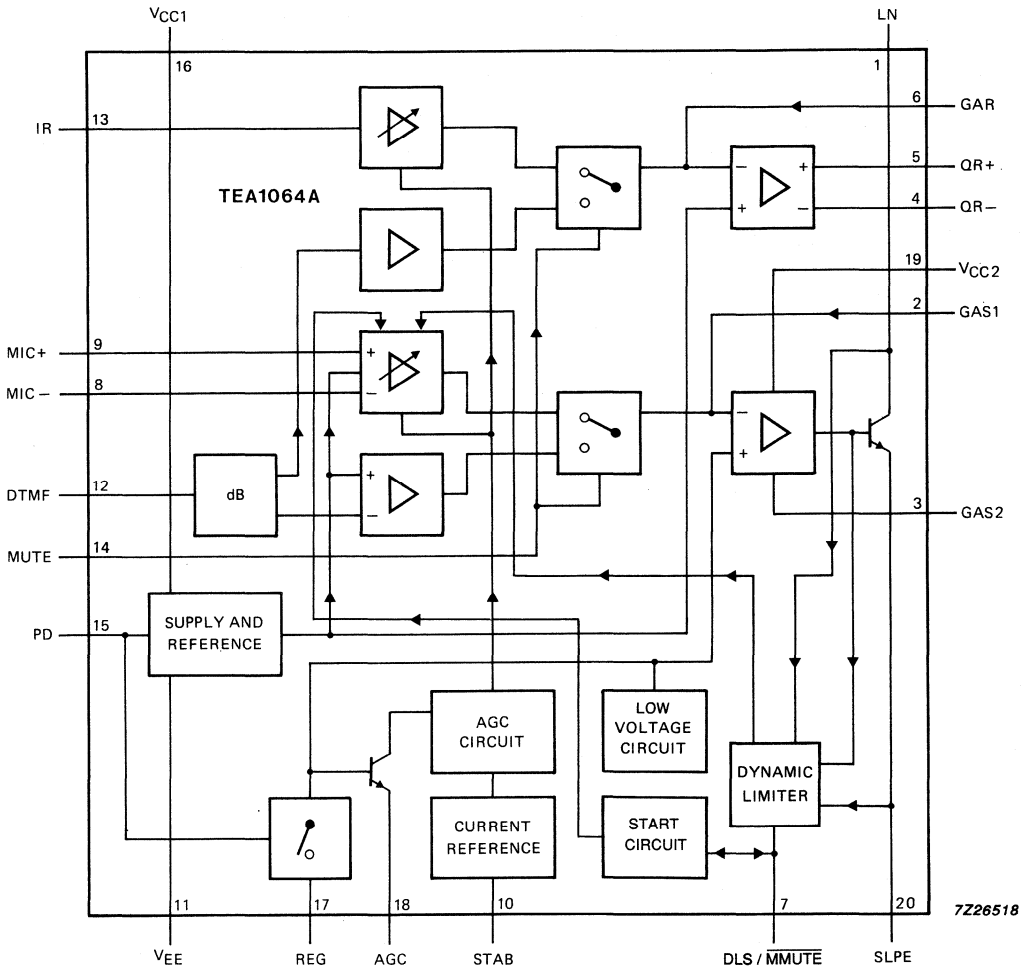


Fig. 1 Block diagram.

DEVELOPMENT DATA

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Operating ambient temperature range		T_{amb}	−25	–	+ 75	°C
Line current operating range:						
normal operation		I_{line}	11	–	140*	mA
with reduced performance		I_{line}	2	–	11	mA
Internal supply current:						
power-down input LOW	V_{CC1} = 2.8 V	I_{CC1}	–	1.3	1.6	mA
power-down input HIGH	V_{CC1} = 2.8 V	I_{CC1}	–	60	82	μA
Voltage gain range:						
microphone amplifier		G_v	44	–	52	dB
receiving amplifier		G_v	20	–	45	dB
Line loss compensation:						
gain control range		G_v	5.7	6.1	6.5	dB
exchange supply voltage range		V_{exch}	36	–	60	V
exchange feeding bridge resistance range		R_{exch}	400	–	1000	Ω
Maximum output voltage swing on LN (peak-to-peak value)	R15 + R16 = 448 Ω					
	I_{line} = 15 mA					
	I_p = 2 mA	$V_{LN(p-p)}$	3.7	3.95	4.2	V
	I_p = 4 mA	$V_{LN(p-p)}$	3.0	3.25	3.5	V
Regulated line voltage application						
	R15 = 0 Ω; R16 = 392 Ω					
Supply for peripherals	I_{line} = 15 mA					
	I_p = 1.4 mA	V_p	2.5	–	–	V
	I_p = 2.7 mA; $R_{REG-SLPE}$ = 20 kΩ	V_p	2.9	–	–	V
DC line voltage	I_{line} = 15 mA					
	without $R_{REG-SLPE}$	V_{LN}	–	3.57	–	V
	$R_{REG-SLPE}$ = 20 kΩ	V_{LN}	–	4.57	–	V
Stabilized supply voltage application						
	R15 = 392 Ω; R16 = 56 Ω					
Supply for peripherals	I_{line} = 15 mA					
	I_p = 0 to 4 mA	$V_{CC2-SLPE}$	3.05	3.3	3.55	V
DC line voltage	I_{line} = 15 mA					
	I_p = 2 mA	V_{LN}	4.2	4.4	4.8	V
	I_p = 4 mA	V_{LN}	4.9	5.1	5.5	V

* For TEA1064AT the maximum line current depends on the heat dissipating qualities of the mounted device.

PINNING

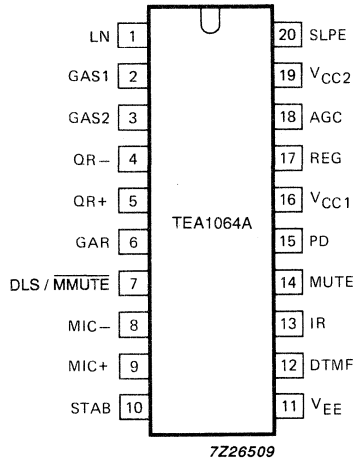


Fig. 2 Pinning diagram.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR−	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	DLS/$\overline{\text{MMUTE}}$	decoupling for transmit amplifier dynamic and microphone MUTE input
8	MIC−	inverting microphone input
9	MIC+	non-inverting microphone input
10	STAB	current stabilizer
11	V_{EE}	negative line terminal
12	DTMF	dual-tone multi-frequency input
13	IR	receiving amplifier input
14	MUTE	mute input
15	PD	power-down input
16	V_{CC1}	internal supply decoupling
17	REG	voltage regulator decoupling
18	AGC	automatic gain control input
19	V_{CC2}	reference voltage with respect to SLPE
20	SLPE	slope adjustment for DC curve/reference for peripheral circuits.

FUNCTIONAL DESCRIPTION

Supplies V_{CC1}, V_{CC2}, LN, SLPE, REG and STAB (Fig. 3)

Power for the TEA1064A and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply voltage at V_{CC1} and regulates its voltage drop. The internal supply requires a decoupling capacitor between V_{CC1} and V_{EE}. The internal current stabilizer is set by a 3.6 kΩ resistor between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the subscriber line DC resistance R_{line} and the DC voltage (including polarity guard) on the subscriber set (see Fig. 3).

The internal voltage regulator generates a temperature-compensated reference voltage that is available between V_{CC2} and SLPE [$V_{ref} = V_{CC2\text{-}SLPE}$ = 3.3 V (typ.)] .This internal voltage regulator requires decoupling by a capacitor between REG and V_{EE} (C3).

The reference voltage can be used to:

- regulate directly the line voltage (stabilized $V_{LN\text{-}SLPE} = V_{CC2\text{-}SLPE}$)*;
- to stabilize the supply voltage for peripherals.

Regulated line voltage

In this application the V_{CC2} pin is connected to the LN pin as shown in Fig. 3. This configuration gives a stabilized voltage across pins LN and SLPE which, applied via the low-pass filter R16, C15, provides a supply to the peripherals that is independent of the line current and depends only on the peripheral supply current.

The value of R16 and the level of the DC voltage $V_{LN\text{-}SLPE}$ determine the supply capabilities. In the basic application R16 = 392 Ω and C15 = 220 μF. The worst-case peripheral supply current as a function of supply voltage is shown in Fig. 4. To increase the supply capabilities, the DC voltage $V_{LN\text{-}SLPE}$ can be increased by using $R_{VA(REG\text{-}SLPE)}$ or by decreasing the value of R16.

* The TEA1064A application with regulated line voltage is the same as is used for TEA1060/TEA1061, TEA1067 and TEA1068 integrated circuits.

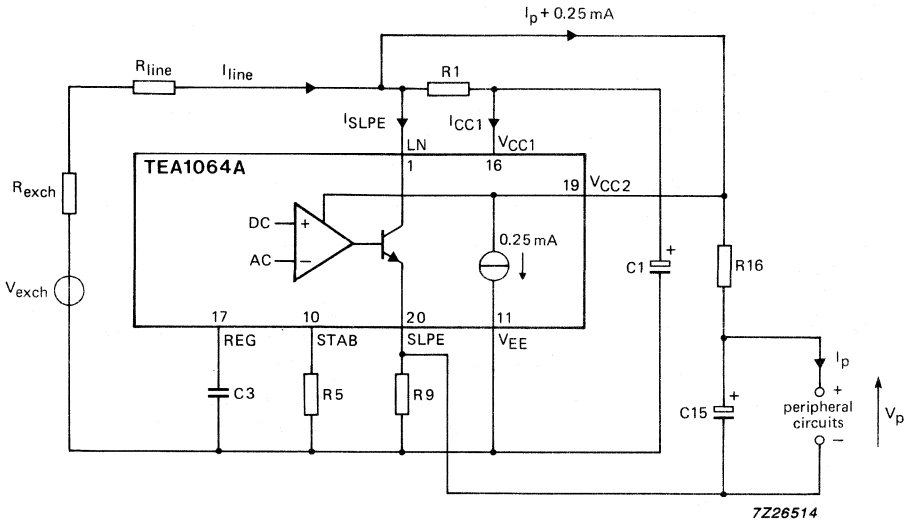


Fig. 3 Application with regulated line voltage (stabilized $V_{LN-SLPE}$). The voltage $V_{LN-SLPE}$ is fixed to V_{ref} = 3.3 ± 0.25 V. Resistor R16 together with the line current determine the supply capabilities and the maximum output swing on the line (no loop damping is necessary). The line voltage V_{LN} = V_{ref} + ([I_{line} - 1.55 mA] x R9).

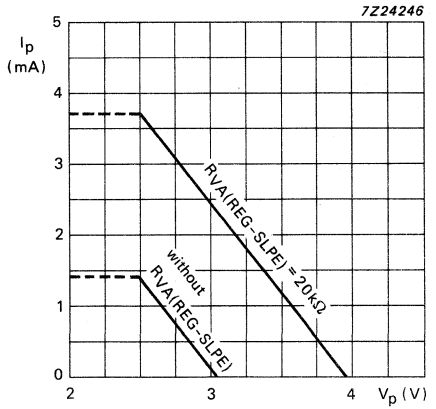


Fig. 4 Minimum supply current for peripherals (I_p) as a function of the peripheral supply voltage (V_p): I_{line} = 15 mA; R16 = 392 Ω; R15 = 0 Ω; valid for MUTE = 0 and 1. Line current has very little influence.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Regulated line voltage (continued)

The maximum AC output swing on the line at low line currents is influenced by R16 (limited by current) and the maximum output swing on the line at high line currents is influenced by the DC voltage $V_{LN-SLPE}$ (limited by voltage). In both these situations, the internal dynamic limiter in the sending channel prevents distortion when the microphone input is overdriven. The maximum AC output swing on LN is shown in Fig. 5; practical values for R16 are from 200 to 600 Ω and this influences both the maximum output swing at low line currents and the supply capabilities.

The SLPE pin is the ground reference for peripheral circuits, therefore inputs MUTE, PD and DTMF are also referenced to SLPE.

Active microphones can be supplied between V_{CC1} and V_{EE}. Low-power circuits that provide only MUTE and/or PD inputs to the TEA1064A also can be powered from V_{CC1}. However V_{CC1} cannot be used for circuits that provide DTMF signals to the TEA1064A because V_{CC1} is referred to ground.

If the line current I_{line} exceeds I_{CC1} + 0.25 mA, the voltage converter shunts the excess current to SLPE via LN; where $I_{CC1} \approx 1.3$ mA, the value required by the IC for normal operation.

The DC line voltage on LN is:

$$V_{LN} = V_{LN-SLPE} + (I_{SLPE} \times R9)$$

$$V_{LN} = V_{ref} + ([I_{line} - I_{CC1} - 0.25 \times 10^{-3} A] \times R9)$$

in which

V_{ref} = 3.3 V ± 0.25 V is the internal reference voltage between V_{CC2} and SLPE; its value can be adjusted by external resistor R_{VA}

R9 = external resistor between SLPE and V_{EE} (20 Ω in basic application).

With R9 = 20 Ω, this results in:

V_{LN} = 3.57 ± 0.25 V at I_{line} = 15 mA

V_{LN} = 4.17 ± 0.3 V at I_{line} = 15 mA, $R_{VA(REG-SLPE)}$ = 33 kΩ

V_{LN} = 4.57 ± 0.35 V at I_{line} = 15 mA, $R_{VA(REG-SLPE)}$ = 20 kΩ

The preferred value for R9 is 20 Ω. Changing R9 influences microphone gain, DTMF gain, the gain control characteristics, sidetone, and the DC characteristics (especially the low voltage characteristics).

In normal conditions, $I_{SLPE} >> (I_{CC1} + 0.25$ mA) and the static behaviour is equivalent to a voltage regulator diode with an internal resistance of R9. In the audio frequency range the dynamic impedance is determined mainly by R1. The equivalent impedance of the circuit in the audio frequency range is shown in Fig. 6.

The internal reference voltage $V_{CC2-SLPE}$ can be increased by external resistor $R_{VA(REG-SLPE)}$ connected between REG and SLPE. The supply voltage $V_{CC2-SLPE}$ is shown as a function of $R_{VA(REG-SLPE)}$ in Fig. 7. Changing the reference voltage influences the output swing of both sending and receiving amplifiers.

At line currents below 8 mA (typ.), the DC voltage dropped across the circuit is adjusted to a lower level automatically (approximately 1.8 V at 2 mA). This gives the possibility of operating more telephone sets in parallel with DC line voltages (excluding polarity guard) down to an absolute minimum of 1.8 V. At line currents below 8 mA (typ.), the circuit has limited sending and receiving levels.

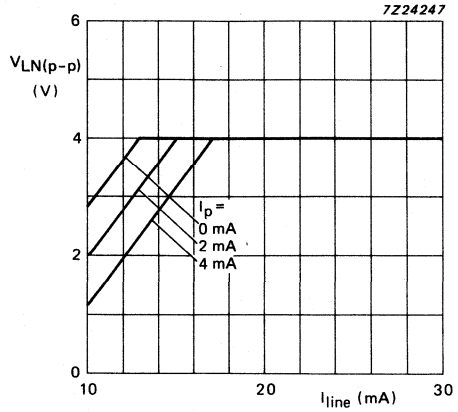


Fig. 5 Maximum AC output swing on the line as a function of line current with peripheral supply current as a parameter: R15 = 0 Ω; R16 = 392 Ω.

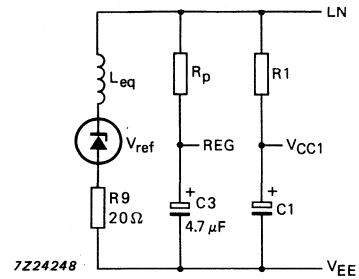


Fig. 6 Equivalent impedance between LN and V_{EE} in the application with stabilized $V_{LN-SLPE}$:
R15 = 0 Ω
L_{eq} = C3 x R9 x R_p
R_p = 15 kΩ

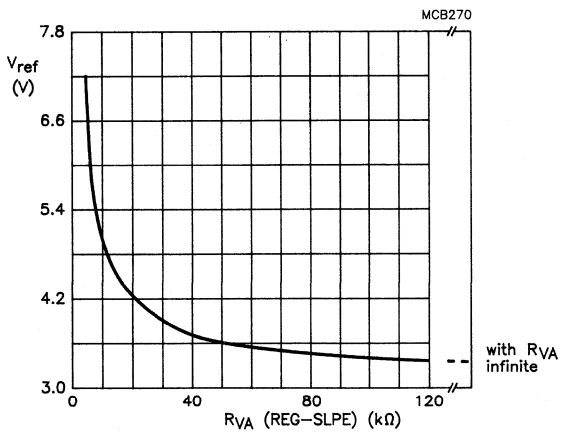


Fig. 7 Internal reference voltage $V_{CC2-SLPE}$ as a function of resistor $R_{VA(REG-SLPE)}$ for line currents between 11 and 140 mA.

In the stabilized supply application:

$$V_{LN} = V_{CC2-SLPE} + ([I_p + 0.25 \times 10^{-3}\,A] \times R15) + ([I_{line} - 1.55 \times 10^{-3}\,A] \times R9)$$

In the unregulated supply application (R15 = 0 Ω):

$$V_{LN} = V_{CC2-SLPE} + ([I_{line} - 1.55 \times 10^{-3}\,A] \times R9)$$

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Stabilized peripheral supply voltage

The configuration shown in Fig. 8 provides a stabilized voltage across pins V_{CC2} and SPLE for peripheral circuits (such as dialling and control circuits); the DC voltage V_{LN} now varies with the peripheral supply current.

The $V_{CC2\text{-}SLPE}$ supply must be decoupled by capacitor C15. For stable loop operation, resistor R16 ($\approx 50\ \Omega$) is connected between V_{CC2} and SLPE in series with C15. The voltage regulator control loop is completed by resistor R15 between LN and V_{CC2}.

For sets with an impedance of 600 Ω, practical values are: R15 = 200 to 600 Ω; C15 = 220 μF; C3 = 470 nF. The ratio $R15/R16 \leqslant 8$ is for stable loop operation with sufficient phase margin, and $R15/R16 \geqslant 6$ is for satisfactory set impedance in the audio frequency range.

For sets with complex impedance, the value of C3 and the ratio R15/R16 are different (further information is given in the TEA1064A Application Report*).

The peripheral supply capability depends mainly on the available line current, the required AC output swing on the line, the maximum permitted DC voltage on the line and the values of external components (especially R15). With R15 = 392 Ω and R16 = 56 Ω (basic application) the maximum possible AC output swing on the line as a function of line current is as shown in Fig. 9, the curve parameter is the peripheral supply current (I_p). Different values for R15 (from 200 to 600 Ω) maintaining $6 < R15/R16 < 8$ give different results (these are described in the TEA1064A Application Report*).

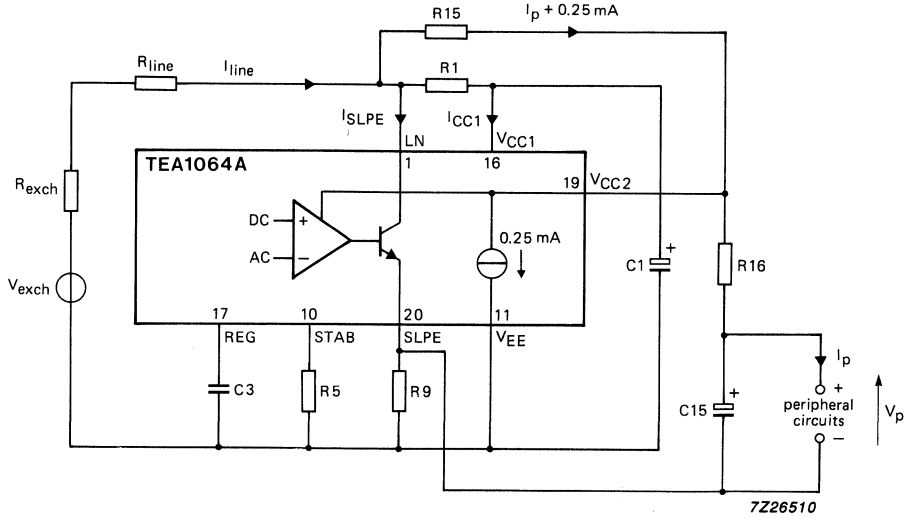


Fig. 8 Application with stabilized supply voltage for peripheral circuits: R15 = 392 Ω; R16 = 56 Ω.

* Supplied on request.

The DC line voltage on LN is

$$V_{LN} = V_{LN\text{-}SLPE} + (I_{SLPE} \times R9).$$

Therefore

$$V_{LN} = V_{ref} + ([I_p + 0.25 \times 10^{-3}\,A] \times R15) + ([I_{line} - I_{CC1} - 0.25 \times 10^{-3}\,A] \times R9)$$

in which:

V_{ref} is the internal reference voltage between V_{CC2} and SLPE (the value of V_{ref} can be adjusted by an external resistor, R_{VA}). V_{ref} = 3.3 V (typ.) without R_{VA}

I_p is the supply current used by peripheral circuits

R15 is an external resistor between LN and V_{CC2} (392 Ω in the basic application)

R9 is an external resistor between SLPE and V_{EE} (20 Ω in the basic application)

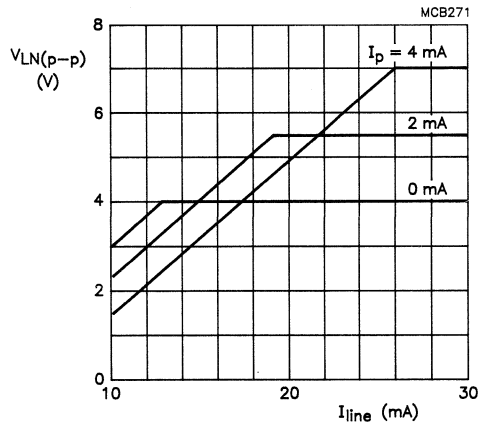


Fig. 9 Maximum output swing on line as a function of line current with the peripheral supply current as a parameter; R15 = 392 Ω; R16 = 56 Ω. As different values of R15 and R16 are allowed, different curves would then apply.

The DC voltage $V_{LN\text{-}SLPE}$ as a function of I_p with R15 as a parameter is shown in Fig. 10. In the audio frequency range, the dynamic impedance is determined mainly by R1. The equivalent impedance in the audio range of the circuit (Fig. 8) is shown in Fig. 11.

FUNCTIONAL DESCRIPTION (continued)

Stabilized peripheral supply voltage (continued)

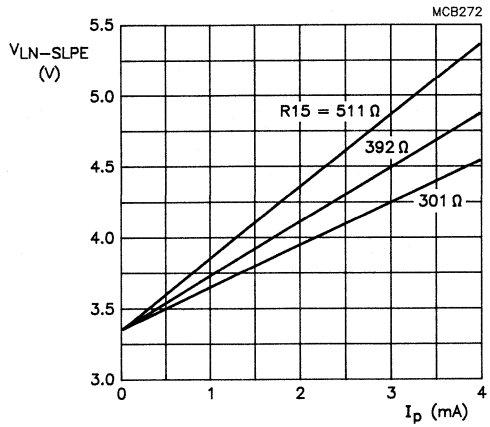
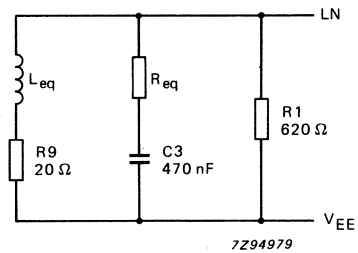


Fig. 10 Curves showing the typical voltage drop between LN and SLPE as a function of the supply current for peripherals with R15 as a parameter: $V_{CC2-SLPE}$ = 3.3 V (R_{VA} not connected). $V_{CC2-SLPE}$ can be adjusted between approximately 3.3 and 4.3 V by changing the value of R_{VA}, this results in a parallel-shift of the curves.
The total voltage drop $V_{LN} \approx V_{LN-SLPE} + ([I_{line} - 1.55\ mA] \times R9)$.



$$R_{eq} = R_p \left(\frac{R15}{R16} + 1\right)$$

$$L_{eq} = C3 \times R9 \times R_{eq}$$

with R_p = 15 kΩ

Fig. 11 Equivalent impedance between LN and V_{EE} at f > 300 Hz in the application with stabilized supply voltage for peripheral circuits.

Microphone inputs MIC+ and MIC− and gain pins GAS1 and GAS2

The TEA1064A has symmetrical microphone inputs, its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage amplification is typ. 52 dB with R7 = 68 kΩ. Either dynamic, magnetic or piezo-electric microphones can be used, or an electret microphone with a built-in FET buffer. Arrangements for the microphone types are shown in Fig. 12.

The gain of the microphone amplifier is proportional to external resistor R7 connected between GAS1 and GAS2 and with this it can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer.

An external 100 pF capacitor (C6) is required between GAS1 and SLPE to ensure stability. A larger value of C6 may be chosen to obtain a first-order low-pass filter with a cut-off frequency corresponding to the time constant R7 x C6.

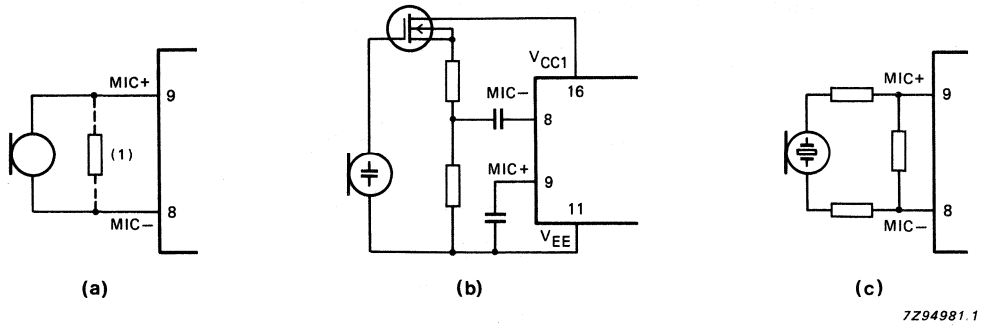


Fig. 12 Microphone arrangements: a) magnetic or dynamic microphone, the resistor (1) may be connected to reduce the terminating impedance, or for sensitive types a resistive attenuator can be used to prevent overloading the microphone inputs; b) electret microphone; c) piezo-electric microphone.

Dynamic limiter (microphone) pin DLS/$\overline{\text{MMUTE}}$

A low level at the DLS/$\overline{\text{MMUTE}}$ pin inhibits the microphone inputs MIC+ and MIC− but has no influence on the receiving and DTMF amplifiers.
Removing the low level at the DLS/$\overline{\text{MMUTE}}$ pin provides the normal function of the microphone amplifier after a short time determined by the capacitor connected to DLS/$\overline{\text{MMUTE}}$ pin. The microphone mute function can be realised by a simple switch as shown in Fig.13.

To prevent distortion of the transmitted signal, the gain of the sending amplifier is reduced rapidly when peaks of the signal on the line exceed an internally-determined threshold. The time in which gain reduction is effected (attack time) is very short. The circuit stays in the gain-reduced condition until the peaks of the sending signal remain below the threshold level. The sending gain then returns to normal after a time determined by the capacitor connected to DLS/$\overline{\text{MMUTE}}$ (release time).

The internal threshold adapts automatically to the DC voltage setting of the circuit (voltage $V_{LN-SLPE}$). This means that the maximum output swing on the line will be higher if the DC voltage dropped across the circuit is increased.

Fig. 14 shows the maximum possible output swing on the line as a function of the DC voltage drop ($V_{LN-SLPE}$) with $I_{line} - I_p$ as a parameter.

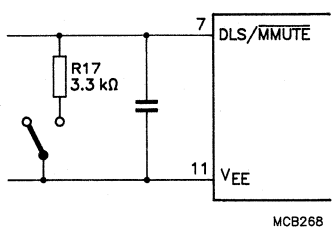


Fig. 13 Microphone-mute function.

FUNCTIONAL DESCRIPTION (continued)

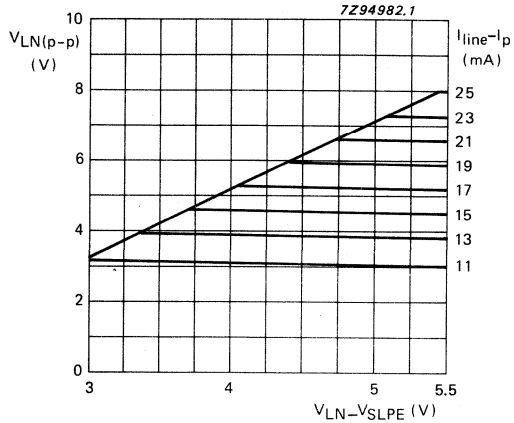


Fig. 14 Maximum output swing on line as a function of the DC voltage drop $V_{LN-SLPE}$ with $I_{line} - I_p$ as a parameter: R15 = 392 Ω; R16 = 56 Ω; or R15 = 0 Ω and R16 = 392 + 56 = 448 Ω.

The internal threshold level is lowered automatically if the DC current in the transmit output stage is insufficient. This prevents distortion of the sending signal in applications using parallel-connected telephones or telephones operating over long lines, for example.

Dynamic limiting also considerably improves sidetone performance in over-drive conditions (less distortion; limited sidetone level).

Receiving amplifier IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, QR+ (non-inverting) and QR− (inverting). These outputs may be used for single-ended or differential drive, depending on the type and sensitivity of the earpiece used (see Fig. 15). Gain from IR to QR+ is typically 31 dB with R4 = 100 kΩ, sufficient for low-impedance magnetic or dynamic earpieces which are suitable for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB. Differential drive can be used when the earpiece impedance exceeds 450 Ω as with high-impedance dynamic, magnetic or piezo-electric earpieces.

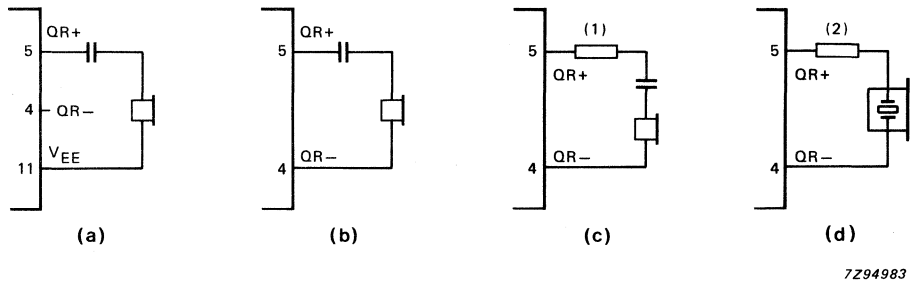


Fig. 15 Alternative receiver arrangements: a) dynamic earpiece with an impedance less than 450 Ω; b) dynamic earpiece with an impedance more than 450 Ω; c) magnetic earpiece with an impedance more than 450 Ω, resistor (1) may be connected to prevent distortion (inductive load); d) piezo-electric earpiece, resistor (2) is required to increase the phase margin (stability with capacitive load).

The output voltage of the receiving amplifier is specified for continuous-wave drive. Fig. 16 shows the maximum output swing of the receiving amplifier as a function of the DC voltage drop (V_{LN}). The maximum output voltage will be higher under speech conditions, where the ratio of the peak to the RMS value is higher.

The gain of the receiving amplifier can be adjusted to suit the sensitivity of the transducer used. The adjustment range is between 20 dB and 39 dB with single-ended drive and between 26 dB and 45 dB with differential drive. The gain is proportional to the external resistor R4 connected between GAR and QR+. The overall gain between LN and QR+ can be found by subtracting the attenuation of the anti-sidetone network (32 dB) from the amplifier gain.

Two external capacitors (C4 = 100 pF and C7 = 10 x C4 = 1 nF) ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R4 x C4. The relationship C7 = 10 x C4 must be maintained.

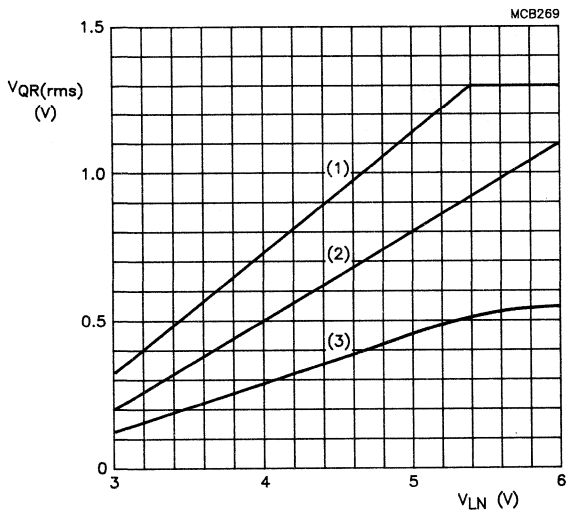


Fig. 16 Maximum output swing of the receiving amplifier as a function of DC voltage drop V_{LN} with the load at the receiver output as parameter: valid for both supply options; THD = 2%; I_{line} = 15 mA. Curve (1) is for a differential load of 47 nF (series resistance = 100 Ω); f = 3400 Hz. Curve (2) is for a differential load of 450 Ω; f = 1 kHz. Curve (3) is for a single-ended load of 150 Ω; f = 1 kHz.

DEVELOPMENT DATA

Automatic gain control input AGC

Automatic compensation of line loss is obtained by connecting a resistor (R6) between AGC and V_{EE}. This automatic gain control varies the gain of the microphone amplifier and receiving amplifier in accordance with the DC line current. The control range is 6.1 dB; this corresponds to a 5 km line of 0.5 mm diameter copper twisted-pair cable (DC resistance = 176 Ω/km, average attenuation = 1.2 dB/km). The DTMF gain is not affected by this feature.

The value of R6 must be chosen with reference to the exchange supply voltage and its feeding bridge resistance (see Fig. 17 and Table 1). Different values of R6 give the same line current ratios at the start and the end of the control range. If automatic line-loss compensation is not required the AGC pin can be left open, the amplifiers then give their maximum gain.

FUNCTIONAL DESCRIPTION (continued)

Automatic gain control input AGC (continued)

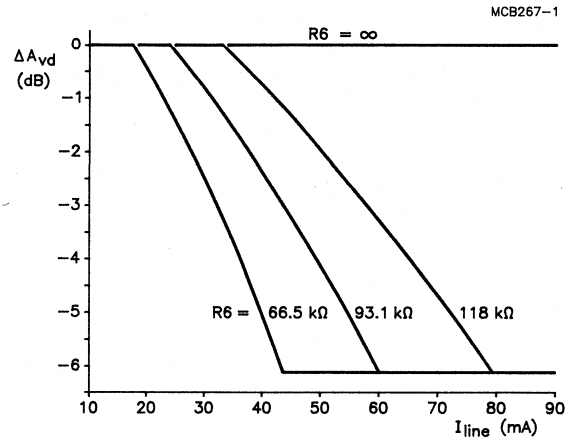


Fig. 17 Variation of gain as a function of line current with R6 as a parameter; R9 = 20 Ω.

Table 1 Values of R6 giving optimum line-loss compensation at various values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	36	84.5	66.5	X	X
	48	118	93.1	77.8	66.5
	60	X	X	97.6	84.5

MUTE input (see notes 1 and 2)

MUTE = HIGH enables the DTMF input and inhibits the microphone and receiving amplifier inputs.

MUTE = LOW or open-circuit disables the DTMF input and enables the microphone and receiving amplifier inputs.

Switching MUTE gives negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF (see note 1)

When the DTMF input is enabled, dialling tones may be sent on to the line. The voltage gain between DTMF-SLPE and LN-V_{EE} is typ. 26 dB less than the gain of the microphone amplifier and varies with R7 in the same way as the gain of the microphone amplifier. This means that the tone level at the DTMF input has to be adjusted after setting the gain of the microphone amplifier.
With R7 = 68 kΩ the gain is typically 26 dB.

The signalling tones can be heard in the earpiece at a low level (confidence tone).

Power-down input PD (see notes 1 and 2)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted; as a consequence it provides no supply for the transmission circuit connected to V_{CC1} or for the peripherals between V_{CC2} and SLPE.
These supply gaps are bridged by the charges in the capacitors C1 and C15. The requirements on these capacitors are eased by applying a HIGH level to the PD input during the time of the loop break. This reduces the internal supply current I_{CC1} from (typ.) 1.3 mA to (typ.) 60 μA and switches off the voltage regulator to prevent discharge via LN and V_{CC2}.

A HIGH level at PD also internally disconnects the capacitor at REG so that the voltage stabilizer has no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall.

When the power-down facility is not required, the PD pin can be left open-circuit or connected to SLPE.

DEVELOPMENT DATA

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-sidetone network comprising $R1//Z_{line}$, R2, R3, R8, R9 and Z_{bal} (see Fig. 18). Maximum compensation is obtained when the following conditions are fulfilled:

$$a)\quad R9 \times R2 = R1 \times (R3 + [R8//Z_{bal}])$$

$$b)\quad (Z_{bal}/[Z_{bal} + R8]) = (Z_{line}/[Z_{line} + R1])$$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) is always fulfilled provided $|R8//Z_{bal}| \ll R3$.

To obtain optimum sidetone suppression, condition b) has to be fulfilled, resulting in:

$$Z_{bal} = (R8/R1) \times Z_{line} = k \times Z_{line}$$

where k is a scale factor; k = (R8/R1).

The scale factor k (value of R8) is chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal};
- $|Z_{bal}//R8| \ll R3$ to fulfill condition a) and thus ensure correct anti-sidetone bridge operation;
- $|Z_{bal} + R8| \gg R9$ to avoid influencing the transmit gain.

In practice Z_{line} varies considerably with the line length and line type. Therefore the value chosen for Z_{bal} should be for an average line length giving satisfactory sidetone suppression with short and long lines. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

Example

The line impedance for which optimum suppression is to be obtained can be represented by 210 Ω + (1265 Ω // 140 nF). This represents a 5 km line of 0.5 mm diameter copper twisted-pair cable matched with 600 Ω (176 Ω/km; 38 nF/km).

With k = 0.64 this results in: R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω // 220 nF).

Side-tone suppression (continued)

The anti-sidetone network for the TEA1060 family shown in Fig. 18 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range.

Alternatively a conventional Wheatstone bridge can be used as an anti-sidetone circuit (Fig. 19). Both bridge types can be used with either resistive or complex set impedances. (More information on the balancing of anti-sidetone bridges can be obtained in our publication 'Versatile speech transmission ICs for electronic telephone sets', order number 9398 341 10011.)

Notes

1. The reference used for the MUTE, DTMF and PD inputs is SLPE.
2. A LOW level for any of these pins is defined by connection to SLPE, a HIGH level is defined as a voltage greater than V_{SLPE} + 1.5 V and smaller than V_{CC1} + 0.4 V.

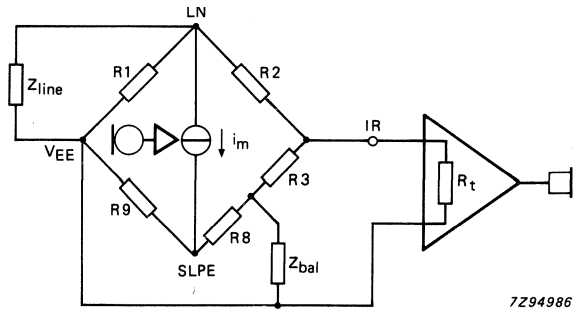


Fig. 18 Equivalent circuit of TEA1060 family anti-side-tone bridge.

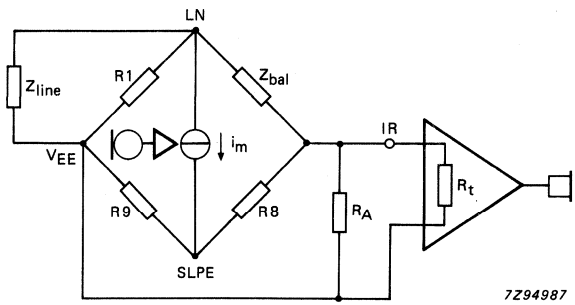


Fig. 19 Equivalent circuit of an anti-sidetone network in the Wheatstone bridge configuration.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive line voltage continuous		V_{LN}	–	12	V
Repetitive line voltage during switch-on line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage one 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω (Fig. 24)	V_{LN}	–	28	V
Line current TEA1064A (1)	R9 = 20 Ω	I_{LN}	–	140	mA
Line current TEA1064AT (1)	R9 = 20 Ω	I_{LN}	–	140	mA
Input voltage on pins other than LN and V_{CC2}		V_i	$V_{EE}-0.7$	$V_{CC1}+0.7$	V
Total power dissipation (2)	R9 = 20 Ω				
TEA1064A		P_{tot}	–	714	mW
TEA1064AT		P_{tot}	–	555	mW
Storage temperature range		T_{stg}	−40	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

(1) Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE. See Figs 20 and 21 to determine the current as a function of the required voltage and the temperature.

(2) Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

From junction to ambient in free air

TEA1064A	$R_{th\ j\text{-}a}$	=	70 K/W
TEA1064AT mounted on glass epoxy board 41 x 19 x 1.5 mm	$R_{th\ j\text{-}a}$	=	90 K/W

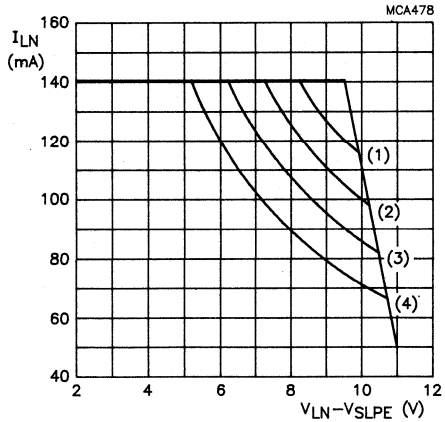


Fig. 20 TEA1064A safe operating area.

	T_{amb}	P_{tot}
(1)	45 °C	1143 mW
(2)	55 °C	1000 mW
(3)	65 °C	857 mW
(4)	75 °C	714 mW

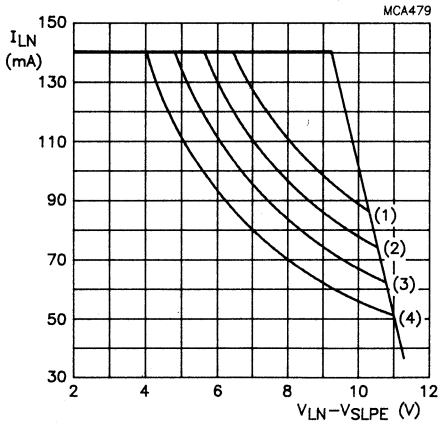


Fig. 21 TEA1064AT safe operating area.

	T_{amb}	P_{tot}
(1)	45 °C	888 mW
(2)	55 °C	777 mW
(3)	65 °C	666 mW
(4)	75 °C	555 mW

DEVELOPMENT DATA

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; R_L = 600 Ω; tested in the circuit of Fig. 22 or 23); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies LN, V_{CC1}, V_{CC2} (pins 1, 16, 19)						
Reference DC voltage between V_{CC2} and SLPE	I_{line} = 15 mA I_p = 0; 4 mA					
R_{VA} not connected		$V_{CC2-SLPE}$	3.05	3.3	3.55	V
Variation with temperature	I_{line} = 15 mA	$\frac{V_{CC2-SLPE}}{\Delta T}$	−3.0	−1.0	1.0	mV/K
Variation with line current referred to 15 mA	I_{line} = 100 mA	$\Delta V_{CC2-SLPE}$	–	60	–	mV
With R_{VA} connected between REG and SLPE	R_{VA} = 33 kΩ	$V_{CC2-SLPE}$	3.6	3.8	4.2	V
	R_{VA} = 20 kΩ	$V_{CC2-SLPE}$	3.95	4.2	4.65	V
DC line voltage:						
voltage drop between LN and V_{EE}	MIC−, MIC+ inputs open; R15 = 392 Ω; without R_{VA}					
at I_{line} = 15 mA	I_p = 0 mA	V_{LN}	3.4	3.6	4.0	V
	I_p = 2 mA	V_{LN}	4.2	4.4	4.8	V
	I_p = 4 mA	V_{LN}	4.9	5.1	5.5	V
at I_{line} = 100 mA	I_p = 2 mA	V_{LN}	–	6.1	7.0	V
at I_{line} = 140 mA	I_p = 2 mA	V_{LN}	–	7.0	7.8	V
Voltage drop under low current conditions	I_p = 0 mA					
	I_{line} = 2 mA	V_{LN}	–	1.8	–	V
	I_{line} = 4 mA	V_{LN}	*	2.2	*	V
	I_{line} = 7 mA	V_{LN}	*	3.2	*	V
	I_{line} = 11 mA	V_{LN}	*	3.5	*	V
Internal supply current I_{CC1}:						
current into pin V_{CC1}	V_{CC1} = 2.8 V					
	PD = LOW	I_{CC1}	–	1.3	1.6	mA
	PD = HIGH	I_{CC1}	–	60	82	μA
Microphone inputs MIC−, MIC+ (pins 8, 9)						
Input impedance:						
differential		Z_i	51	64	77	kΩ
single-ended		Z_i	25.5	32.0	38.5	kΩ

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Common mode rejection ratio		CMRR	–	82	–	dB
Voltage gain (see Fig. 22)	I_{line} = 15 mA; R7 = 68 kΩ	G_v	51	52	53	dB
Variation of G_v with frequency, referred to 0.8 kHz	f = 300 and 3400 Hz	$\Delta G_v/\Delta f$	−0.5	± 0.1	+ 0.5	dB
Variation of G_v with temperature, referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta G_v/\Delta T$	–	± 0.2	–	dB
DTMF input (pin 12)						
Input impedance		Z_i	16.8	20.7	24.6	kΩ
Voltage gain (see Fig. 22)	I_{line} = 15 mA; R7 = 68 kΩ	G_v	25	26	27	dB
Variation of G_v with frequency, referred to 0.8 kHz	f = 300 and 3400 Hz	$\Delta G_v/\Delta f$	−0.5	± 0.1	+ 0.5	dB
	f = 697 and 1633 Hz	$\Delta G_v/\Delta f$	−0.2	± 0.05	+ 0.2	dB
Variation of G_v with temperature, referred to 25 °C	I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta G_v/\Delta T$	–	± 0.2	0.5	dB
Gain adjustment inputs GAS1, GAS2 (pins 2, 3)						
Transmitting amplifier, gain adjustment range		ΔG_v	−8	–	+ 0	dB
Sending amplifier output LN (pin 1)						
Dynamic limiter						
Output voltage swing (peak-to-peak value)	I_{line} = 15 mA; R7 = 68 kΩ; I_p = 0 mA; $V_{i(rms)}$ = 3.6 mV	$V_{LN(p-p)}$	3.6	4.0	4.5	V
Total harmonic distortion	V_i = 3.6 mV + 10 dB	THD	–	1.5	2.0	%
	V_i = 3.6 mV + 15 dB	THD	–	2.8	10.0	%
Output voltage swing (peak-to-peak value)	V_i = 3.6 mV + 10 dB					
	I_p = 2 mA	$V_{LN(p-p)}$	3.7	3.95	4.2	V
	I_p = 4 mA	$V_{LN(p-p)}$	3.0	3.25	3.5	V
	I_p = 0 mA; I_{line} = 7 mA	$V_{LN(p-p)}$	–	2	–	V
	I_p = 0 mA; I_{line} = 4 mA	$V_{LN(p-p)}$	–	1	–	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
LN output (continued)						
Dynamic behaviour of limiter	C16 = 470 nF					
attack time, V_{mic} jumps from 2 mV to 40 mV		t_{att}	–	1.5	5.0	ms
release time, V_{mic} jumps from 40 mV to 2 mV		t_{rel}	50	150	–	ms
Noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	–72	–	dBmp
Receiving amplifier input IR (pin 13)						
Input impedance		Z_i	17	21	25	kΩ
Receiving amplifier outputs QR– QR+ (pins 4, 5)						
Output impedance	single-ended	Z_o	–	4	–	Ω
Voltage gain	Fig. 23; I_{line} = 15 mA; R4 = 100 kΩ					
single-ended; R_T = 300 Ω		G_v	30	31	32	dB
differential; R_T = 600 Ω		G_v	36	37	38	dB
Variation with frequency, referred to 0.8 kHz	f = 300 and 3400 Hz	$\Delta G_v/\Delta f$	–0.5	–0.2	0	dB
Variation with temperature, referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = –25 to +75 °C	$\Delta G_v/\Delta T$	–	± 0.2	–	dB
Output voltage (RMS value)	THD = 2%; sinewave drive; R4 = 100 kΩ; I_{line} = 15 mA					
single-ended; R_T = 150 Ω	I_p = 0 mA	$V_{o(rms)}$	*	0.22	–	V
	I_p = 2 mA	$V_{o(rms)}$	*	0.35	–	V
differential; R_T = 450 Ω	I_p = 0 mA	$V_{o(rms)}$	*	0.39	–	V
	I_p = 2 mA	$V_{o(rms)}$	*	0.64	–	V
differential; C_T = 47 nF; (100 Ω series resistor); f = 3400 Hz	I_p = 0 mA	$V_{o(rms)}$	*	0.57	–	V
	I_p = 2 mA	$V_{o(rms)}$	*	0.9	–	V

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output voltage (RMS value)	I_p = 0 mA; THD = 10%; sinewave drive; R4 = 100 kΩ; single-ended; R_T = 150 Ω;					
	I_{line} = 4 mA	$V_{o(rms)}$	–	25	–	mV
	I_{line} = 7 mA	$V_{o(rms)}$	–	160	–	mV
Noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; psophometrically weighted (P53 curve); pin IR open					
	single-ended; R_T = 300 Ω	$V_{no(rms)}$	–	45	–	μV
	differential; R_T = 600 Ω	$V_{no(rms)}$	–	90	–	μV
Noise output voltage (RMS value)	in circuit of Fig. 23; S1 in position 2; 200 Ω between MIC+ and MIC−; single-ended; R_T = 300 Ω					
	R7 = 68 kΩ	$V_{no(rms)}$	–	100	–	μV
	R7 = 24.9 kΩ	$V_{no(rms)}$	–	65	–	μV
Gain adjustment input GAR (pin 6)						
Receiving amplifier, gain adjustment range		ΔG_v	−11	–	+8	dB
MUTE INPUT (pin 14)						
Input voltage HIGH		V_{IH}	1.5 + V_{SLPE}	–	V_{CC1} + 0.4	V
Input voltage LOW		V_{IL}	0	–	0.3 + V_{SLPE}	V
Input current		I_{mute}	–	11	20	μA
Change of microphone amplifier gain at mute-ON	MUTE = HIGH	$-\Delta G_v$	–	100	–	dB
Voltage gain from input DTMF-SLPE to QR+ output with mute-ON	MUTE = HIGH; single-ended load; R_L = 300 Ω	G_v	–	−18	–	dB

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Power-down input PD (pin 15)						
Input voltage HIGH		V_{IH}	1.5 + V_{SLPE}	–	V_{CC1} + 0.4	V
Input voltage LOW		V_{IL}	0	–	0.3 + V_{SLPE}	V
Input current		I_{PD}	–	5	10	μA
Automatic gain control input AGC (pin 18)						
Controlling the gain from IR (pin 13) to QR+, QR– (pins 4, 5) and the gain from MIC+, MIC– (pins 8, 9) to LN (pin 1)	R6 = 93.1 kΩ (between pins 18 and 11)					
gain control range with respect to I_{line} = 15 mA	I_{line} = 75 mA	$-G_v$	5.7	6.1	6.5	dB
Highest line current for maximum gain		I_{line}	–	24	–	mA
Lowest line current for minimum gain		I_{line}	–	61	–	mA
Change of gain between I_{line} = 15 and 35 mA		$-\Delta G_v$	0.9	1.4	1.9	dB
Microphone mute input DLS/$\overline{\text{MMUTE}}$ (pin 7)						
Input voltage low		V_{IL}	V_{EE}	–	V_{EE} + 0.3	V
Input current at low input voltage		I_{IL}	–85	–60	–35	μA
Release time after a low level on pin 7	C16 = 470 nF	t_{rel}	–	30	–	ms
Change of microphone amplifier gain at low input voltage on pin 7		$-\Delta G_v$	–	100	–	dB

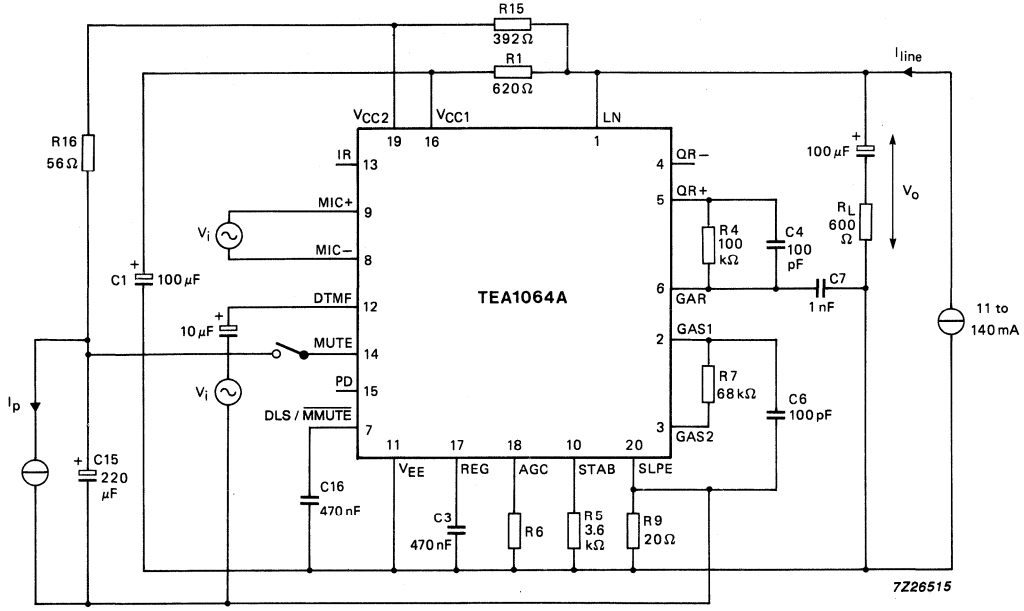


Fig. 22 Test circuit for defining voltage gain of MIC−, MIC+ and DTMF inputs; voltage gain (G_V) is defined as 20 log$|V_o/V_i|$. For measuring the gain from MIC+ and MIC− the MUTE input should be LOW or open-circuit; for measuring the DTMF input, the MUTE input should be HIGH. Inputs not being tested should be open-circuit.

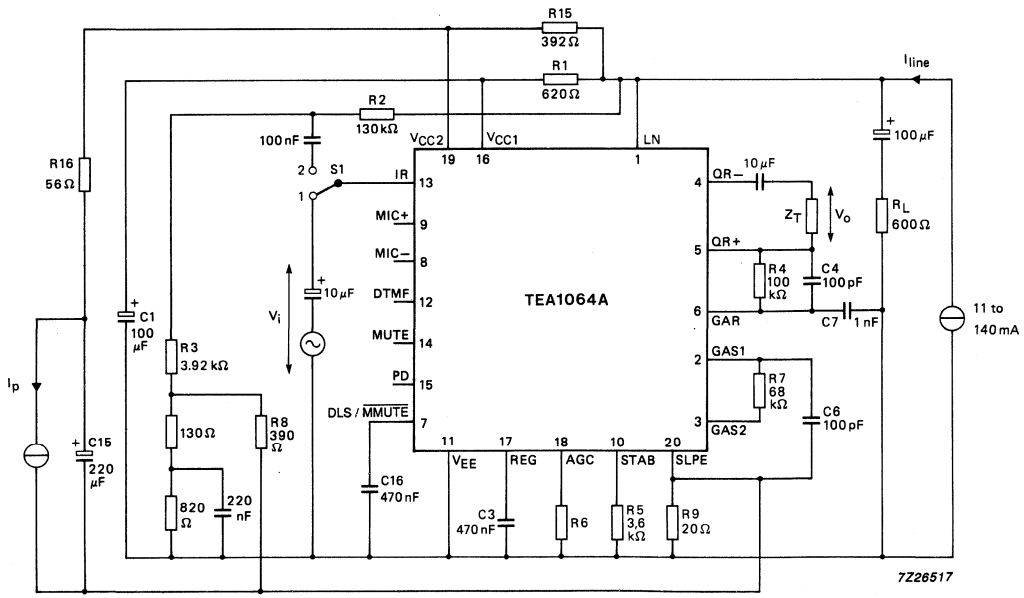


Fig. 23 Test circuit for defining voltage gain of the receiving amplifier, voltage gain (G_V) is defined as 20 log$|V_o/V_i|$ (with S1 in position 1).

APPLICATION INFORMATION

The basic application circuit is shown in Fig. 24 and some typical applications are shown in Figs 25, 26 and 27.

In the basic application, the circuit provides two possibilities for supplies to peripheral circuits:

- regulated line voltage V_{LN} (stabilized $V_{LN\text{-}SLPE}$) and unregulated supply voltage for peripheral circuits, the supply voltage is dependent only on the peripheral supply current. This application is the same as that used for TEA1060/TEA1061, TEA1067 and TEA1068;
- stabilized supply voltage for peripherals ($V_{CC2\text{-}SLPE}$), the DC line voltage depends on the current flowing to the peripheral circuits.

APPLICATION INFORMATION (continued)

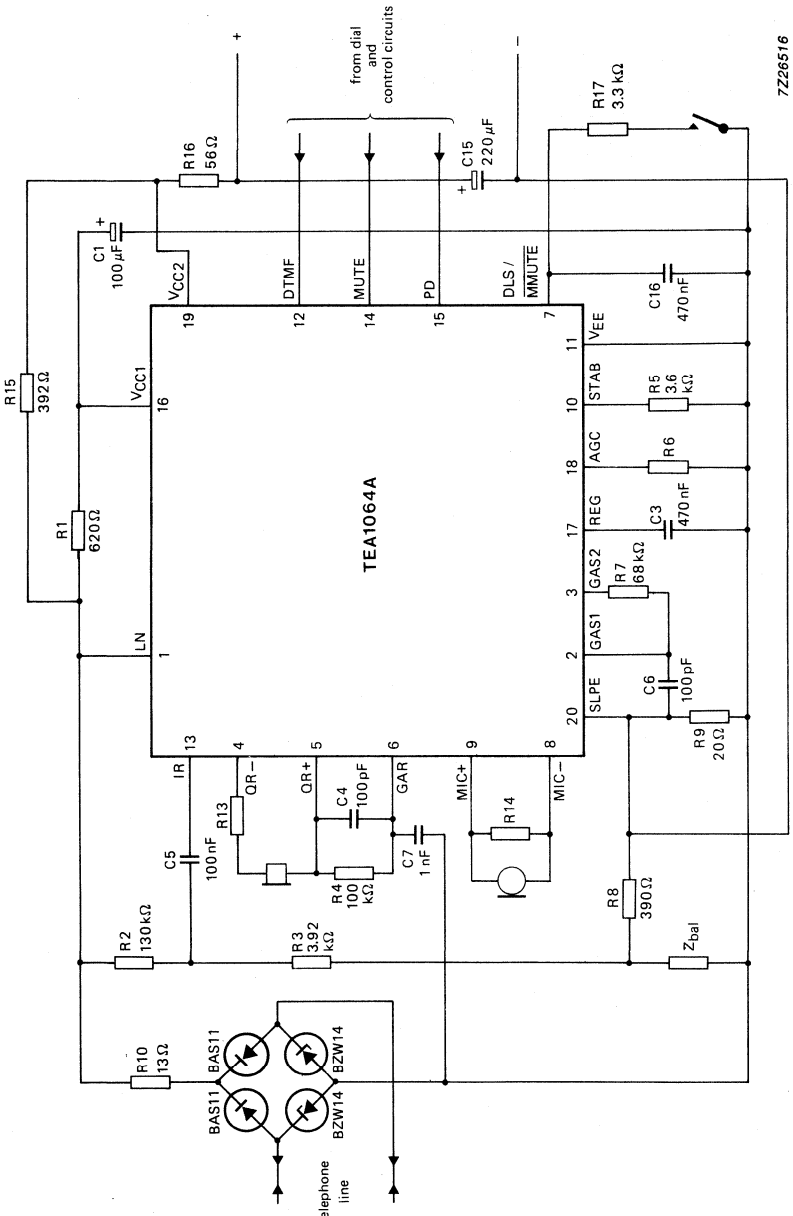


Fig. 24 Basic application of the TEA1064A with stabilized supply for peripherals, shown here with a piezo-electric earpiece and DTMF dialling. The diode bridge and R10 limit the current into, and the voltage across, the circuit during line transients. A different protection arrangement is required for pulse dialling or register recall.

For the basic application giving regulated line voltage the above circuit is changed as follows:

– R15 must be short-circuited;
– the value of R16 is changed to 392 Ω;
– the value of C3 is changed to 4.7 μF.

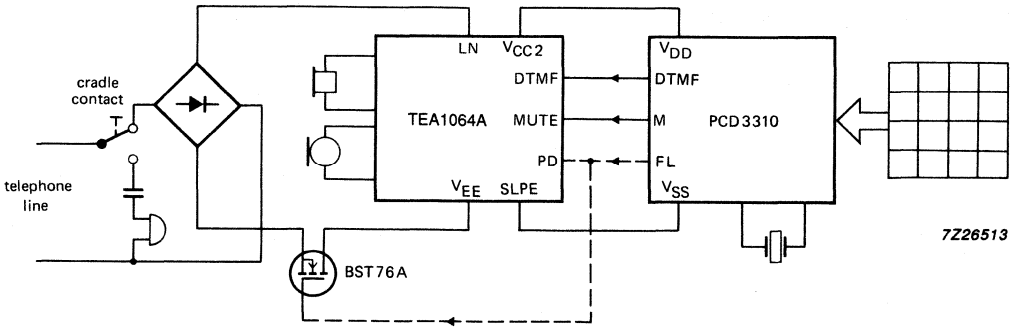


Fig. 25 Typical DTMF-pulse set application circuit (simplified) showing the TEA1064A with the CMOS bilingual dialling circuit PCD3310; the broken line indicates optional flash (register recall by timed loop break).

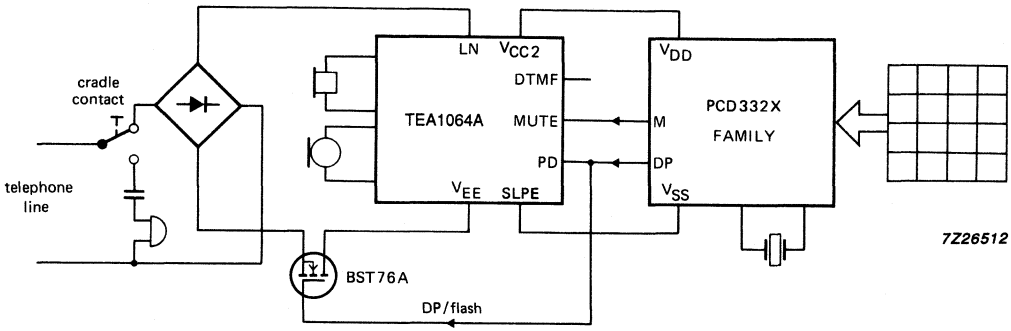


Fig. 26 Typical pulse dial set application circuit (simplified) showing the TEA1064A with one of the PCD332X family of CMOS interrupted current-loop dialling circuits.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

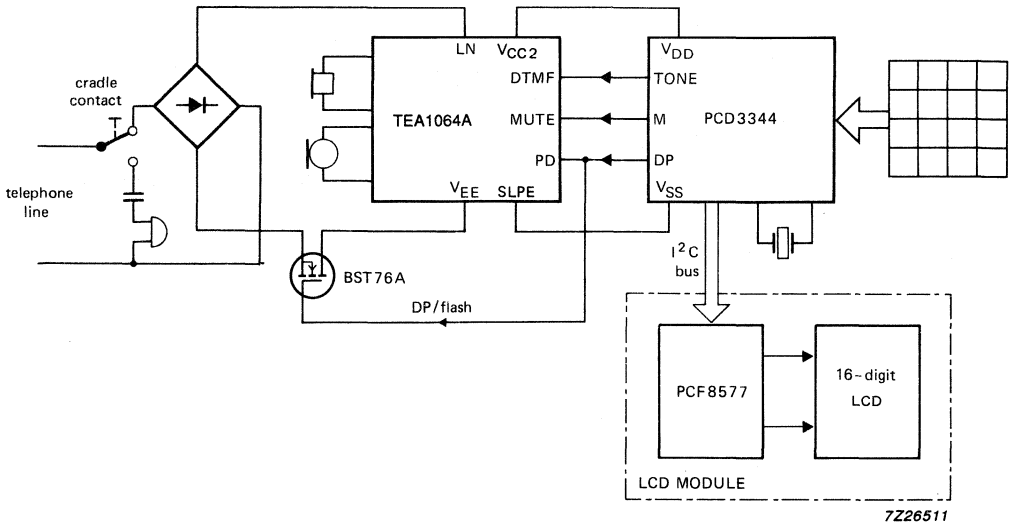


Fig. 27 Typical dual-standard (pulse and DTMF) feature phone application circuit (simplified) showing the TEA1064A and the PCD3344 CMOS telephone microcontroller with on-chip DTMF generator plus I^2C-bus.

VERSATILE TELEPHONE TRANSMISSION CIRCUIT WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1066T is a bipolar integrated circuit which performs all speech and line interface functions that are required in fully electronic telephone sets. The circuit performs electronic switching between dialling and speech.

Features

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical low-impedance inputs for dynamic and magnetic microphones
- Symmetrical high-impedance inputs for piezoelectric microphone
- Asymmetrical high-impedance input for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent (microphone and earpiece amplifiers)
- Gain control adaptable to exchange supply
- DC line voltage adjustment facility

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Line voltage	I_{line} = 15 mA	V_{LN}	4.25	4.45	4.65	V
Line current operating range		I_{line}	10	–	100	mA
Internal supply current						
power down input LOW		I_{CC}	–	0.96	1.3	mA
power down input HIGH		I_{CC}	–	55	82	μA
Supply voltage for peripherals	I_{line} = 15 mA; MUTE input HIGH					
	I_p = 1.2 mA	V_{CC}	2.8	3.05	–	V
	I_p = 1.7 mA	V_{CC}	2.5	–	–	V
Voltage gain range for microphone amplifier						
Low impedance inputs (pins 9 and 7)		G_v	44	–	60	dB
High impedance inputs (pins 10 and 8)		G_v	30	–	46	dB
Receiving amplifier		G_v	17	–	39	dB
Line loss compensation						
Gain control range		ΔG_v	5.5	5.9	6.3	dB
Exchange supply voltage range		V_{exch}	24	–	60	V
Exchange feeding bridge resistance range		R_{exch}	400	–	1000	Ω
Operating ambient temperature range		T_{amb}	–25	–	+ 75	°C

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).

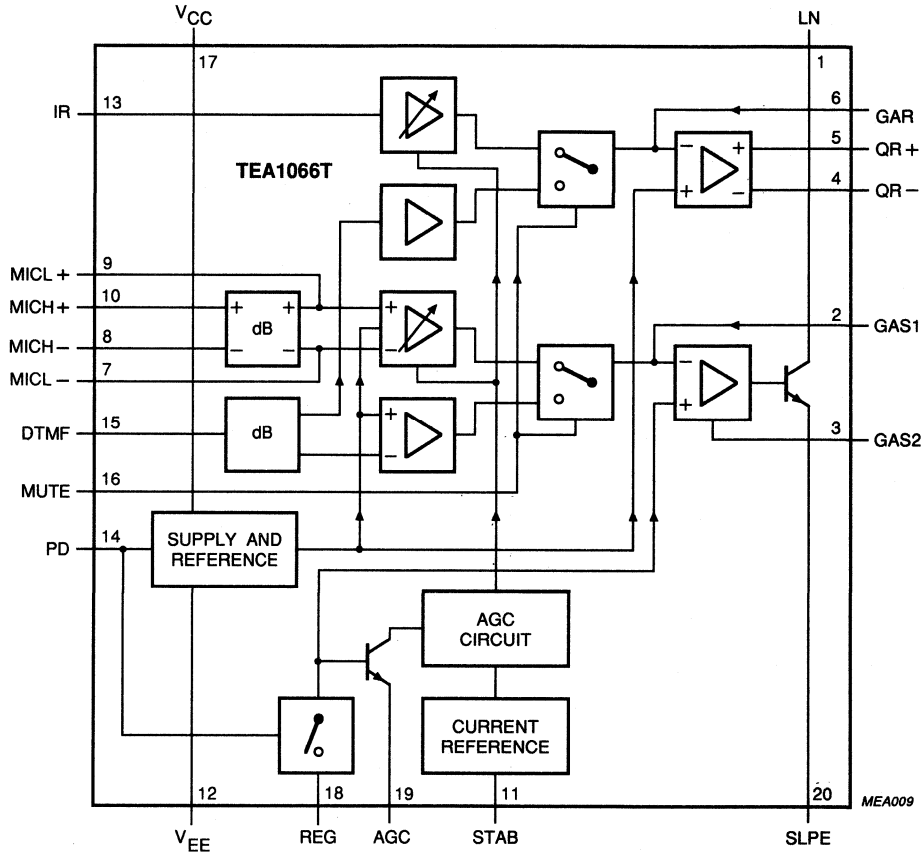


Fig. 1 Block diagram.

The blocks marked "dB" are attenuators.

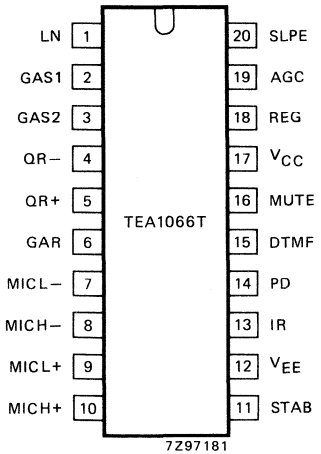


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAS1	gain adjustment transmitting amplifier
3	GAS2	gain adjustment transmitting amplifier
4	QR−	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment receiving amplifier
7	MICL−	inverting microphone input, low impedance
8	MICH−	inverting microphone input, high impedance
9	MICL+	non-inverting microphone input, low impedance
10	MICH+	non-inverting microphone input, high impedance
11	STAB	current stabilizer
12	V_{EE}	negative line terminal
13	IR	receiving amplifier input
14	PD	power-down input
15	DTMF	dual-tone multi-frequency input
16	MUTE	mute input
17	V_{CC}	positive supply decoupling
18	REG	voltage regulator decoupling
19	AGC	automatic gain control input
20	SLPE	slope (DC resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

Power for the TEA1066T and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g. dialling and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3.6 kΩ between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the DC resistance of the subscriber line R_{line} and the DC voltage on the subscriber set (see Fig. 7).

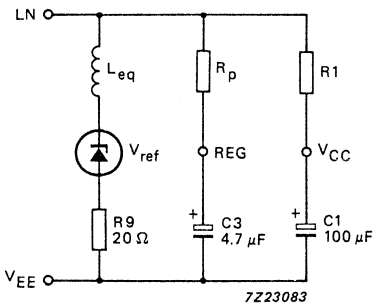
If the line current I_{line} exceeds the current I_{CC} + 0.5 mA required by the circuit itself, about 1 mA, plus the current I_p required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:
$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0.5 \times 10^{-3}\text{A} - I_p) \times R9$, where V_{ref} is an internally generated temperature compensated reference voltage of 4,2 V and R9 being an external resistor connected between SLPE and V_{EE}. The preferred value for R9 is 20 Ω. Changing R9 will have influence on microphone gain, DTMF gain, gain control characteristics, side-tone level and maximum output swing on LN.

FUNCTIONAL DESCRIPTION (continued)

Under normal conditions $I_{SLPE} \geqslant I_{CC} + 0.5$ mA + I_P. The static behaviour of the circuit then equals a 4.2 V voltage regulator diode with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1 (see Fig. 3). The internal reference voltage can be adjusted by means of an external resistor R_{VA}. This R_{VA} connected between LN and REG (pins 1 and 18) will decrease the internal reference voltage. R_{VA} connected between REG and SLPE (pins 18 and 20) will increase the internal reference voltage.

Current I_P, available from V_{CC} for supplying peripheral circuits, depends on external components and on the line current. Fig. 8 shows this current for $V_{CC} > 2.2$ V and > 3 V (being the minimum supply voltage for most CMOS circuits including voltage drop for an enable diode). If MUTE is LOW the available current is further reduced when the receiving amplifier is driven.



$R_p = 17.5\ k\Omega$
$L_{eq} = C3 \times R9 \times R_p$

Fig. 3 Equivalent impedance circuit.

Microphone inputs MICL+, MICH+, MICL− and MICH− and amplification adjustment connections GAS1 and GAS2

The TEA1066T has symmetrical microphone inputs. The MICL+ and MICL− inputs are intended for low-sensitivity, low-impedance dynamic or magnetic microphones. Input impedance is 8.2 kΩ (2 x 4.1 kΩ) and its voltage gain is typ. 52 dB. The MICH+ and MICH− inputs are intended for a piezoelectric microphone or an electret microphone with built-in FET source follower. Its input impedance is 40.8 kΩ (2 x 20.4 kΩ) and its voltage gain is typical 38 dB. The arrangements with the microphone types mentioned are shown in Fig. 9.

The gain of the microphone amplifier in both types can be adjusted over a range of ± 8 dB to suit the sensitivity of the transducer used. The gain is proportional to external resistor R7 connected between GAS1 and GAS2.

An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 x C6.

Mute input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier; a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the earpiece outputs and on the line.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typ. 25.5 dB and varies with R7 in the same way as the gain of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR−. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig. 10). Gain from IR to QR+ is typ. 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB and differential drive becomes possible. This feature can be used in case the earpiece impedance exceeds 450 Ω (high-impedance dynamic, magnetic or piezo-electric earpieces.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and RMS value is higher.

The gain of the receiving amplifier can be adjusted over a range of ± 8 dB to suit the sensitivity of the transducer used. The gain is proportional to external resistor R4 connected from GAR to QR+.

Two external capacitors C4 = 100 pF and C6 = 10 x C4 = 1 nF are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order, low-pass filter. The "cut-off" frequency corresponds with the time constant R4 x C4.

Automatic amplification control input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 6 dB. This corresponds with a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 11 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range.

If automatic line loss compensation is not required AGC may be left open. The amplifiers then all give their maximum gain as specified.

Power-down input PD

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, as a consequence it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input during the time of the loop break, which reduces the supply current from typ. 1 mA to typ. 55 μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall.
When this facility is not required PD may be left open.

FUNCTIONAL DESCRIPTION (continued)

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of $R1//Z_{line}$, R2, R3, R8, R9 and Z_{bal} (see Fig. 14). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9.R2 = R1(R3 + [R8//Z_{bal}])$

b) $[Z_{bal}/(Z_{bal} + R8)] = [Z_{line}/(Z_{line} + R1)]$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) will always be fulfilled provided that $|R8//Z_{bal}| < R3$.
To obtain optimum side tone suppression, condition b) has to be fulfilled resulting in:

$$Z_{bal} = (R8/R1)\, Z_{line} = k.Z_{line}$$

where k is a scale factor; $k = (R8/R1)$.

Scale factor k (value of R8) must be chosen to meet the following criteria:
- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| \ll R3$
- $|Z_{bal}+R8| \gg R9$

In practice Z_{line} varies strongly with line length and cable type; consequently an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal}/k equals the average line impedance.

Example

The balanced line impedance $|Z_{bal}|$ at which the optimum suppression is preset can be calculated by: suppose $Z_{line} = 210\ \Omega + (1265\ \Omega/140\ nF)$, representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).
When k = 0.64 then R8 = 390 Ω; $Z_{bal} = 130\ \Omega + (820\ \Omega//220\ nF)$.

The anti-sidetone network for the TEA1060 family shown in Fig. 4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. Fig. 5 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances.

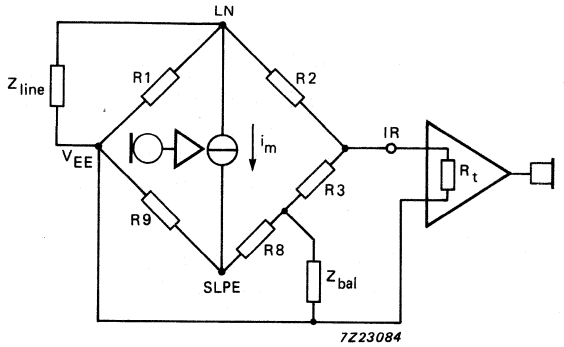


Fig. 4 Equivalent circuit of TEA1060 family anti-sidetone bridge.

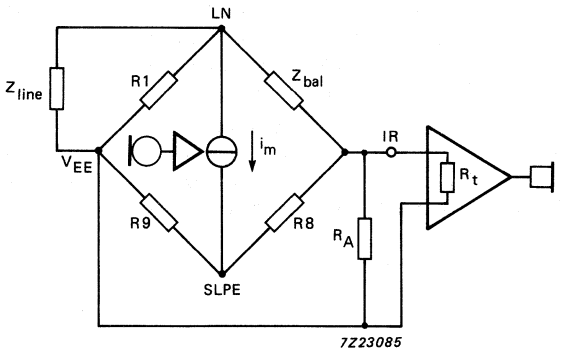


Fig. 5 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

FUNCTIONAL DESCRIPTION (continued)

The anti-sidetone network as used in the standard application (Fig. 13) attenuates the signal from the line with 32 dB. The attenuation is nearly flat over the audio-frequency range.
Instead of the above described special TEA1066 bridge, the conventional Wheatstone bridge configuration can be used as an alternative anti-sidetone circuit. Both bridge types can be used with either a resistive set impedance or with a complex set impedance.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive line voltage continuous		V_{LN}	–	12	V
Repetitive line voltage during switch-on or line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω (Fig. 10)	V_{LN}	–	28	V
Line current (1)	R9 = 20 Ω	I_{line}	–	140	mA
Voltage on all other pins		V_i	–	V_{CC} + 0.7	V
		$-V_i$	–	0.7	V
Total power dissipation (2)	R9 = 20 Ω	P_{tot}	–	555	mW
Storage temperature range		T_{stg}	−40	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

Notes to the ratings

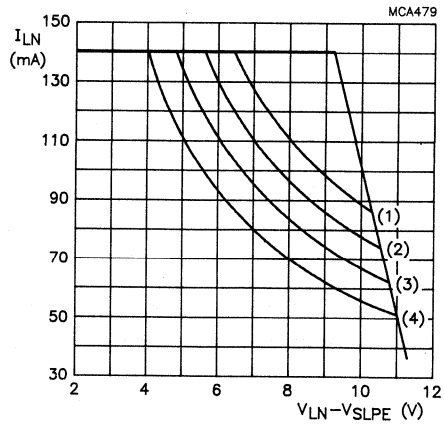
(1) Mostly dependent on the maximum required T_{amb} and the voltage between LN and SLPE (see Fig. 6).

(2) Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

From junction to ambient in free air

TEA1066T mounted on glass epoxy board 41 x 19 x 1.5 mm $R_{th\ j\text{-}a}$ = 90 K/W



	T_{amb}	P_{tot}
(1)	45 °C	888
(2)	55 °C	777
(3)	65 °C	666
(4)	75 °C	555

Fig. 6 Safe operating area.

CHARACTERISTICS

I_{line} = 10 to 100 mA; V_{EE} = 0 V; f = 800 Hz; R9 = 20 Ω; T_{amb} = 25 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 17)						
Voltage drop over circuit	I_{line} = 5 mA	V_{LN}	3.95	4.25	4.55	V
	I_{line} = 15 mA	V_{LN}	4.25	4.45	4.65	V
	I_{line} = 100 mA	V_{LN}	5.40	6.10	6.70	V
	I_{line} = 140 mA	V_{LN}	–	–	7.50	V
Voltage drop variation with temperature	I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	−4	−2	0	mV/K
Voltage drop over circuit	I_{line} = 15 mA; R_{VA} = R1-18 = 68 kΩ	V_{LN}	3.50	3.80	4.05	V
	R_{VA} = R18-20 = 39 kΩ	V_{LN}	4.70	5.0	5.30	V
Supply current (pin 17)						
PD (pin 14) = LOW	V_{CC} = 2.8 V	I_{CC}	–	0.96	1.3	mA
PD (pin 14) = HIGH	V_{CC} = 2.8 V	I_{CC}	–	55	82	μA
Supply voltage available for peripheral circuits	I_{line} = 15 mA; MUTE = HIGH					
	I_P = 0 mA	V_{CC}	3.5	3.75	–	V
	I_P = 1.2 mA	V_{CC}	2.8	3.05	–	V
Microphone inputs MICL+ and MICL−; MICH+ and MICH−						
Input impedance						
MICL+ (pin 9); MICL− (pin 7)		$\|Z_i\|$	3.3	4.1	4.9	kΩ
MICH+ (pin 10); MICH− (pin 8)		$\|Z_i\|$	16.5	20.4	24.5	kΩ
Common-mode rejection ratio		k_{CMR}	–	82	–	dB
Voltage gain	I_{line} = 15 mA; R7 = 68 kΩ					
MICL+/MICL− to LN		G_v	51	52	53	dB
MICH+/MICH− to LN		G_v	37	38	39	dB
gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	−0.5	±0.2	+ 0.5	dB
gain variation with temperature at T_{amb} = −25 °C and + 75 °C	I_{line} = 50 mA; w.r.t. 800 Hz	ΔG_{vT}	–	±0.2	–	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Dual-tone multi-frequency input DTMF (pin 15)						
Input impedance		$\|Z_i\|$	16.8	20.7	24.6	kΩ
Voltage gain from DTMF to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	24.5	25.5	26.5	dB
gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	−0.5	±0.2	+ 0.5	dB
gain variation with temperature at T_{amb} = −25 °C and + 75 °C	I_{line} = 50 mA; w.r.t. 25 °C	ΔG_{vT}	−	±0.2	−	dB
Gain adjustment connections GAS1 and GAS2 (pins 2 and 3)						
Gain variation with R7, transmitting amplifier		ΔG_v	−8	−	+ 8	dB
Transmitting amplifier output LN (pin 1)						
Output voltage	I_{line} = 15 mA; THD = 2%	$V_{LN(rms)}$	1.9	2.3	−	V
	THD = 10%	$V_{LN(rms)}$	−	2.6	−	V
Noise output voltage	I_{line} = 15 mA; R7 = 68 kΩ; microphone inputs open psophometrically weighted (P53 curve)	$V_{no(rms)}$	−	−70	−	dBmp
Receiving amplifier input IR (pin 13)						
Input impedance		$\|Z_i\|$	17	21	25	kΩ
Receiving amplifier outputs QR+ and QR− (pins 5 and 4)						
Output impedance	single-ended	$\|Z_o\|$	−	4	−	Ω
Voltage gain from IR to QR+ or QR−	I_{line} = 15 mA; R4 = 100 kΩ; single-ended R_L = 300 Ω	G_v	24	25	26	dB
	differential R_L = 600 Ω	G_v	30	31	32	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	−0.5	±0.2	+ 0.5	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Receiving amplifier outputs QR+ and QR− (continued)						
Gain variation with temperature at T_{amb} = −25 °C and + 75 °C	I_{line} = 50 mA; w.r.t. 25 °C	ΔG_{vT}	−	±0.2	−	dB
Output voltage	I_P = 0 mA; I_{line} = 15 mA; THD = 2%;					
sine-wave drive	R4 = 100 kΩ					
single-ended	R_L = 150 Ω	$V_{o(rms)}$	0.30	0.38	−	V
	R_L = 450 Ω	$V_{o(rms)}$	0.4	0.52	−	V
differential	C_L = 47 nF R series = 100 Ω; f = 3400 Hz	$V_{o(rms)}$	0.8	1.0	−	V
Noise output voltage	I_{line} = 15 mA; R4 = 100 kΩ; pin 13 (IR) open psophometrically weighted (P53 curve)					
single-ended	R_L = 300 Ω	$V_{no(rms)}$	−	50	−	μV
differential	R_L = 600 Ω	$V_{no(rms)}$	−	100	−	μV
Gain adjustment GAR (pin 6)						
Gain variation with R4 connected between pin 6 and pin 5 receiving amplifier		ΔG_v	−8	−	+ 8	dB
MUTE input (pin 16)						
Input voltage HIGH		V_{IH}	1.5	−	V_{CC}	V
Input voltage LOW		V_{IL}	−	−	0.3	V
Input current		I_{MUTE}	−	5	10	μA
Reduction of voltage gain from MICL+ (pin 9) and MICL− (pin 7) to LN (pin 1)	MUTE = HIGH	ΔG_v	−	70	−	dB
Voltage gain from DTMF to QR+ or QR−	MUTE = HIGH; R4 = 100 kΩ					
single-ended	R_L = 300 Ω	G_v	−21	−19	−17	dB
Power-down input PD (pin 14)						
Input voltage HIGH		V_{IH}	1.5	−	V_{CC}	V
Input voltage LOW		V_{IL}	−	−	0.3	V
Input current		I_{PD}	−	5	10	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Automatic gain control input AGC (pin 19)						
Gain control range from IR to QR+/QR− and from MIC+/MIC− to LN; R6 = 110 kΩ between AGC and V_{EE}						
Gain control range	I_{line} = 70 mA	$-\Delta G_v$	−5.5	−5.9	−6.3	dB
Highest line current for maximum gain	I_{line}	–	–	23	–	mA
Lowest line current for minimum gain	I_{line}	–	–	61	–	mA
Reduction of gain between I_{line} = 15 mA and I_{line} = 35 mA		$-\Delta G_v$	−1.0	−1.5	−2.0	dB

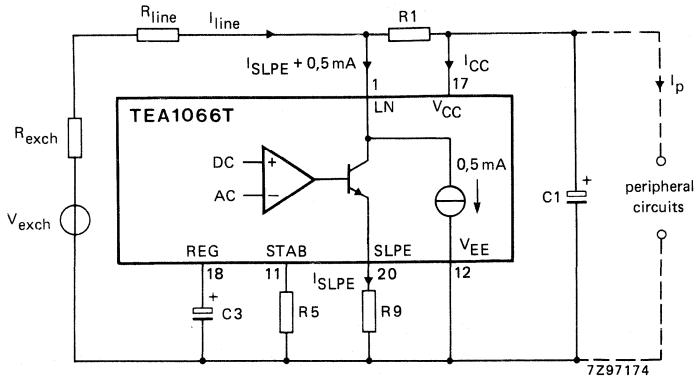


Fig. 7 Supply arrangement.

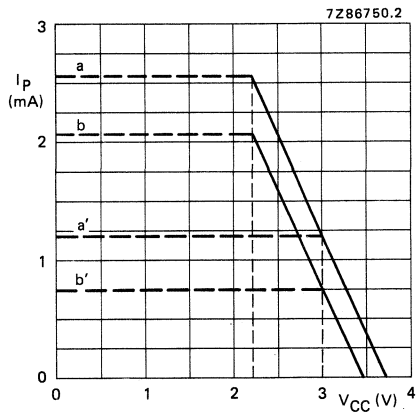


Fig. 8 Typicalmum current I_P available from V_{CC} for external (peripheral) circuitry with $V_{CC} > 2.2$ V and $V_{CC} > 3$ V. Curves (a) and (a') are valid when the receiving amplifier is not driven or when MUTE = HIGH, curves (b) and (b') are valid when MUTE = LOW and the receiving amplifier is driven, $V_{o(rms)} = 150$ mV, $R_L = 150\ \Omega$ (asymmetrical).
$I_{line} = 15$ mA; $V_{LN} = 4.45$ V; R1 = 620 Ω and R9 = 20 Ω.
(a) = 2.55 mA; (b) = 2.1 mA; (a') = 1.2 mA and (b') = 0.75 mA.

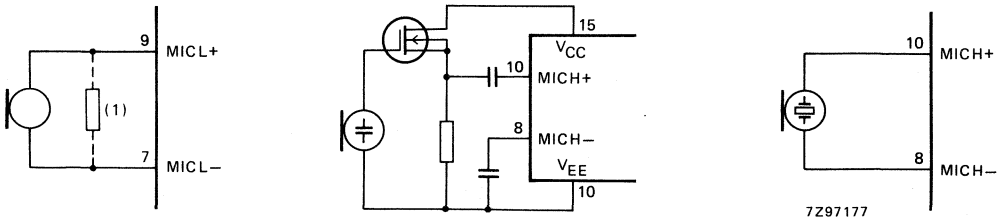


Fig. 9 Alternative microphone arrangements. (a) magnetic or dynamic microphone. The resistor marked (1) may be connected to lower the terminating impedance. (b) electret microphone, (c) piezo-electric microphone.

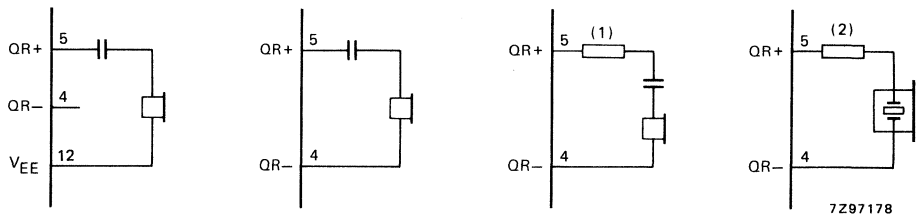


Fig. 10 Alternative receiver arrangements. (a) dynamic earpiece with less than 450 Ω impedance. (b) dynamic earpiece with more than 450 Ω impedance. (c) magnetic earpiece with more than 450 Ω impedance. The resistor marked (1) may be connected to prevent distortion (inductive load). (d) piezoelectric earpiece. The resistor marked (2) is required to increase the phase margin (capacitive load).

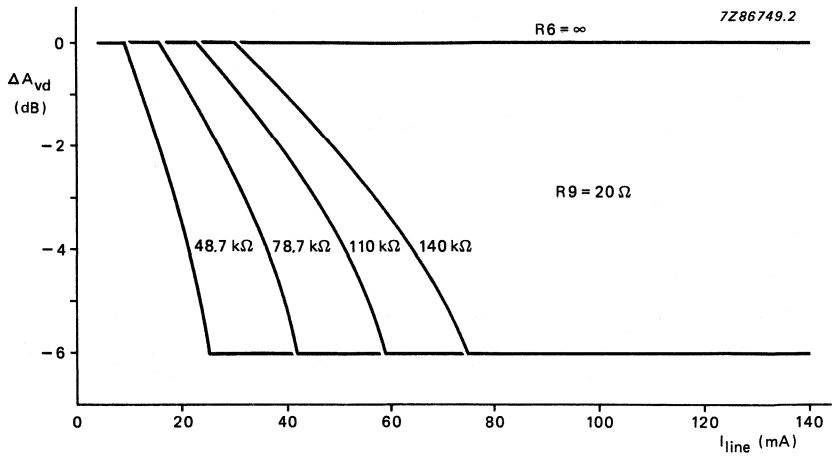


Fig. 11 Variation of gain with line current, with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}; R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	24	61.9	48.7	X	X
	36	100	78.7	68	60.4
	48	140	110	93.1	82
	60	X	X	120	102

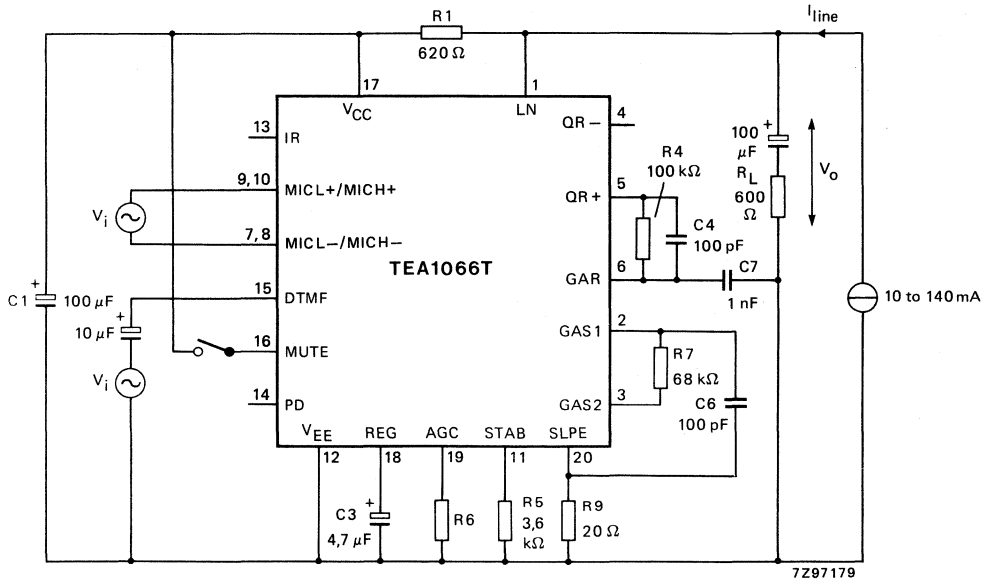


Fig. 12 Test circuit for defining voltage gain of MICL+, MICL−, MICH+ and MICH− DTMF inputs. Voltage gain is defined as: $G_v = 20 \log |V_o/V_i|$. For measuring the gain from MICL+, MICL− or MICH+ and MICH− the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

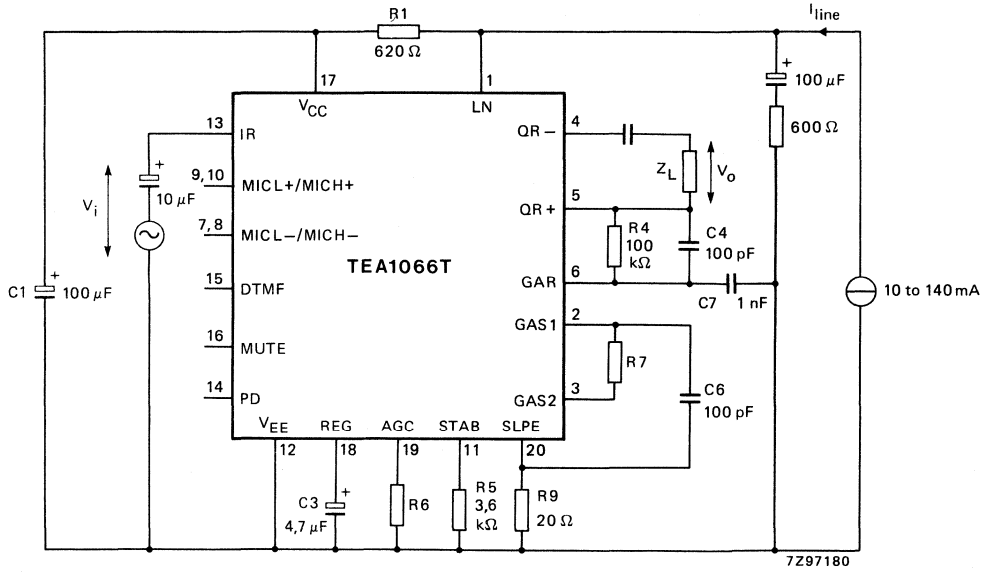


Fig. 13 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as: $G_v = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

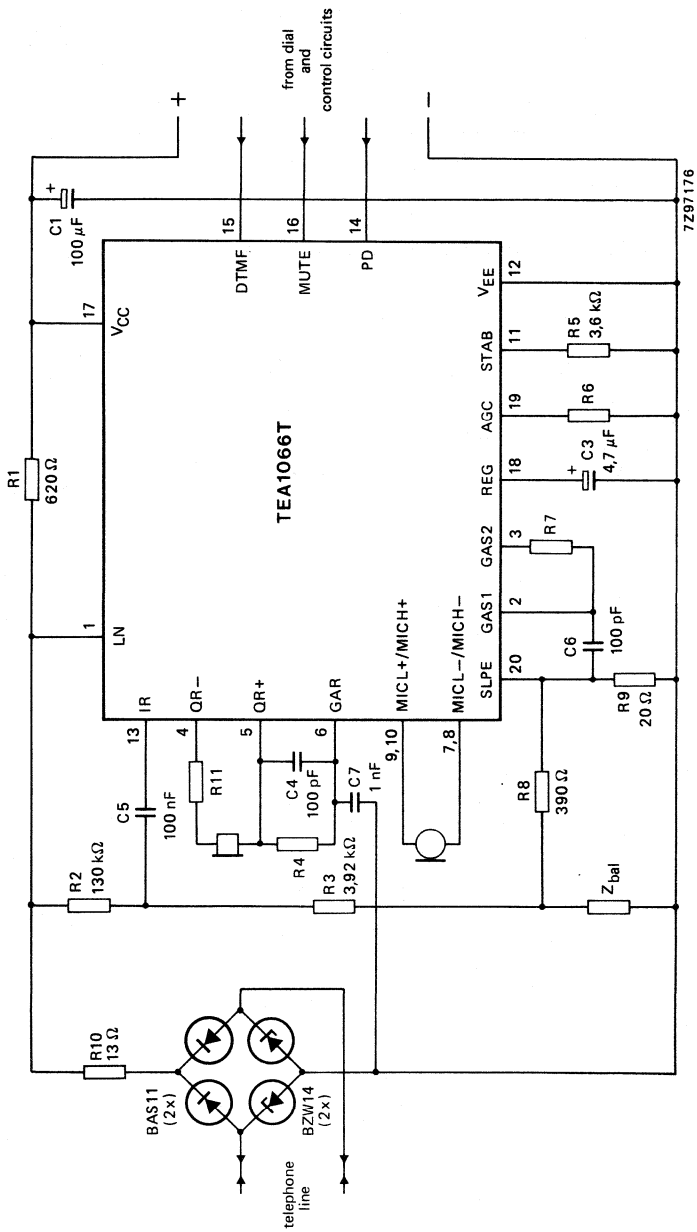
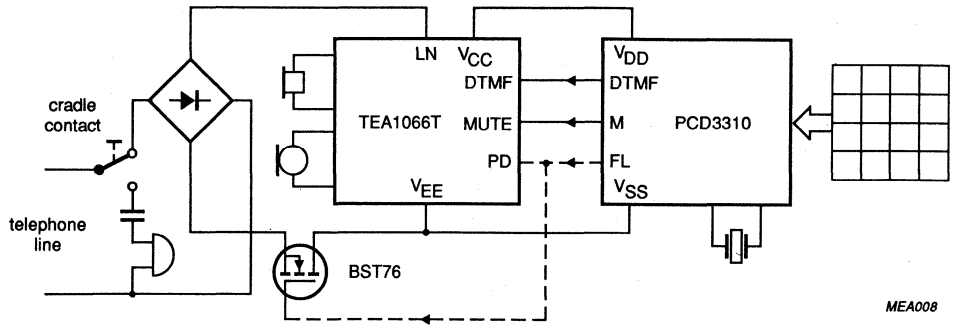
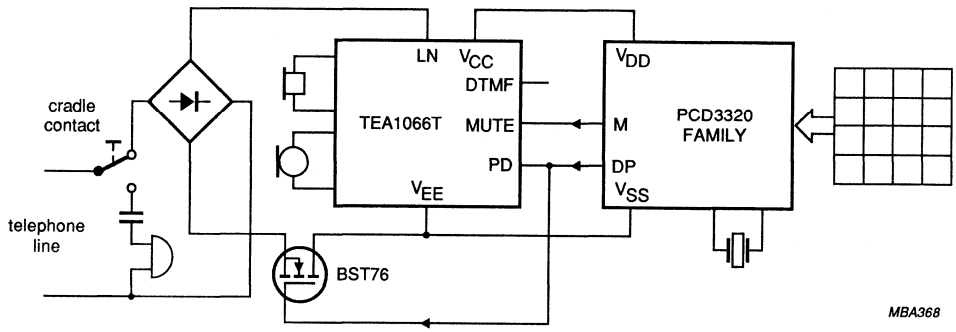


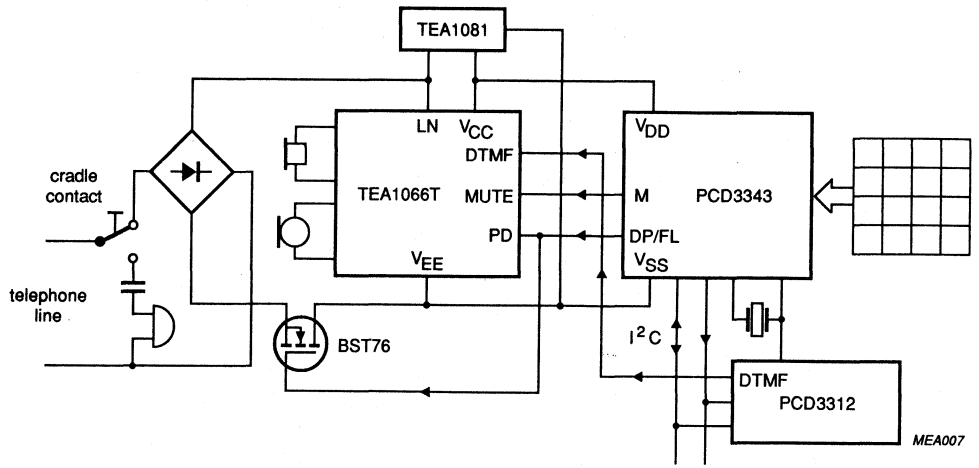
Fig. 14 Typical application of the TEA1066T, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.



(a)



(b)



(c)

Fig.15 Typical applications of the TEA1066T (simplified).

(a) DTMF pulse set with CMOS PCD3310 dialling circuit. The dashed lines show an optional flash (register recall by timed loop break).

(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.

(c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C-bus. Supply is provided by the TEA1081 supply circuit.

LOW VOLTAGE VERSATILE TELEPHONE TRANSMISSION CIRCUIT WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1067 is a bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech. The circuit is able to operate down to a DC line voltage of 1.6 V (with reduced performance) to facilitate the use of more telephone sets in parallel.

Features

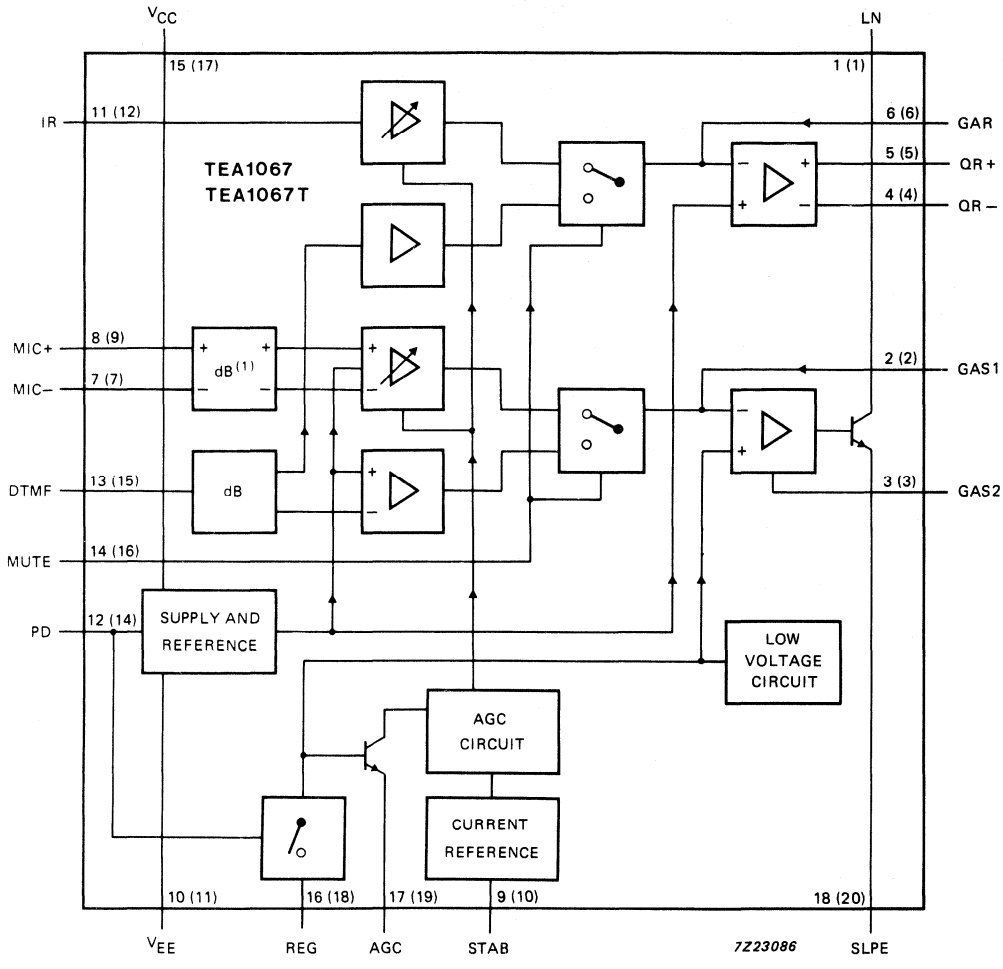
- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable static resistance
- Provides supply with limited current for external circuitry
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezoelectric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line current dependent line loss compensation facility for microphone and earpiece amplifiers
- Gain control adaptable to exchange supply
- DC line voltage adjustment capability

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Line voltage	I_{line} = 15 mA	V_{LN}	3.65	3.9	4.15	V
Line current operating range	normal operation					
	TEA1067	I_{line}	11	–	140	mA
	TEA1067T	I_{line}	11	–	140	mA
	with reduced performance	I_{line}	1	–	11	mA
Internal supply current	power down					
	input LOW	I_{CC}	-	1	1.35	mA
	input HIGH	I_{CC}	–	55	82	μA
Supply voltage for peripherals	I_{line} = 15 mA; I_p = 1.4 mA; mute input HIGH	V_{CC}	2.2	2.4	–	V
	I_{line} = 15 mA; I_p = 0.9 mA; mute input HIGH	V_{CC}	2.5	–	–	V
Voltage gain range						
microphone amplifier		G_v	44	–	52	dB
receiving amplifier		G_v	20	–	45	dB
Line loss compensation gain control range		ΔG_v	5.5	5.9	6.3	dB
Exchange supply voltage range		V_{exch}	36	–	60	V
Exchange feeding bridge resistance range		R_{exch}	0.4	–	1	kΩ

PACKAGE OUTLINES

TEA1067: 18-lead DIL; plastic (SOT102).
TEA1067T: 20-lead mini-pack: plastic (SO20; SOT163A).



Figures in parenthesis refer to TEA1067T.

Fig. 1 Block diagram.

PINNING

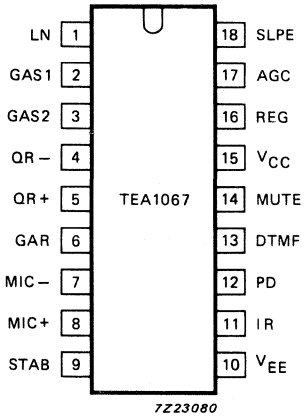


Fig. 2 (a) Pinning diagram for TEA1067 18-lead DIL version.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (DC resistance) adjustment

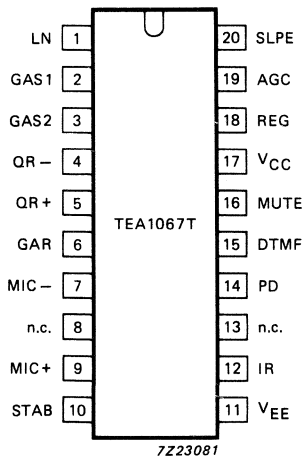


Fig. 2 (b) Pinning diagram for TEA1067T 20-lead mini-pack version.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment, receiving amplifier
7	MIC–	inverting microphone input
8	n.c.	not connected
9	MIC+	non-inverting microphone input
10	STAB	current stabilizer
11	V_{EE}	negative line terminal
12	IR	receiving amplifier input
13	n.c.	not connected
14	PD	power-down input
15	DTMF	dual-tone multi-frequency input
16	MUTE	mute input
17	V_{CC}	positive supply decoupling
18	REG	voltage regulator decoupling
19	AGC	automatic gain control input
20	SLPE	slope (DC resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

Power for the TEA1067 and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external circuits e.g. dialling and control circuits.

Decoupling of the supply voltage is performed by a capacitor between V_{CC} and V_{EE} while the internal voltage regulator is decoupled by a capacitor between REG and V_{EE}.

The DC current drawn by the device will vary in accordance with varying values of the exchange voltage (V_{exch}), the feeding bridge resistance, (R_{exch}) and the DC resistance of the telephone line (R_{line}).

The TEA1067 has an internal current stabilizer working at a level determined by a 3.6 kΩ resistor connected between STAB and V_{EE} (see Fig. 6). When the line current (I_{line}) is more than 0.5 mA greater than the sum of the IC supply current (I_{CC}) and the current drawn by the peripheral circuitry connected to V_{CC} (I_p) the excess current is shunted to V_{EE} via LN.
The regulated voltage on the line terminal (V_{LN}) can be calculated as:

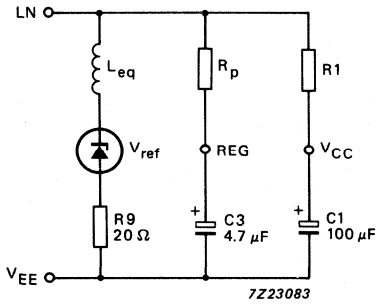
$$V_{LN} = V_{ref} + I_{SLPE} \times R9; \text{ or } V_{LN} = V_{ref} + [(I_{line} - I_{CC} - 0.5 \times 10^{-3}\,A) - I_p] \times R9$$

Where V_{ref} is an internally generated temperature compensated reference voltage of 3.6 V and R9 is an external resistor connected between SLPE and V_{EE}. In normal use the value of R9 would be 20 Ω. Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics, side-tone level and maximum output swing on LN, and the DC characteristics (especially at the lower voltages).

Under normal conditions, when $I_{SLPE} \gg I_{CC} + 0.5\ mA + I_p$, the static behaviour of the circuit is that of a 3.6 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1. Fig. 3 shows the equivalent impedance of the circuit.

At line currents below 9 mA the internal reference voltage is automatically adjusted to a lower value (typically 1.6 V at 1 mA). This means that the operation of more sets in parallel is possible with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. With line currents below 9 mA the circuit has limited sending and receiving levels. The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor connected between LN and REG will decrease the internal reference voltage, connected between REG and SLPE it will increase the internal reference voltage.

Current (I_p) available from V_{CC} for peripheral circuits depends on the external components used. Fig. 9 shows this current for $V_{CC} > 2.2$ V. If MUTE is LOW when the receiving amplifier is driven the available current is further reduced. Current availability can be increased by connecting the supply IC (TEA1081) in parallel with R1, as shown in Fig. 16 (c), or by increasing the DC line voltage by means of an external resistor (R_{VA}) connected between REG and SLPE.



$R_p = 16.2\ k\Omega$
$L_{eq} = C3 \times R9 \times R_p$

Fig. 3 Equivalent impedance circuit.

Microphone inputs (MIC+ and MIC−) and gain adjustment pins (GAS1 and GAS2)

The TEA1067 has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage gain is typically 52 dB (when R7 = 68 kΩ, see Fig. 13). Dynamic, magnetic, piezoelectric or electret (with built-in FET source followers) microphones can be used. Microphone arrangements are shown in Fig. 10.

The gain of the microphone amplifier can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer in use. The gain is proportional to the value of R7 which is connected between GAS1 and GAS2. Stability is ensured by the external capacitor C6 which is connected between GAS1 and SLPE. The value of C6 is 100 pF but this may be increased to obtain a first-order low-pass filter. The cut-off frequency corresponds to the time constant R7 x C6.

Mute input (MUTE)

When MUTE is HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when MUTE is LOW or open-circuit. MUTE switching causes only negligible clicking on the earpiece outputs and line. If the number of parallel sets in use causes a drop in line current to below 6 mA the speech amplifiers remain active independent to the DC level applied to the MUTE input.

Dual-tone multi-frequency input (DTMF)

When the DTMF input is enabled dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the microphone gain. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving Amplifier (IR, QR+, QR− and GAR)

The receiving amplifier has one input (IR), one non-inverting complementary output (QR+) and an inverting complementary output (QR−). These outputs may be used for single-ended or differential drive depending on the sensitivity and type of earpiece used (see Fig. 11). IR to QR + gain is typically 31 dB (when R4 = 100 kΩ), this is sufficient for low-impedance magnetic or dynamic microphones which are suited for single-ended drive. Using both outputs for differential drive gives an additional gain of 6 dB. This feature can be used when the earpiece impedance exceeds 450 Ω (high-impedance dynamic or piezoelectric types).

FUNCTIONAL DESCRIPTION (continued)

Receiving Amplifier (IR, QR+, QR− and GAR) (continued)

The receiving amplifier gain can be adjusted between 20 and 39 dB with single-ended drive and between 26 and 45 dB with differential drive, to match the sensitivity of the transducer in use. The gain is set with the value of R4 which is connected between GAR and QR+. Overall receive gain between LN and QR+ is calculated by substracting the anti-sidetone network attenuation (32 dB) from the amplifier gain. Two external capacitors C4 and C7, ensure stability. C4 is normally 100 pF and C7 is 10 x the value of C4. The value of C4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant R4 x C4.
The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.

Automatic gain control input (AGC)

Automatic line loss compensation is achieved by connecting a resistor (R6) between AGC and V_{EE}. The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 5.9 dB. This corresponds to a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation 1.2 dB/km. Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 12 and Table 1). The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line loss compensation is required the AGC may be left open-circuit. The amplifiers, in this condition, will give their maximum specified gain.

Power-down input (PD)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted. During these interruptions the telephone line provides no power for the transmission circuit or circuits supplied by V_{CC}. The charge held on C1 will bridge these gaps. This bridging is made easier by a HIGH level on the PD input which reduces the typical supply current from 1 mA to 55 μA and switches off the voltage regulator preventing discharge through LN. When PD is HIGH the capacitor at REG is disconnected with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required PD may be left open-circuit.

Side-tone suppression

The anti-sidetone network, $R1//Z_{line}$, R2, R3, R9 and Z_{bal}, (see Fig. 4) suppresses transmitted signal in the earpiece. Compensation is maximum when the following conditions are fulfilled:

(a) $R9 \times R2 = R1\ (R3 + [R8//Z_{bal}])$;

(b) $(Z_{bal}/[Z_{bal} + R8]) = (Z_{line}/[Z_{line} + R1])$

If fixed values are chosen for R1, R2, R3, and R9 then condition (a) will always be fulfilled when $|R8//Z_{bal}| \ll R3$. To obtain optimum side-tone suppression condition (b) has to be fulfilled resulting in:

$Z_{bal} = (R8/R1)\ Z_{line} = k.Z_{line}$ where k is a scale factor; $k = (R8/R1)$

The scale factor (k), dependent on the value of R8, is chosen to meet the following criteria:

(a) Compatability with a standard capacitor from the E6 or E12 range for Z_{bal}

(b) $|Z_{bal}//R8| \ll R3$ to fulfill condition (a) and thus ensuring correct anti-sidetone bridge operation

(c) $|Z_{bal} + R8| \gg R9$ to avoid influencing the transmitter gain

In practice Z_{line} varies considerably with the line type and length. The value chosen for Z_{bal} should therefore be for an average line length thus giving optimum setting for short or long lines.

Example

The line balance impedance (Z_{bal}) at which the optimum suppression is present can be calculated by: suppose Z_{line} = 210 Ω + (1265 Ω/140 nF), representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).
When k = 0.64 then R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig. 4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. Fig. 5 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances.

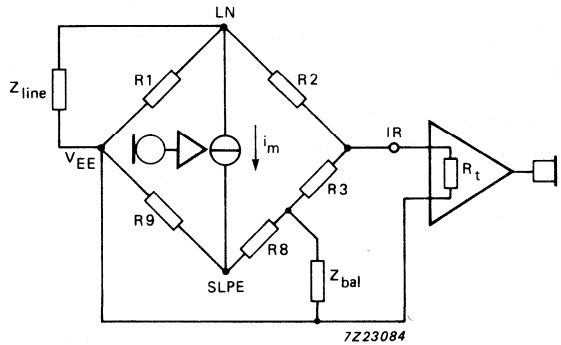


Fig. 4 Equivalent circuit of TEA1060 anti-sidetone bridge.

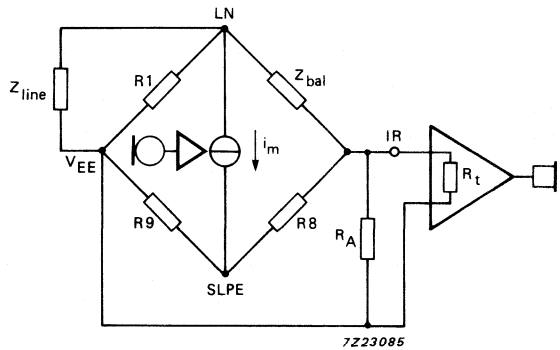


Fig. 5 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

More information can be found in the designer guide; 9398 341 10011

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive continuous line voltage		V_{LN}	–	12	V
Repetitive line voltage during switch-on line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω (Fig. 15)	V_{LN}	–	28	V
Line current TEA1067(1)	R9 = 20 Ω	I_{line}	–	140	mA
Line current TEA1067T (1)	R9 = 20 Ω	I_{line}	–	140	mA
Voltage on all other pins		V_i	–	V_{CC} + 0.7	V
		$-V_i$	–	0.7	V
Total power dissipation (2)	R9 = 20 Ω				
TEA1067		P_{tot}	–	769	mW
TEA1067T		P_{tot}	–	550	mW
Storage temperature range		T_{stg}	−40	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

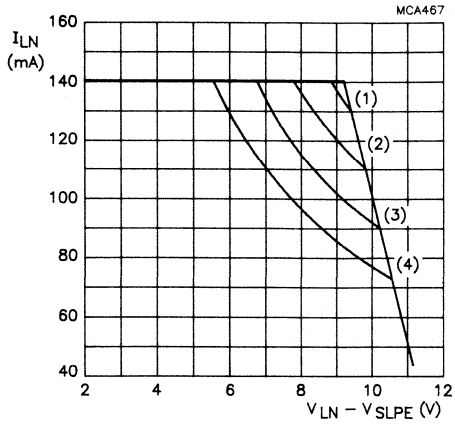
(1) Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE. See Figs 6 and 7 to determine the current as a function of the required voltage and the temperature.

(2) Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

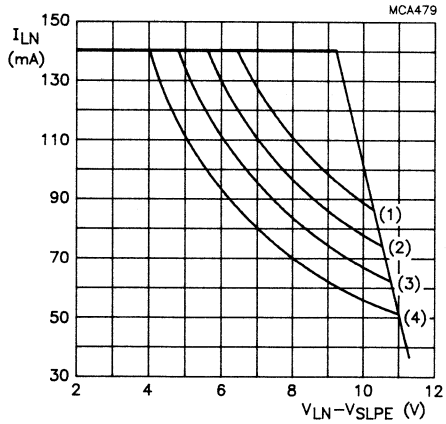
From junction to ambient in free air

TEA1067	$R_{th\ j\text{-}a}$	typ.	65	K/W
TEA1067T mounted on glass epoxy board 41 x 19 x 1.5 mm	$R_{th\ j\text{-}a}$	typ.	90	K/W



	T_{amb}	P_{tot}
(1)	45 °C	1231 mW
(2)	55 °C	1077 mW
(3)	65 °C	923 mW
(4)	75 °C	769 mW

Fig. 6 TEA1067 safe operating area.



	T_{amb}	P_{tot}
(1)	45 °C	888 mW
(2)	55 °C	777 mW
(3)	65 °C	666 mW
(4)	75 °C	555 mW

Fig. 7 TEA1067T safe operating area.

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Supply; LN and V_{CC}						
Voltage drop over circuit, between LN and V_{EE}	microphone inputs open					
	I_{line} = 1 mA	V_{LN}	–	1.6	–	V
	I_{line} = 4 mA	V_{LN}	1.75	2.0	2.25	V
	I_{line} = 7 mA	V_{LN}	2.25	2.8	3.35	V
	I_{line} = 11 mA	V_{LN}	3.55	3.8	4.05	V
	I_{line} = 15 mA	V_{LN}	3.65	3.9	4.15	V
	I_{line} = 100 mA	V_{LN}	4.9	5.6	6.5	V
	I_{line} = 140 mA	V_{LN}	–	–	7.5	V
Variation with temperature	I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	−3	−1	1	mV/K
Voltage drop over circuit, between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA; R_{VA} (LN to REG) = 68 kΩ		3.1	3.4	3.7	V
	I_{line} = 15 mA; R_{VA} (REG to SLPE) = 39 kΩ		4.2	4.5	4.8	V
Supply current	PD = LOW; V_{CC} = 2.8 V	I_{CC}	–	1.0	1.35	mA
Supply current	PD = HIGH; V_{CC} = 2.8 V	I_{CC}	–	55	82	μA
Supply voltage available for peripheral circuitry	I_{line} = 15 mA; MUTE = HIGH					
	I_p = 1.4 mA	V_{CC}	2.2	2.4	–	V
	I_p = 0 mA	V_{CC}	2.95	3.2	–	V
Microphone inputs MIC+ and MIC−						
Input impedance (differential) between MIC− and MIC+		$\|Z_i\|$	51	64	77	kΩ
Input impedance (single-ended) MIC− or MIC+ to V_{EE}		$\|Z_i\|$	25.5	32	38.5	kΩ
Common mode rejection ratio		k_{CMR}	–	82	–	dB
Voltage gain MIC+/MIC− to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	51	52	53	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Microphone inputs MIC+ and MIC– (continued)						
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	–0.5	± 0.2	+0.5	dB
Gain variation with temperature at –25 °C and +75 °C	w.r.t. 25 °C without R6; I_{line} = 50 mA	ΔG_{vT}	–	± 0.2	–	dB
Dual-tone multi-frequency input DTMF						
Input impedance		$\lvert Z_i \rvert$	16.8	20.7	24.6	kΩ
Voltage gain from DTMF to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	24.5	25.5	26.5	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t 800 Hz	ΔG_{vf}	–0.5	±0.2	+0.5	dB
Gain variation with temperature at –25 °C and +75 °C	w.r.t. 25 °C; I_{line} = 50 mA	ΔG_{vT}	–	±0.2	–	dB
Gain adjustment GAS1 and GAS2						
Gain variation of the transmitting amplifier by varying R7 between GAS1 and GAS2		ΔG_v	–8	–	0	dB
Sending amplifier output LN						
Output voltage	I_{line} = 15 mA; THD = 2%	$V_{LN(rms)}$	–	1.9	–	V
	I_{line} = 15 mA; THD = 10%	$V_{LN(rms)}$	1.9	2.2	–	V
	I_{line} = 4 mA; THD = 10%	$V_{LN(rms)}$	–	0.8	–	V
	I_{line} = 7 mA; THD = 10%	$V_{LN(rms)}$	–	1.4	–	V
Noise output voltage	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	–72	–	dBmp

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Receiving amplifier input IR						
Input impedance		$\|Z_i\|$	17	21	25	kΩ
Receiving amplifier outputs QR+ and QR–						
Output impedance (single-ended)		$\|Z_o\|$	–	4	–	Ω
Voltage gain from IR to QR+ or QR–	I_{line} = 15 mA R4 = 100 kΩ					
single-ended	R_L (from QR+ or QR–) = 300 Ω	G_v	30	31	32	dB
differential	R_L (from QR+ or QR–) = 600 Ω	G_v	36	37	38	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	–0.5	–0.2	0	dB
Gain variation with temperature at –25 °C and +75 °C	w.r.t. 25 °C without R6; I_{line} = 50 mA	ΔG_{vT}	–	±0.2	–	dB
Output voltage	sinewave drive I_{line} = 15 mA; I_p = 0 mA; THD = 2% R4 = 100 kΩ					
single-ended	RL = 150 Ω	$V_{o(rms)}$	0.25	0.29	–	V
	RL = 450 Ω	$V_{o(rms)}$	0.45	0.55	–	V
differential	f = 3400 Hz; series R = 100 Ω; C_L = 47 nF	$V_{o(rms)}$	0.65	0.80	–	V
Output voltage	THD = 10%; RL = 150 Ω R4 = 100 kΩ					
	I_{line} = 4 mA	$V_{o(rms)}$	–	15	–	mV
	I_{line} = 7 mA	$V_{o(rms)}$	–	130	–	mV
Noise output voltage	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted; (P53 curve)					
single-ended	RL = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential	RL = 600 Ω	$V_{no(rms)}$	–	100	–	μV

parameter	conditions	symbol	min.	typ.	max.	unit
Gain adjustment GAR						
Gain variation of receiving amplifier achievable by varying R4 between GAR and QR		ΔG_v	−11	–	+8	dB
Mute input						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{MUTE}	–	8	15	μA
Gain reduction MIC+ or MIC− to LN	MUTE = HIGH	ΔG_v	–	70	–	dB
Voltage gain from DTMF to QR+ or QR−	MUTE = HIGH; R4 = 100 kΩ; single-ended; R_L = 300 Ω	G_v	−21	−19	−17	dB
Power-down input PD						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{PD}	–	5	10	μA
Automatic gain control input AGC Controlling the gain from IR to QR+/QR− and the gain from MIC+/MIC− to LN; R6 between AGC and V_{EE}	R6 = 110 kΩ					
Gain control range	I_{line} = 70 mA	ΔG_v	−5.5	−5.9	−6.3	dB
Highest line current for maximum gain		I_{line}	–	23	–	mA
Minimum line current for minimum gain		I_{line}	–	61	–	mA
Reduction of gain between I_{line} = 15 mA and I_{line} = 35 mA		ΔG_v	−1.0	−1.5	−2.0	dB

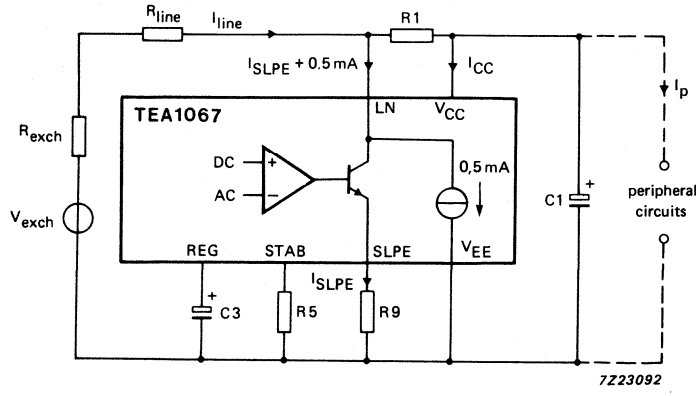
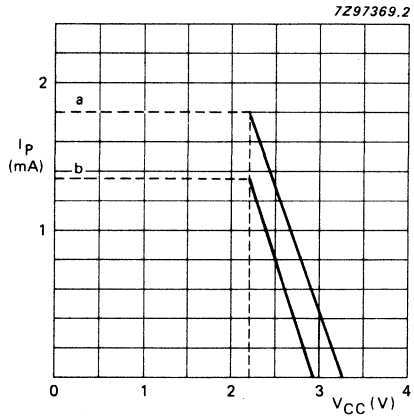


Fig. 8 Supply arrangement.



(a) I_p = 1.8 mA
(b) I_p = 1.35 mA
I_{line} = 15 mA at V_{LN} = 3.9 V
R1 = 620 Ω and R9 = 20 Ω.

Fig. 9 Typical current I_p available from V_{CC} for peripheral circuitry with $V_{CC} >= 2.2$ V. Curve (a) is valid when the receiving amplifier is not driven or when MUTE = HIGH, curve (b) is valid when MUTE = LOW and the receiving amplifier is driven; $V_{o(rms)}$ = 150 mV, R_L = 150 Ω asymmetrical.
The supply possibilities can be increased simply by setting the voltage drop over the circuit V_{LN} to a higher value by means of resistor R_{VA} connected between REG and SLPE.

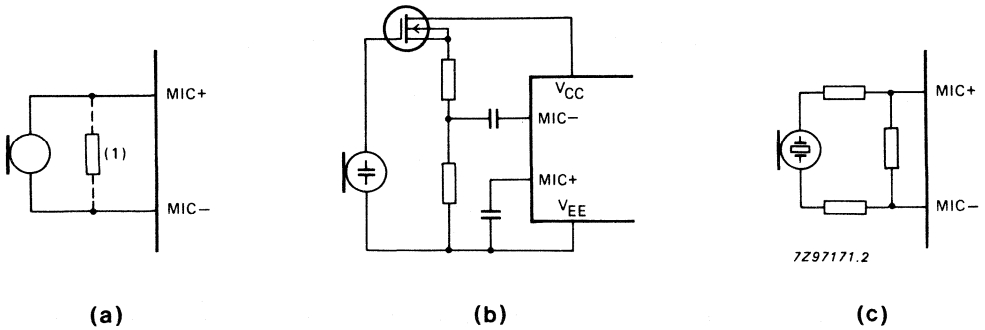


Fig. 10 Alternative microphone arrangements.

(a) Magnetic or dynamic microphone. The resistor marked (1) may be connected to decrease the terminating impedance.
(b) Electret microphone.
(c) Piezoelectric microphone.

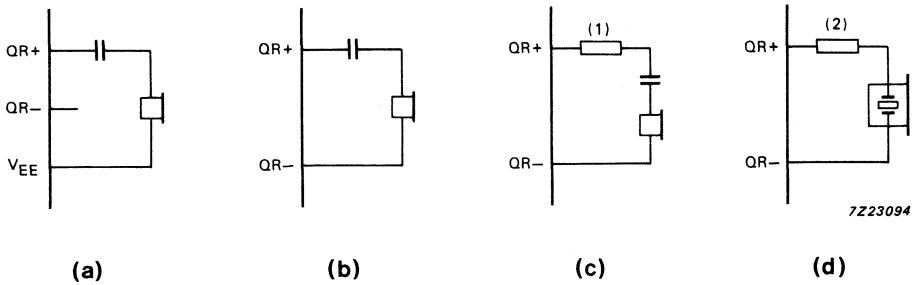


Fig. 11 Alternative receiver arrangements.

(a) Dynamic earpiece with less than 450 Ω impedance.
(b) Dynamic earpiece with more than 450 Ω impedance.
(c) Magnetic earpiece with more than 450 Ω impedance. The resistor marked (1) may be connected to prevent distortion (inductive load).
(d) Piezoelectric earpiece. The resistor marked (2) is required to increase the phase margin (capacitive load).

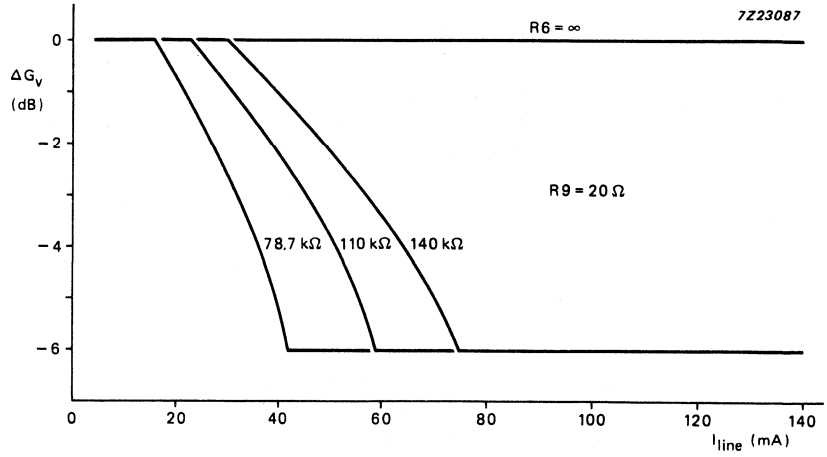


Fig. 12 Variation of gain with line current, with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	36	100	78.7	X	X
	48	140	110	93.1	82
	60	X	X	120	102

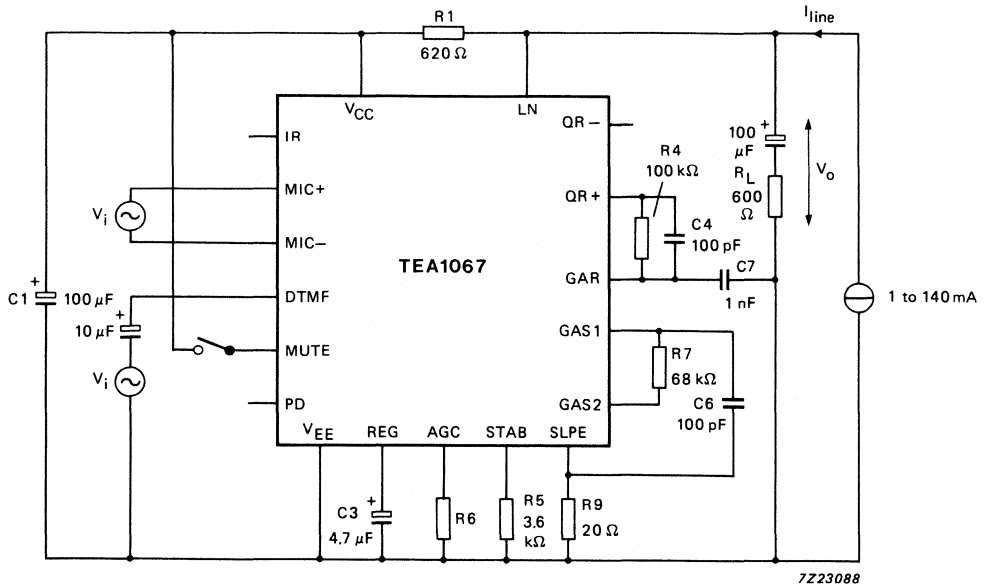


Fig. 13 Test circuit for defining voltage gain of MIC+, MIC– and DTMF inputs. Voltage gain is defined as; $G_V = 20 \log |V_o/V_i|$. For measuring the gain from MIC+ and MIC– the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

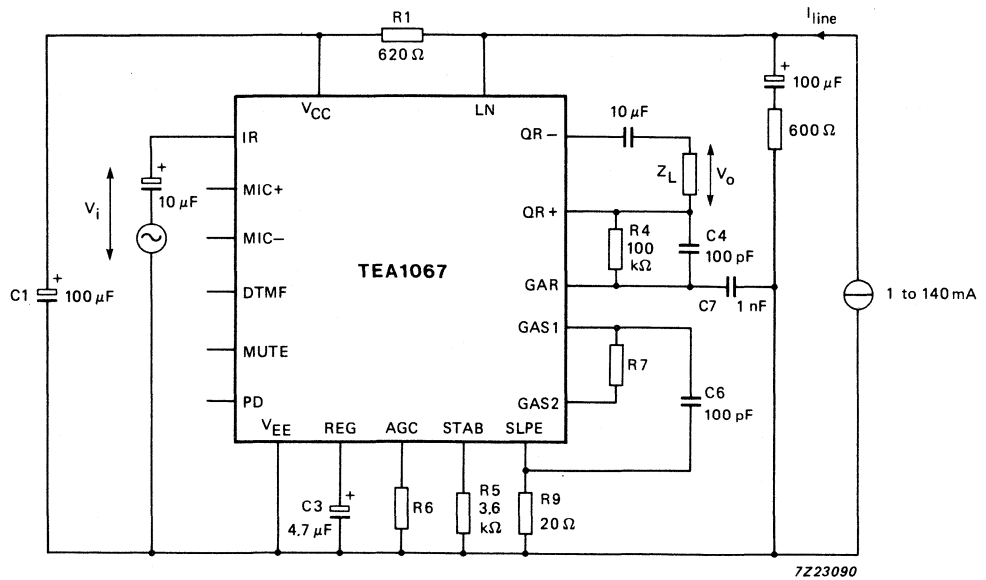


Fig. 14 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as; $G_V = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

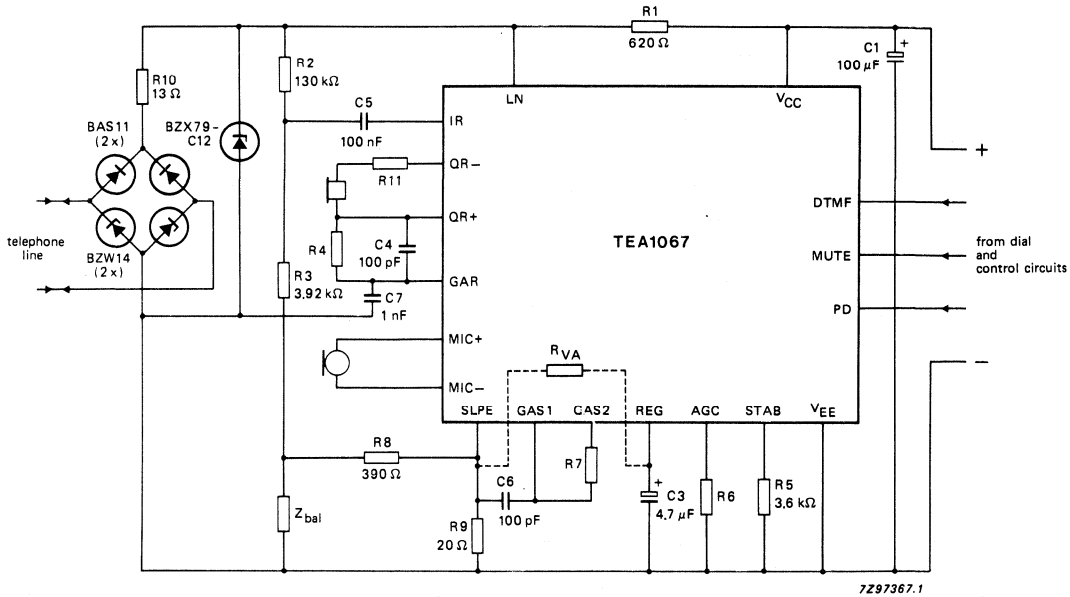


Fig. 15 Typical application of the TEA1067, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left, the zener diode and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.
The DC line voltage can be set to a higher value by the resistor R_{VA} (REG to SLPE).

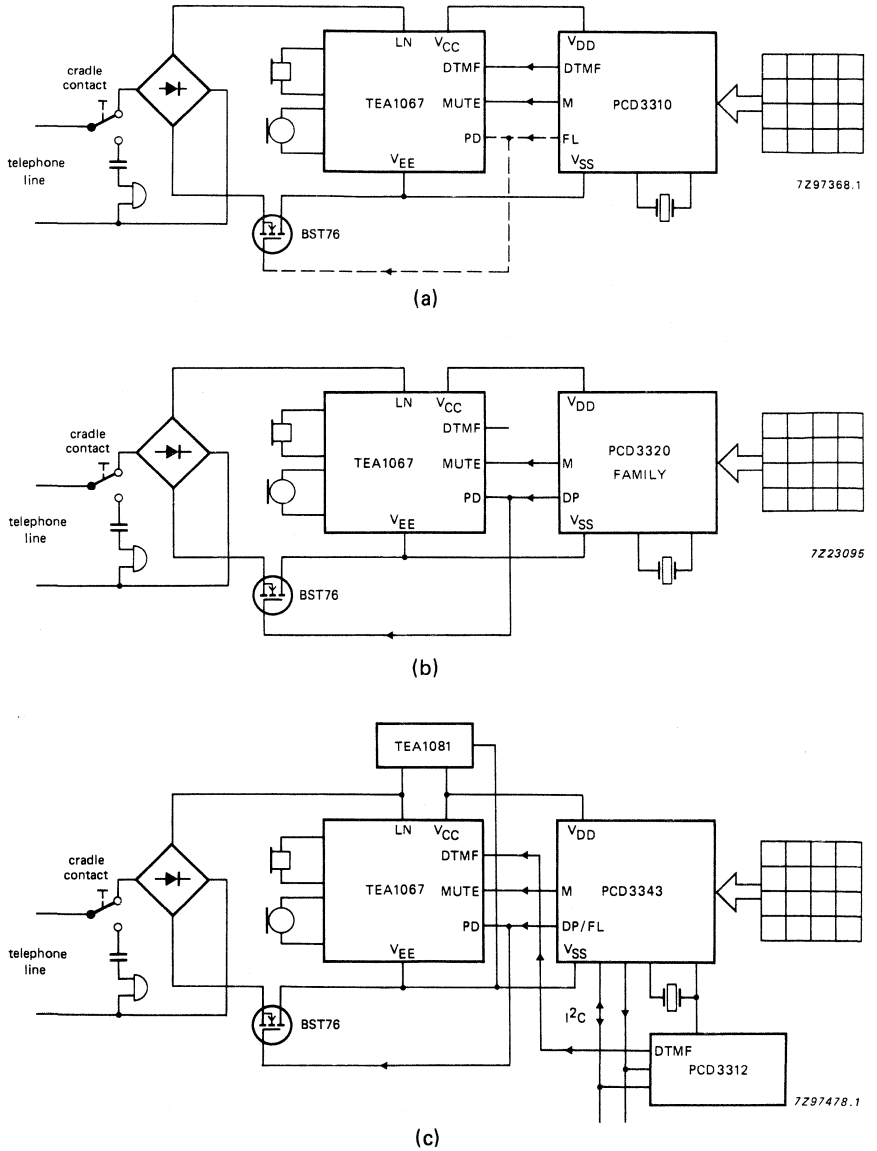


Fig. 16 Typical applications of the TEA1067 (simplified).

(a) DTMF-Pulse set with CMOS dialling circuit PCD3310.
The dashed lines show an optional flash (register recall by timed loop break).
(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.
(c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS controller and the PCD3312 CMOS DTMF generator with I^2C-bus. Supply is provided by the TEA1081 supply circuit.

VERSATILE TELEPHONE TRANSMISSION CIRCUIT WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1068 is a bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech.

Features

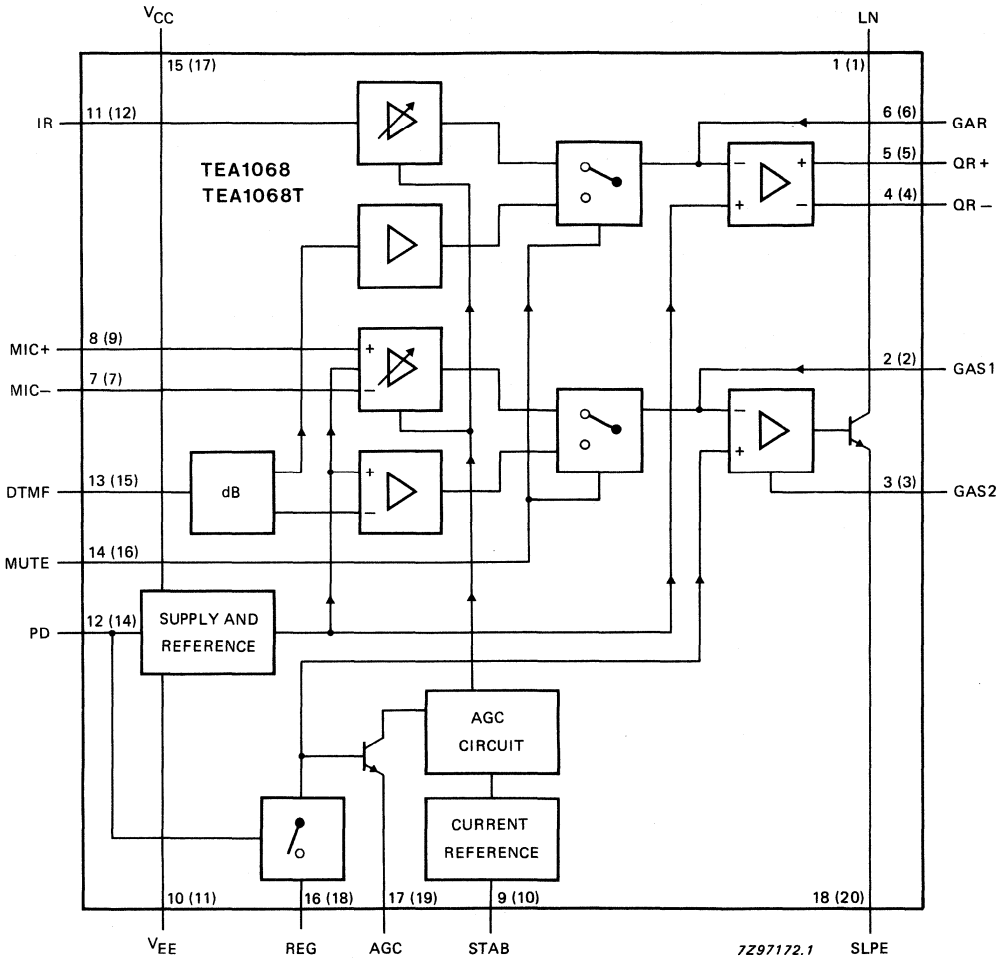
- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezoelectric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line current dependent line loss compensation facility for microphone and earpiece amplifiers
- Gain control adaptable to exchange supply
- DC line voltage adjustment capability.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Line voltage	I_{line} = 15 mA	V_{LN}	4.2	4.45	4.7	V
Line current operating range	normal operation					
	TEA1068	I_{line}	10	–	140	mA
	TEA1068T	I_{line}	10	–	100	mA
Internal supply current	power down					
	input LOW	I_{CC}	–	0.96	1.3	mA
	input HIGH	I_{CC}	–	55	82	μA
Supply voltage for peripherals	I_{line} = 15 mA; mute input HIGH					
	I_p = 1.2 mA	V_{CC}	2.8	3.05	–	V
	I_p = 1.7 mA	V_{CC}	2.5	–	–	V
Voltage gain range						
microphone amplifier		G_v	44	–	60	dB
receiving amplifier		G_v	17	–	39	dB
Line loss compensation gain control range		ΔG_v	5.5	5.9	6.3	dB
Exchange supply voltage range		V_{exch}	24	–	60	V
Exchange feeding bridge resistance range		R_{exch}	0.4	–	1	kΩ

PACKAGE OUTLINES

TEA1068: 18-lead DIL; plastic (SOT102).
TEA1068T: 20-lead mini-pack; plastic (SO20; SOT163A).



Figures in parenthesis refer to TEA1068T.

Fig. 1 Block diagram.

PINNING

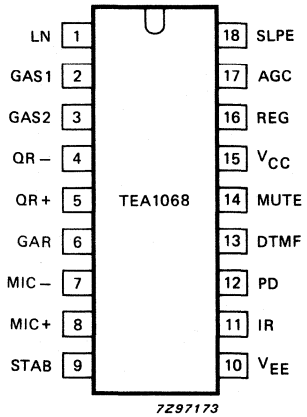


Fig. 2 (a) Pinning diagram for TEA1068 18-lead DIL version.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (DC resistance) adjustment

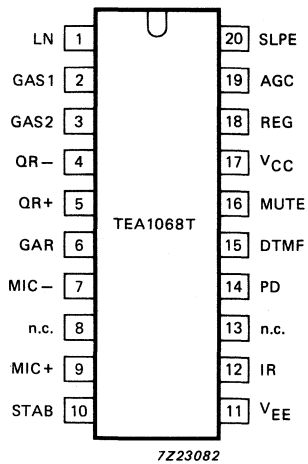


Fig. 2 (b) Pinning diagram for TEA1068T 20-lead mini-pack version.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	n.c.	not connected
9	MIC+	non-inverting microphone input
10	STAB	current stabilizer
11	V_{EE}	negative line terminal
12	IR	receiving amplifier input
13	n.c.	not connected
14	PD	power-down input
15	DTMF	dual-tone multi-frequency input
16	MUTE	mute input
17	V_{CC}	positive supply decoupling
18	REG	voltage regulator decoupling
19	AGC	automatic gain control input
20	SLPE	slope (DC resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply; V_{CC}, LN, SLPE, REG and STAB

Power for the TEA1068 and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external circuits e.g. dialling and control circuits.

Decoupling of the supply voltage is performed by a capacitor between V_{CC} and V_{EE} while the internal voltage regulator is decoupled by a capacitor between REG and V_{EE}.

The DC current drawn by the device will vary in accordance with varying values of the exchange voltage (V_{exch}), the feeding bridge resistance, (R_{exch}) and the DC resistance of the telephone line (R_{line}).

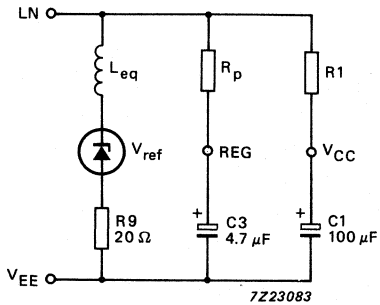
The TEA 1068 has an internal current stabilizer operating at a level determined by a 3.6 kΩ resistor connected between STAB and V_{EE} (see Fig. 8). When the line current (I_{line}) is more than 0.5 mA greater than the sum of the IC supply current (I_{CC}) and the current drawn by the peripheral circuitry connected to V_{CC} (I_p) the excess current is shunted to V_{EE} via LN.
The regulated voltage on the line terminal (V_{LN}) can be calculated as:

$$V_{LN} = V_{ref} + I_{SLPE} \times R9; \text{ or } V_{LN} = V_{ref} + [(I_{line} - I_{CC} - 0.5 \times 10^{-3}) - I_p] \times R9$$

Where V_{ref} is an internally generated temperature compensated reference voltage of 4.2 V and R9 is an external resistor connected between SLPE and V_{EE}. In normal use the value of R9 would be 20 Ω. Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics side-tone level and maximum output swing on LN, and the DC characteristics (especially at the lower voltages).

Under normal conditions, when $I_{SLPE} \geqslant I_{CC} + 0.5\ mA + I_p$, the static behaviour of the circuit is that of a 4.2 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1. Fig. 3 shows the equivalent impedance of the circuit.

The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor connected between LN and REG will decrease the internal reference voltage, connected between REG and SLPE it will increase the internal reference voltage.
Current (I_p) available from V_{CC} for supplying peripheral circuits depends on external components and on the line current. Figure 9 shows this current for $V_{CC} > 2.2$ V and for $V_{CC} > 3$ V (being the minimum supply voltage for most CMOS circuits including voltage drop for an enable diode).
If MUTE is LOW when the receiving amplifier is driven available current is further reduced.



$R_p = 17.5\ k\Omega$
$L_{eq} = C3 \times R9 \times R_p$

Fig. 3 Equivalent impedance circuit.

Microphone inputs (MIC+ and MIC−) and gain adjustment pins (GAS1 and GAS2)

The TEA1068 has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage gain is typically 52 dB (when R7 = 68 kΩ, see Fig. 13). Dynamic, magnetic, piezoelectric or electret (with built-in FET source followers) microphones can be used. Microphone arrangements are shown in Fig. 10.

The gain of the microphone amplifier can be adjusted between 44 dB and 60 dB. The gain is proportional to the value of R7 which is connected between GAS1 and GAS2. Stability is ensured by the external capacitor C6 which is connected between GAS1 and SLPE. The value of C6 is 100 pF but this may be increased to obtain a first-order low-pass filter. The cut-off frequency corresponds to the time constant R7 x C6.

Mute input (MUTE)

When MUTE is HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when MUTE is LOW or open-circuit. MUTE switching causes only negligable clicking on the earpiece outputs and the line.

Dual-tone multi-frequency input (DTMF)

When the DTMF input is enabled dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the microphone gain. The signalling tones can be heard in the telephone earpiece at a low level (confidence tone).

Receiving amplifier (IR, QR+, QR− and GAR)

The receiving amplifier has one input (IR), one non-inverting complementary output (QR+) and an inverting complementary output (QR−). These outputs may be used for single-ended or differential drive depending on the sensitivity and type of earpiece used (see Fig. 11). IR to QR + gain is typically 25 dB (when R4 = 100 kΩ), this is sufficient for low-impedance magnetic or dynamic microphones which are suited for single end drive. Using both outputs for differential drive gives an additional gain of 6 dB. This feature can be used when the earpiece impedance exceeds 450 Ω, (high-impedance dynamic or piezoelectric types).

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.

FUNCTIONAL DESCRIPTION (continued)

Receiving amplifier (IR, QR+, QR– and GAR) (continued)

The receiving amplifier gain can be adjusted between 17 and 33 dB with single-ended drive and between 26 and 39 dB with differential drive to match the sensitivity of the transducer in use. The gain is set by the external resistor R4 connected between GAR and QR+. Overall receive gain between LN and QR+ is calculated by subracting the anti-sidetone network attenuation, (32 dB), from the amplifier gain. Two external capacitors, C4 and C7, ensure stability. C4 is normally 100 pF and C7 is 10 x the value of C4. The value of C4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant R4 x C4.

Automatic gain control input (AGC)

Automatic line loss compensation is acieved by connecting a resistor (R6) between AGC and V_{EE}. The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 5.9 dB. This corresponds to a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation 1.2 dB/km. Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 12 and Table 1). The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line loss compensation is required the AGC may be left open-circuit. The amplifiers, in this condition, will give their maximum specified gain.

Power-down input (PD)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted. During these interruptions the telephone line provides no power for the transmission circuit or circuits supplied by V_{CC}. The charge held on C1 will bridge these gaps. This bridging is made easier by a HIGH level on the PD input which reduces the typical supply current from 1 mA to 55 μA and switches off the voltage regulator preventing discharge through LN. When PD is HIGH the capacitor at REG is disconnected with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required PD may be left open-circuit.

Side-tone suppression

The anti-sidetone network, ($R1//Z_{line}$, R2, R3 and Z_{bal}), (see Fig. 4) suppresses transmitted signal in the earpiece. Compensation is maximum when the following conditions are fulfilled:

(a) $R9 \times R2 = R1 \ (R3 + [R8//Z_{bal}])$;

(b) $(Z_{bal}/[Z_{bal} + R8]) = (Z_{line}/[Z_{line} + R1])$

If fixed values are chosen for R1, R2, R3, and R9 then condition (a) will always be fulfilled when $|R8//Z_{bal}| \ll R3$. To obtain optimum side-tone suppression condition (b) has to be fulfilled resulting in;

$Z_{bal} = (R8/R1)\ Z_{line} = k.Z_{line}$ where k is a scale factor, $k = (R8/R1)$.

The scale factor (k), dependent on the value of R8, is chosen to meet the following criteria:

(a) Compatability with a standard capacitor from the E6 or E12 range for Z_{bal}

(b) $|Z_{bal}//R8| \ll R3$ to fulfill condition (a) and thus ensuring correct anti-sidetone bridge operation

(c) $|Z_{bal} + R8| \gg R9$ to avoid influencing the transmitter gain

In practice Z_{line} varies considerably with the line type and length. The value chosen for Z_{bal} should therefore be for an average line length thus giving optimum setting for short or long lines.

Example

The balanced line impedance (Z_{bal}) at which the optimum suppression is present can be calculated by: suppose Z_{line} = 210 Ω + (1265 Ω/140 nF), representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).
When k = 0.64 then R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig. 4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. Fig. 5 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances.

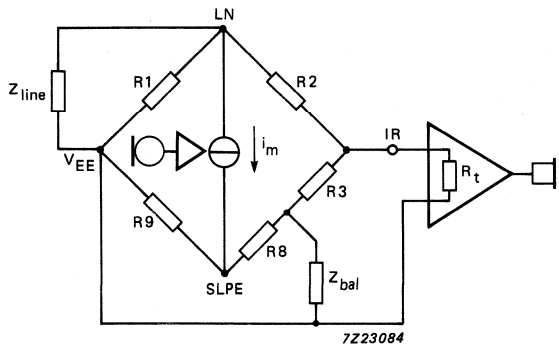


Fig. 4 Equivalent circuit of TEA1060 family anti-sidetone bridge.

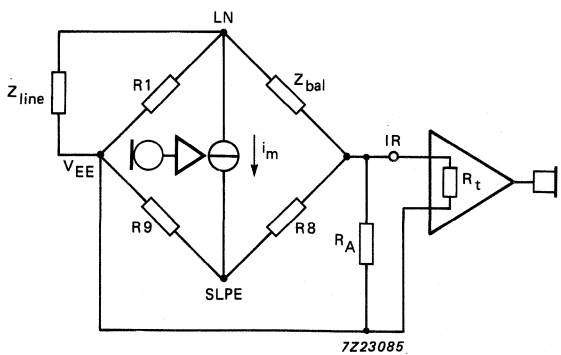


Fig. 5 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

More information can be found in the designer guide; 9398 341 10011

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive continuous line voltage		V_{LN}	–	12	V
Repetitive line voltage during switch-on line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω (Fig. 15)	V_{LN}	–	28	V
Line current TEA1068 (1)	R9 = 20 Ω	I_{line}	–	140	mA
Line current TEA1068T (1)	R9 = 20 Ω	I_{line}	–	140	mA
Voltage on all other pins		V_i	–	V_{CC} + 0.7	V
		V_i	–	−0.7	V
Total power dissipation (2)	R9 = 20 Ω				
TEA1068		P_{tot}	–	769	mW
TEA1068T		P_{tot}	–	555	mW
Storage temperature range		T_{stg}	−40	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

(1) Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE. See Figs 6 and 7 to determine the current as a function of the required voltage and the temperature.

(2) Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

From junction to ambient in free air

TEA1068	$R_{th\ j\text{-}a}$	typ.	65	K/W
TEA1068T mounted on glass epoxy board 41 x 19 x 1.5 mm	$R_{th\ j\text{-}a}$	typ.	90	K/W

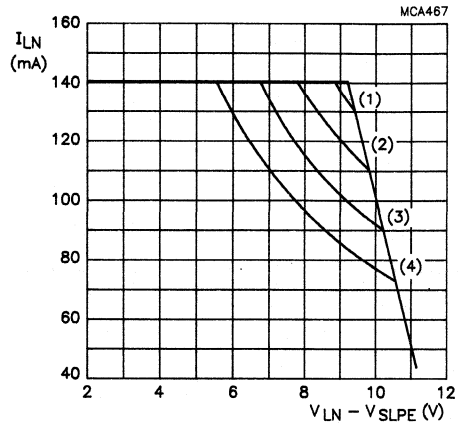


Fig. 6 TEA1068 safe operating area.

	T_{amb}	P_{tot}
(1)	45 °C	1231 mW
(2)	55 °C	1077 mW
(3)	65 °C	923 mW
(4)	75 °C	769 mW

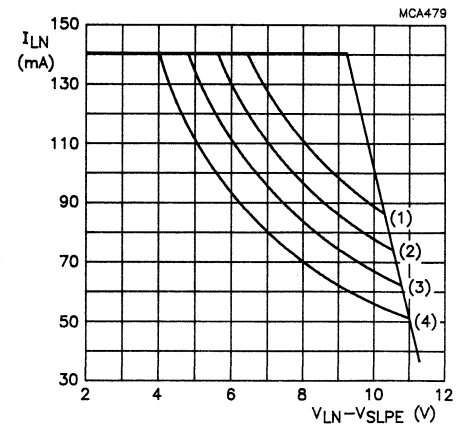


Fig. 7 TEA1068T safe operating area.

	T_{amb}	P_{tot}
(1)	45 °C	888 mW
(2)	55 °C	777 mW
(3)	65 °C	666 mW
(4)	75 °C	555 mW

CHARACTERISTICS

I_{line} = 10 to 140 mA; V_{EE} = 0 V; f = 800 Hz, T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply, LN and V_{CC}						
Voltage drop over circuit, between LN and V_{EE}	microphone inputs open					
	I_{line} = 5 mA	V_{LN}	3.95	4.25	4.55	V
	I_{line} = 15 mA	V_{LN}	4.2	4.45	4.7	V
	I_{line} = 100 mA	V_{LN}	5.4	6.1	6.7	V
	I_{line} = 140 mA	V_{LN}	–	–	7.5	V
Variation with temperature	I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	–4	–2	0	mV/K
Voltage drop over circuit, between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA; R_{VA} (LN to REG) = 68 kΩ		3.45	3.8	4.1	V
	I_{line} = 15 mA; R_{VA} (REG to SLPE) = 39 kΩ		4.65	5.0	5.35	V
Supply current	PD = LOW; V_{CC} = 2.8 V	I_{CC}	–	0.96	1.3	mA
Supply current	PD = HIGH; V_{CC} = 2.8 V	I_{CC}	–	55	82	μA
Supply voltage available for peripheral circuitry	I_{line} = 15 mA; MUTE = HIGH					
	I_p = 1.2 mA	V_{CC}	2.8	3.05	–	V
	I_p = 0 mA	V_{CC}	3.5	3.75	–	V
Microphone inputs MIC+ and MIC–						
Input impedance (differential) between MIC– and MIC+		$\|Z_i\|$	51	64	77	kΩ
Input impedance (single-ended) MIC– or MIC+ to V_{EE}		$\|Z_i\|$	25.5	32	38.5	kΩ
Common mode rejection ratio		k_{CMR}	–	82	–	dB
Voltage gain MIC+/MIC– to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	51	52	53	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	–0.5	± 0.2	+0.5	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Microphone inputs MIC+ and MIC– (continued)						
Gain variation with temperature at –25 °C and +75 °C	w.r.t. 25 °C; without R6; I_{line} = 50 mA	ΔG_{vT}	–	± 0.2	–	dB
Dual-tone multi-frequency input DTMF						
Input impedance		$\|Z_i\|$	16.8	20.7	24.6	kΩ
Voltage gain from DTMF ro LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	24.5	25.5	26.5	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t 800 Hz	ΔG_{vf}	–0.5	± 0.2	+ 0.5	dB
Gain variation with temperature at – 25 °C and + 75 °C	w.r.t 25 °C; I_{line} = 50 mA	ΔG_{vT}	–	± 0.5	–	dB
Gain adjustement GAS1 and GAS2						
Gain variation of the transmitting amplifier by varying R7 between GAS1 and GAS2		ΔG_v	–8	–	+8	dB
Sending amplifier output LN						
Output voltage	I_{line} = 15 mA; THD = 2%	$V_{LN(rms)}$	1.9	2.3	–	V
	THD = 10%	$V_{LN(rms)}$	–	2.6	–	V
Noise output voltage	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	–72	–	dBmp
Receiving amplifier input IR						
Input impedance		$\|Z_i\|$	17	21	25	kΩ

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Receiving amplifier outputs QR+ and QR−						
Output impedance (single-ended)		$\|Z_o\|$	–	4	–	Ω
Voltage gain from IR to QR+ or QR−	I_{line} = 15 mA					
single-ended	R_L (from QR+ or QR−) = 300 Ω	G_v	24	25	26	dB
differential	R_L (from QR+ or QR−) = 600 Ω	G_v	30	31	32	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	−0.5	−0.2	0	dB
Gain variation with temperature at −25 °C and +75 °C	w.r.t. 25 °C; I_{line} = 50 mA; without R6	ΔG_{vT}	–	± 0.2	–	dB
Output voltage	sinewave drive; I_{line} = 15 mA; I_p = 0 mA; THD = 2%; R4 = 100 kΩ					
single-ended	RL = 150 Ω	$V_{o(rms)}$	0.3	0.38	–	V
	RL = 450 Ω	$V_{o(rms)}$	0.4	0.52	–	V
differential	f = 3400 Hz; series R = 100 Ω; C_L = 47 nF	$V_{o(rms)}$	0.8	1.0	–	V
Noise output voltage	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted; (P53 curve)					
single-ended	RL = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential	RL = 600 Ω	$V_{no(rms)}$	–	100	–	μV
Gain adjustment GAR						
Gain variation of receiving amplifier achievable by varying R4 between GAR and QR		ΔG_v	−8	–	+8	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Mute input						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{MUTE}	–	8	15	μA
Gain reduction MIC+ or MIC– to LN	MUTE = HIGH	G_v	–	70	–	dB
Voltage gain from DTMF to QR+ or QR–	MUTE = HIGH; R4 = 100 kΩ; single-ended; R_L = 300 Ω	G_v	–21	–19	–17	dB
Power-down input PD						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{PD}	–	5	10	μA
Automatic gain control input AGC						
Controlling the gain from IR to QR+/QR– and the gain from MIC+/MIC– to LN; R6 between AGC and V_{EE}	R6 = 110 kΩ					
Gain control range	I_{line} = 70 mA	ΔG_v	–5.5	–5.9	–6.3	dB
Highest line current for maximum gain		I_{line}	–	23	–	mA
Minimum line current for minimum gain		I_{line}	–	61	–	mA
Reduction of gain between I_{line} = 15 mA and I_{line} = 35 mA		ΔG_v	–1.0	–1.5	–2.0	dB

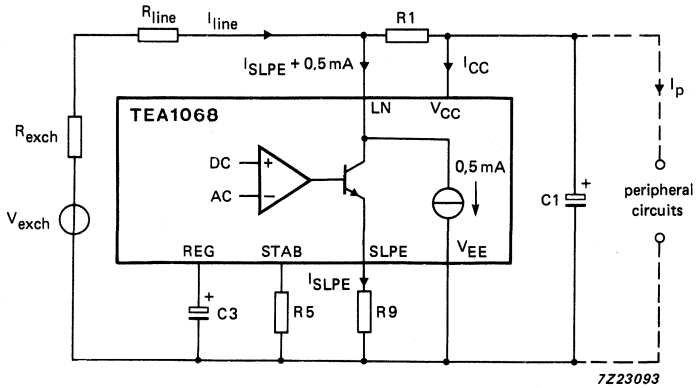


Fig. 8 Supply arrangement.

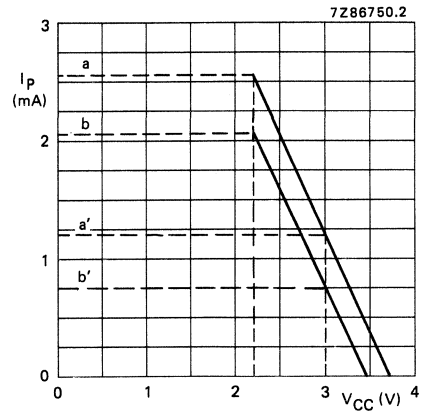


Fig. 9 Typical current I_p available from V_{CC} for peripheral circuitry with $V_{CC} >= 2.2$ V. Curve (a) is valid when the receiving amplifier is not driven or when MUTE = HIGH, curve (b) is valid when MUTE = LOW and the receiving amplifier is driven; $V_{o(rms)} = 150$ mV, $R_L = 150\ \Omega$ asymmetrical. The supply possibilities can be increased simply by setting the voltage drop over the circuit V_{LN} to a higher value by means of resistor R_{VA} connected between REG and SLPE.

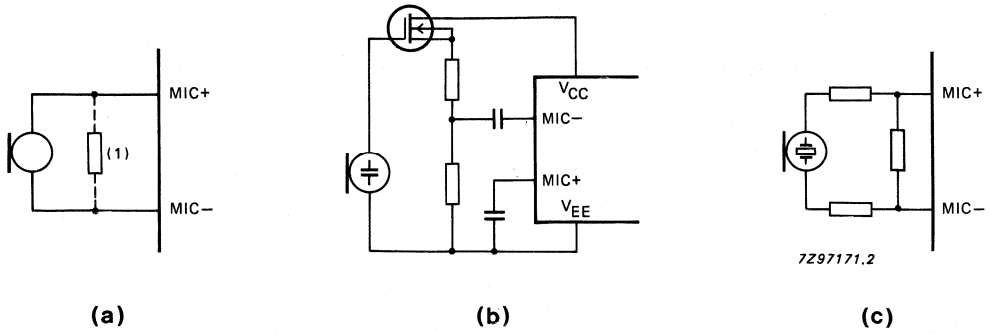


Fig. 10 Alternative microphone arrangements.

(a) Magnetic or dynamic microphone. The resistor marked (1) may be connected to decrease the terminating impedance.
(b) Electret microphone.
(c) Piezoelectric microphone.

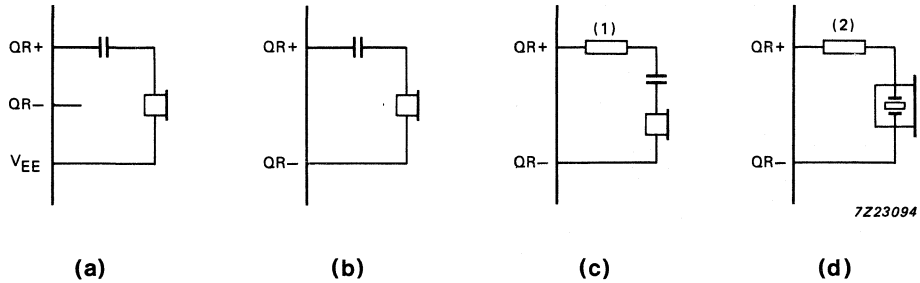


Fig. 11 Alternative receiver arrangements.

(a) Dynamic earpiece with less than 450 Ω impedance.
(b) Dynamic earpiece with more than 450 Ω impedance.
(c) Magnetic earpiece with more than 450 Ω impedance. The resistor marked (1) may be connected to prevent distortion (inductive load).
(d) Piezoelectric telephone. The resistor marked (2) is required to increase the phase margin (capacitive load).

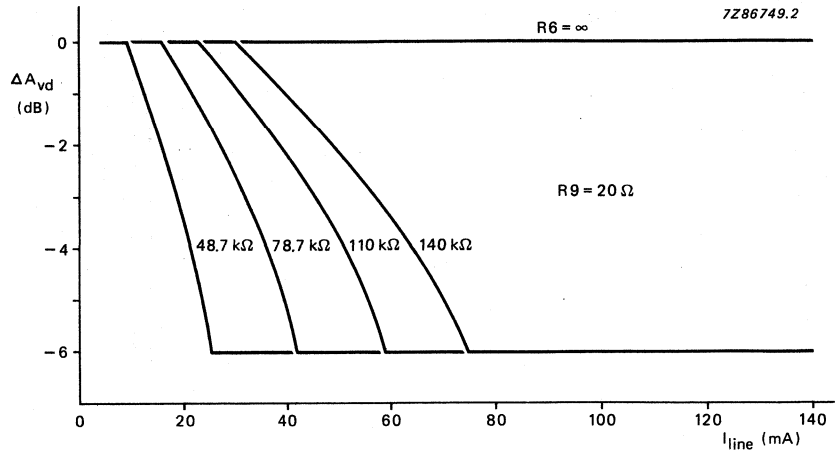


Fig. 12 Variation of gain with line current, with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (KΩ)			
V_{exch} (V)	24	61.9	48.7	X	X
	36	100	78.7	68	60.4
	48	140	110	93.1	82
	60	X	X	120	102

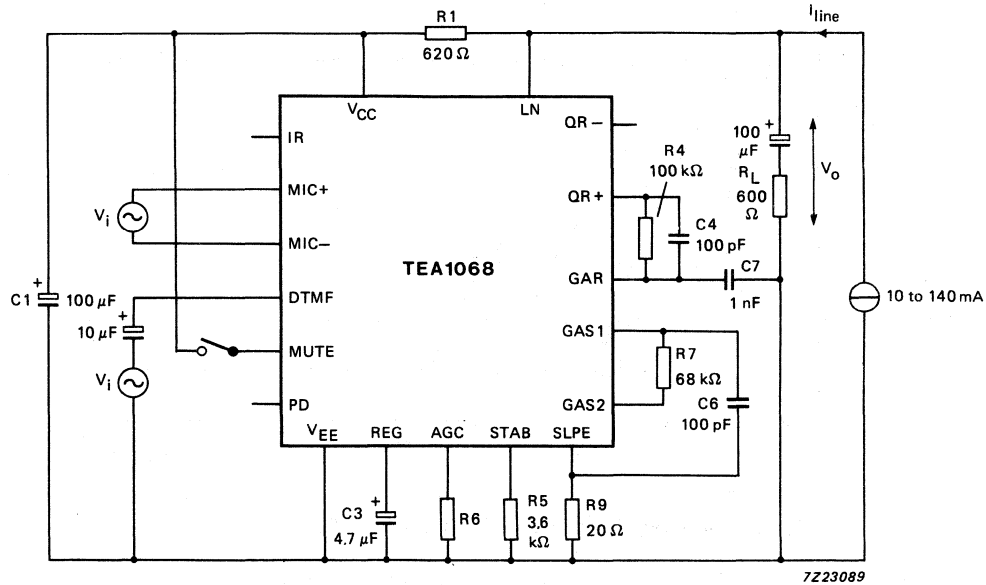


Fig. 13 Test circuit for defining voltage gain of MIC+, MIC– and DTMF inputs. Voltage gain is defined as; $G_V = 20 \log |V_O/V_i|$. For measuring the gain from MIC+ and MIC– the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

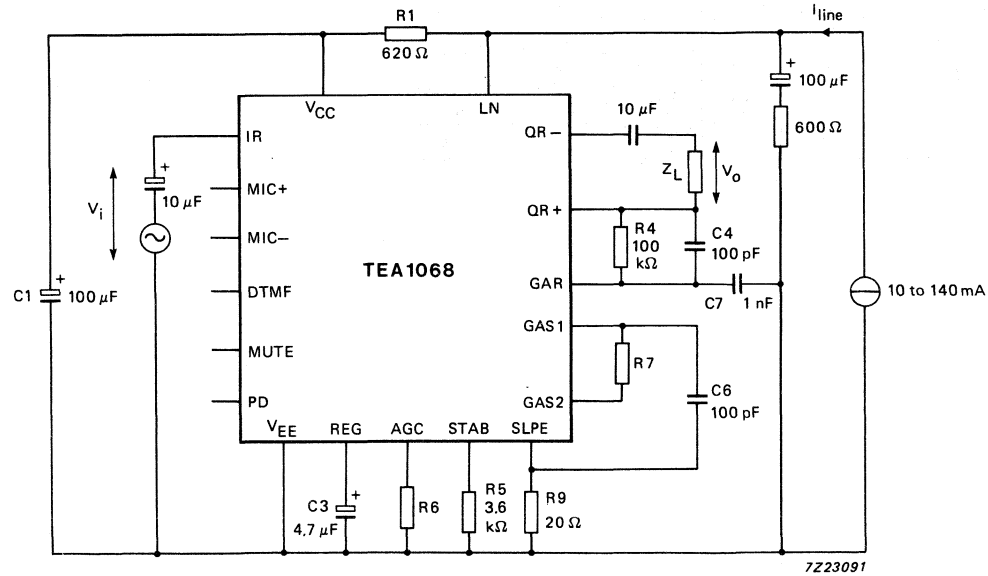


Fig. 14 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as; $G_V = 20 \log |V_O/V_i|$.

APPLICATION INFORMATION

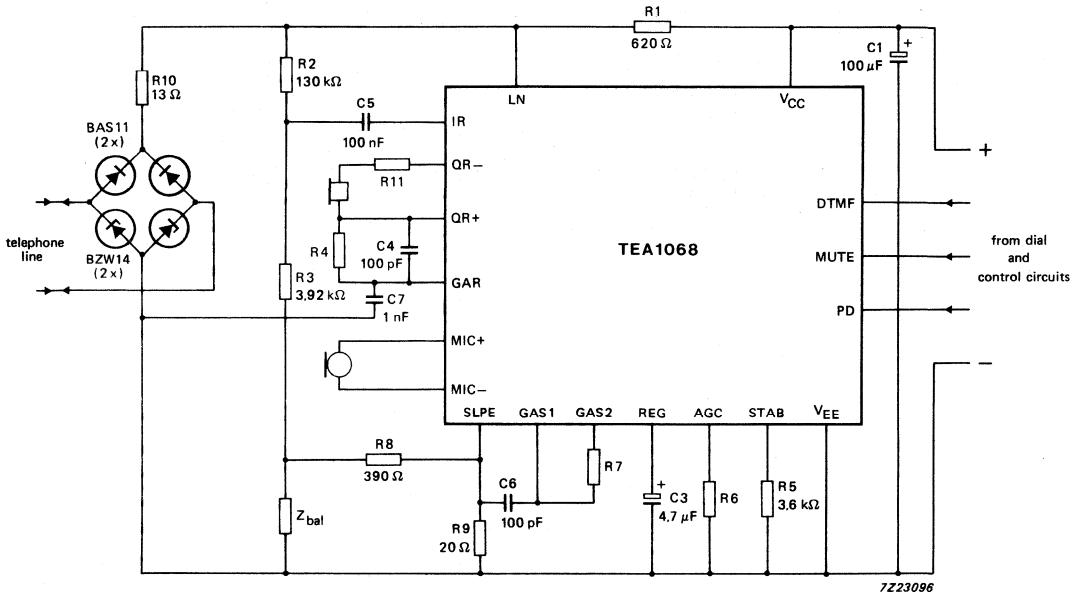


Fig. 15 Typical application of the TEA1068, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

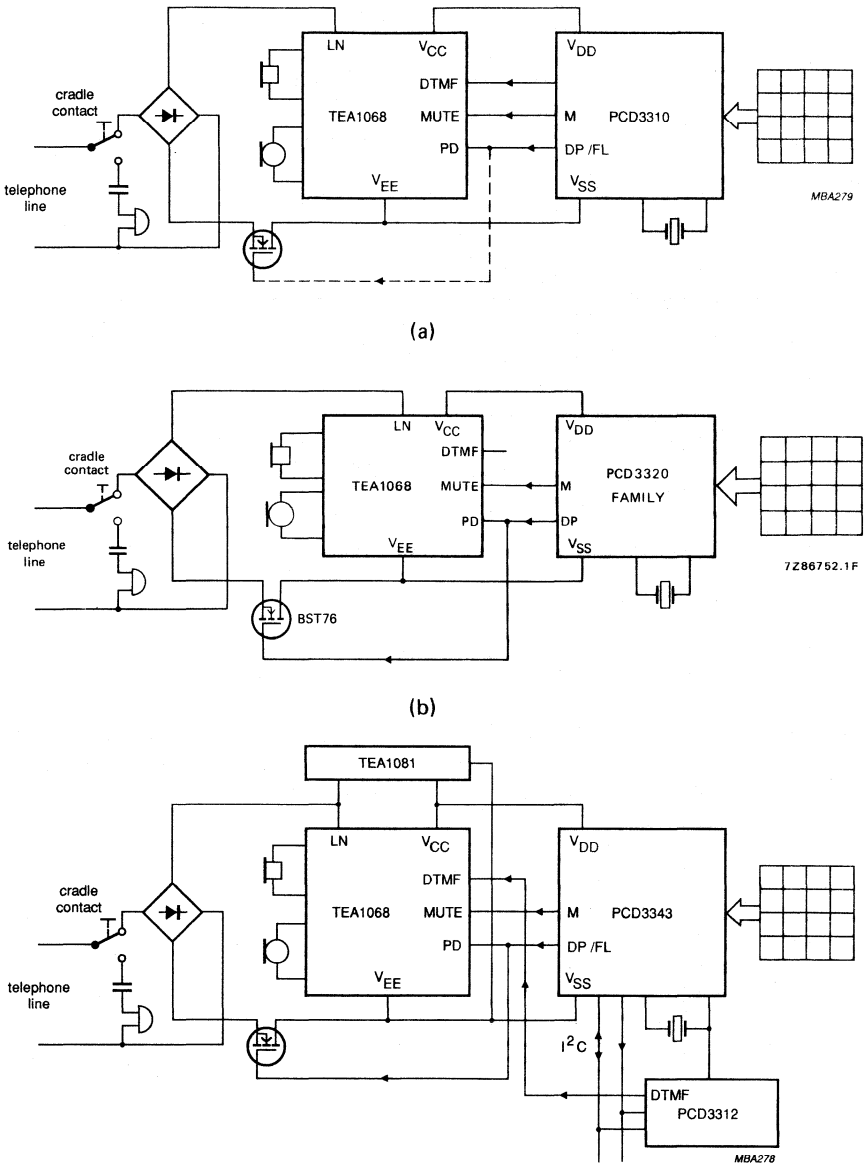


Fig. 16 Typical applications of the TEA1068 (simplified).

(a) DTMF set with a CMOS DTMF dialling circuit. The dashed lines show an optional flash (register recall by times loop break).

(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.

(c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C-bus. The supply is provided by TEA1081 supply circuit.

SUPPLY CIRCUIT WITH POWER-DOWN FOR TELEPHONE SET PERIPHERALS

GENERAL DESCRIPTION

The TEA1081 is a bipolar integrated circuit for use in line-powered telephone sets to supply peripheral circuits for extended dialling and/or loudspeaking facilities.

The IC uses a part of the surplus line current normally drawn by the voltage regulator of the speech/transmission circuit. A power-down function isolates the IC from its load and reduces the input current.

Features

- High input impedance for audio signals
- Low DC series resistance
- High output current
- Large audio signal handling capability
- Low distortion
- Two modes of operation:
  - output voltage that follows the DC line voltage
  - regulated output voltage
- Power-down input
- Low number of external components

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Operating DC line voltage		V_{LN}	2,5	–	12	V
DC output voltage		V_O	2,0	–	10	V
Voltage drop from line to output		V_{LN}-V_O	–	0,5	–	V
Series resistance		R_S	–	20	–	Ω
Output current	V_{LN} = 4 V					
TEA1081		I_O	–	–	30	mA
TEA1081T		I_O	–	–	20	mA
AC line voltage (RMS value)	V_{LN} = 4 V; I_O = 15 mA; d = 2%	$v_{LN(rms)}$	–	1,5	–	V
Internal supply current	V_{LN} = 4 V	I_{INT}	–	0,8	–	mA
Operating ambient temperature range		T_{amb}	–25	–	+ 70	°C

PACKAGE OUTLINES

TEA1081: 8-lead dual in-line; plastic (SOT97).
TEA1081T: 8-lead mini-pack; plastic (SO8; SOT96A).

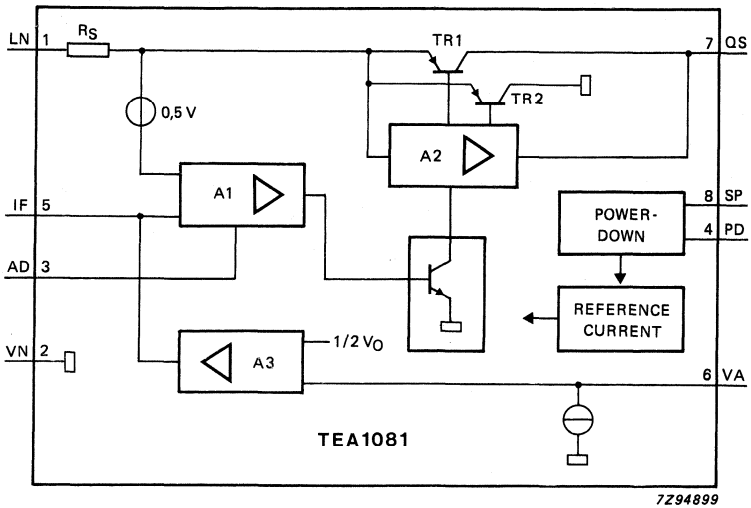


Fig. 1 Block diagram.

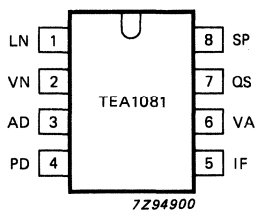


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	VN	negative line terminal
3	AD	amplifier decoupling
4	PD	power-down input
5	IF	low pass filter input
6	VA	output voltage adjustment
7	QS	power supply output
8	SP	supply input: power-down circuit

FUNCTIONAL DESCRIPTION

The TEA1081 is a supply interface between telephone line and peripheral devices in the telephone set. The high input impedance of the circuit allows direct connection to the telephone line (via a diode bridge). An inductor function is obtained by amplifier A1, resistor R_S (Fig. 1) and an external low-pass RC filter.

Under the control of amplifier A2, transistor TR1 supplies peripheral devices and transistor TR2 minimizes line signal distortion by momentarily diverting input current to ground whenever the instantaneous value of the line voltage drops below the output voltage.

Internal circuits are biased by a temperature and line voltage compensated reference current source.

The power-down circuit isolates the supply circuit from external circuitry.

Line terminals: LN, VN (pins 1, 2)

The input terminals LN and VN can be connected directly to the line. The minimum DC line voltage required at the input is given by

$$V_{LN} = I_1 \times R_S + V_{LN\,min} + v_{LN(P)} \quad (V)$$

in which

I_1 = input current
R_S = internal series resistance
$v_{LN\,min}$ = minimum instantaneous line voltage (1,4 V at I_O = 5 mA)
$v_{LN(P)}$ = required peak level of AC line voltage

The internal current (I_{INT}) at I_O = 0 mA is typically 0,8 mA at V_{LN} = 4 V and reaches a maximum of 1,4 mA at V_{LN} = 12 V.

Supply terminals: QS, VA (pins 7, 6)

Peripheral devices are supplied from QS (pin 7). Two modes of output voltage regulation are available:

Output voltage follows line voltage (Fig. 3)

The TEA1081 operates in this mode when there is no external resistor (R_V) between QS and VA (pins 6 and 7).

The output voltage follows the line voltage and is expressed by

$$V_O = V_{LN} - (I_1 \times R_S + 0{,}5) \quad (V)$$

in which

V_{LN} = line voltage
I_1 = input current
R_S = internal series resistance

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

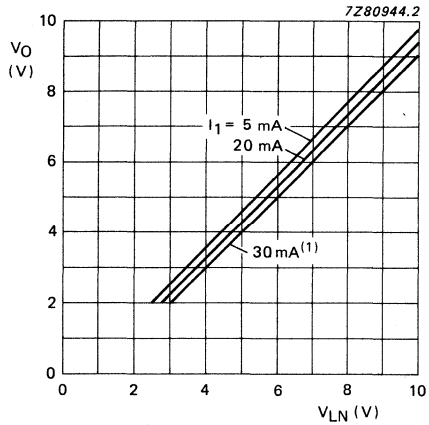
Regulated output voltage (Fig. 4)

The circuit operates in this mode when an external resistor (R_V) is connected between QS and VA (pins 6 and 7, see Fig. 6).

The output voltage is held constant at $V_O = 2 \times I_6 \times R_V$ (V)

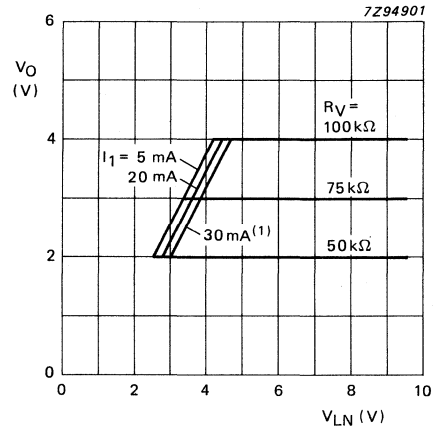
as soon as the line voltage $V_{LN} > (2 \cdot I_6 \cdot R_v + I_1 \cdot R_S + 0{,}5)$ (V)

The control current I_6 is typically 20 μA.



(1) I_1 = 30 mA; not valid for TEA1081T

Fig. 3 Output voltage as a function of line voltage (application without R_V).



(1) I_1 = 30 mA; not valid for TEA1081T

Fig. 4 Output voltage as a function of line voltage (R_V connected between QS and VA).

Input and output currents I_1, I_O (pins 1 and 7)

The maximum available current into pin 1 (I_1) is determined by:

- the minimum line current ($I_{LINE\ min}$) that is available for the telephone set;
- the specified minimum input current ($I_{LN\ min}$) for the speech/transmission circuit.

That is $I_{1\ max} = I_{LINE\ min} - I_{LN\ min}$.

At $v_{LN(rms)} < 150$ mV, the input current I_1 is approximately:

$$I_1 = I_{INT} + k \cdot I_O \quad \text{(mA)}$$

in which

I_{INT} = internal supply current (0,8 mA at V_{LN} = 4 V);
k = correction factor (k < 1,1 for the specified output current range).

With large line signals the instantaneous line voltage may drop below V_O + 0,4 V. Normally (when $v_{LN} > V_O$ + 0,4 V), instantaneous current flows from LN to QS (pin 1 to pin 7) to the output load. When $v_{LN} < V_O$ + 0,4 V, the instantaneous current is diverted to pin 2 to prevent distortion of the line signal.

Input current at $v_{LN(rms)}$ = 1 V and without R_V approximates to

$$I_I = I_{INT} + 2\,I_O \quad \text{(mA)}$$

The maximum supply current (within the specified output current limits) available for peripheral devices is shown by

$$I_{O\,max} = \frac{I_{LINE\,min} - I_{LN\,min} - I_{INT}}{2}$$

in which

$I_{LINE\,min}$ is the minimum line current of the telephone set;

$I_{LN\,min}$ is the specified minimum input current of the speech/transmission circuit.

Input low-pass filter: IF (pin 5)

The input impedance between LN and VN at audio frequencies is determined mainly by the filter elements C_L (between pins 1 and 5), R_L (between pins 5 and 7) and the internal resistor R_S (typical value 20 Ω). At audio frequencies the TEA1081 behaves as an inductor of the value $L_I = C_L \cdot R_L \cdot R_S$ (H). The typical value of L_I at C_L = 2,2 μF and R_L = 100 kΩ is 4,4 H.

Amplifier decoupling: AD (pin 3)

To ensure stability, a 68 pF decoupling capacitor is required between AD (pin 3) and LN (pin 1). If $I_{Omin} < 1{,}5$ mA, a 47 pF capacitor has to be added between AD (pin 3) and VA (pin 6).

Power-down inputs: PD, SP (pins 4 and 8)

During pulse dialling or register recall, or if the input current to pin 1 is insufficient to maintain the output current, the supply to peripheral devices can be switched off by activating the PD input at pin 4. With PD = HIGH, the input current is reduced to (typ.) 40 μA at V_{LN} = 4 V and the internal circuits are isolated from the load at QS (pin 7).

The power-down circuit is supplied via the SP input (pin 8). SP can be wired to QS in conditions where $V_O > V_{SP\,min}$ during line interruptions. When $V_O < V_{SP\,min}$, SP should be wired to an external supply point (e.g. to V_{CC} of the TEA1060 family circuit).

When power-down is not required, the PD and SP inputs can be left open-circuit.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive line voltage	continuous	V_{LN}	–	12	V
	during switch-on or line interruptions	V_{LN}	–	12,5	V
Repetitive line voltage peaks	1 ms/5 s; 12 Ω resistor in series with pin 1	V_{LN}	–	28	V
Voltage on all other terminals		V	V_{VN}–0,5	V_{LN}+0,5	V
Input current (DC)	TEA1081	I_1	–	120	mA
Input current (DC)	TEA1081T	I_1	–	80	mA
Current into all other terminals		I_I	–1	+1	mA
Total power dissipation		P_{tot}	see Fig. 5		
Storage temperature range		T_{stg}	–40	+125	°C
Operating ambient temperature range		T_{amb}	–25	+70	°C
Junction temperature		T_j	–	+125	°C

THERMAL RESISTANCE

From junction to ambient in free air

TEA1081 $R_{th\ j\text{-}a}$ = 120 K/W

TEA1081T (circuit mounted on printed circuit board of 50 x 50 x 1,5 mm) $R_{th\ j\text{-}a}$ = 260 K/W

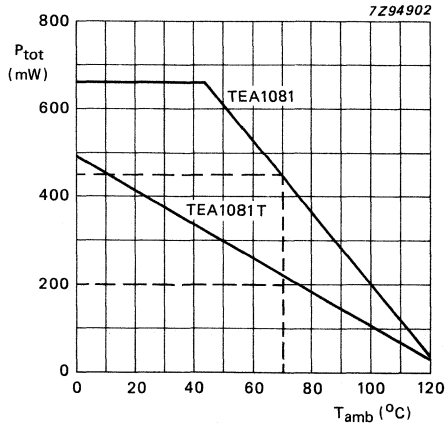


Fig. 5 Power derating curves.

DEVELOPMENT DATA

CHARACTERISTICS

V_{LN} = 4 V; $v_{LN(rms)}$ = 100 mV; I_O = 5 mA; f = 300 to 3400 Hz; R_L = 100 kΩ; C_L = 2,2 μF; R_V = 75 kΩ; T_{amb} = 25 °C; unless otherwise specified; see Fig. 6.

parameter	conditions	symbol	min.	typ.	max.	unit
Operating DC line voltage		V_{LN}	2,5	–	12	V
Min. instantaneous line voltage		V_{LN}	–	–	1,4	V
Max. instantaneous line voltage		V_{LN}	12	–	–	V
Characteristics with R_V = 75 kΩ connected between pins 6 and 7 and C_L = 10 μF						
Input current (pin 1)	v_{LN} = 0 V	I_1	–	5,8	–	mA
	$v_{LN(rms)}$ = 1,5 V; I_O = 15 mA	I_1	–	30	–	mA
Output voltage (pin 7)		V_O	–	3	–	V
Variation of output voltage over the ranges of:						
line voltage	V_{LN} = 4 to 6 V	ΔV_O	–	100	–	mV
temperature	T_{amb} = +25 to −25 °C	ΔV_O	–	−100	–	mV
	T_{amb} = +25 to +75 °C	ΔV_O	–	−100	–	mV
output current	I_O = 5 to 20 mA	ΔV_O	–	−100	–	mV
Control current (pin 6)		I_6	–	20	–	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Characteristics without R_V						
Input current (pin 1)	v_{LN} = 0 V	I_1	–	6,0	–	mA
	$v_{LN(rms)}$ = 1,5 V; I_O = 15 mA	I_1	–	31	–	mA
Voltage drop (pin 1 to pin 7)	I_O = 0 mA	V_{LN}-V_O	–	0,5	–	V
	I_O = 15 mA; $v_{LN(rms)}$ = 1,5 V	V_{LN}-V_O	–	1,1	–	V
Output current (pin 7)						
	TEA1081	I_O	–	–	30	mA
	TEA1081T	I_O	–	–	20	mA
Internal series resistance		R_S	–	20	–	Ω
Internal supply current	I_O = 0 mA; PD = LOW; V_{SP} = V_O	I_{INT}	–	0,8	1,4	mA
	PD = HIGH (note 1); V_{SP} > 2 V	I_{INT}	–	40	60	μA
Total distortion	$v_{LN(rms)}$ = 1,5 V	d_{tot}	–	–	2	%
Balance return loss	600 Ω reference	BRL	25	–	–	dB
Harmonic levels of line voltage	f = 500 Hz; v_{LN} = 0 dBm; Z_{line} = 600 Ω					
	second harmonic	v_{LN}–2H	–	–58	–	dBm
	third harmonic	v_{LN}–3H	–	–60	–	dBm
Noise voltage on input terminal	v_{LN} = 0 mV; R_L = 600 Ω; P53 curve	$v_{ni(rms)}$	–	–83	–	dBmp
Power-down input (pin 4)						
Input voltage HIGH		V_{IH}	1,5	–	V_{SP}	V
Input voltage LOW		V_{IL}	–	–	0,3	V
Input current		I_4	–	–	10	μA
Power-down input (pin 8)						
Supply voltage for power-down		V_8	2	–	V_{LN}	V
Supply current to power-down circuit	V_8 = 3 V	I_8	–	–	70	μA

Note 1. Power-down circuit supplied via external source.

APPLICATION INFORMATION

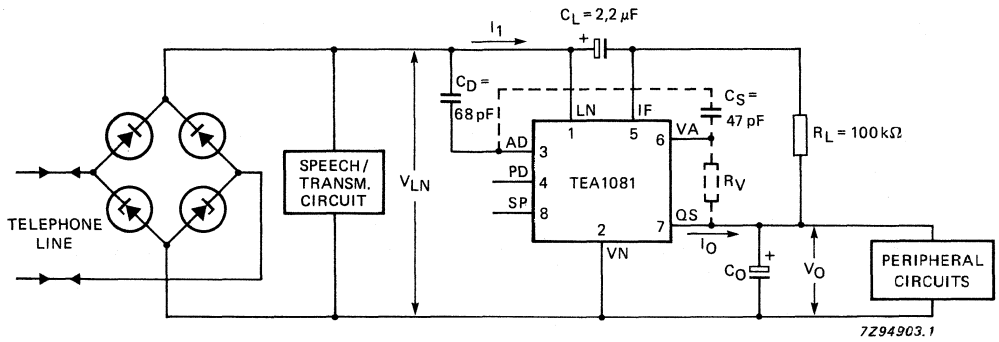


Fig. 6 Application diagram.

DEVELOPMENT DATA

LISTENING-IN CIRCUIT FOR LINE-POWERED TELEPHONE SETS

The TEA1085 is a bipolar IC which has been designed for use in line-powered telephone sets and provides a listening-in facility for the received line signal via a loudspeaker. Nearly all the line current can be used for powering the loudspeaker.
The circuit incorporates a supply circuit, loudspeaker amplifier dynamic limiter, MUTE circuit, power-down facility and logic inputs for gain setting. The device also incorporates a Larsen Level Limiter to reduce howling effects.
The IC is intended for use in conjunction with a transmission circuit of the TEA1060 family.

Features

- Internal supply
  - optimum current split-up
  - — low constant current (adjustable) in transmission IC
  - — nearly all line current available for listening-in
  - adjustable supply voltage
- Loudspeaker amplifier
  - dynamic limiter providing low distortion and the highest possible output power
  - SE or BTL drive for loudspeaker
  - volume control by potentiometer and/or logic inputs (e.g. microcontroller drive)
  - fixed gain of 35 dB
- Larsen level limiter
  - low sensitivity for own speech due to 3rd-order filter and attack delay
  - adjustable voltage thresholds
- Power down input
- MUTE input
  - clickfree switching between listening-in mode and standby mode
  - toggle function
  - start-up in standby condition

PACKAGE OUTLINES

TEA1085: 24-lead dual in-line; plastic (SOT101B).
TEA1085T: 24-lead mini-pack; plastic (SO24; SOT137A).

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Input current range		I_{SUP}	4	–	120	mA
Stabilized supply voltage		V_{BB}	–	3.6	–	V
Current consumption	PD = HIGH	I_{SUP}	–	55	–	μA
Voltage gain loudspeaker amplifier	SE	G_v	–	35	–	dB
	BTL	G_v	–	41	–	dB
Maximum gain reduction with logic inputs (3 steps)		ΔG_v	–	18	–	dB
Minimum input current	P_{OUT} = 20 mW typ. into 50 Ω SE	I_{SUP}	–	15	17	mA
	P_{OUT} = 40 mW typ. into 50 Ω BTL	I_{SUP}	–	–	32	mA
Larsen limiter attack delay time V_{DTI} jumps from 0 to ⩾ 100 mV (RMS value)		$t_{ad(rms)}$	100	–	200	ms
Larsen limiter threshold level	Larsen mode	$V_{DTI(rms)}$	–	7	–	mV
Larsen limiter preamplifier gain setting range		G_v	30	–	52	dB
Operating ambient temperature range		T_{amb}	–25	–	+ 75	°C

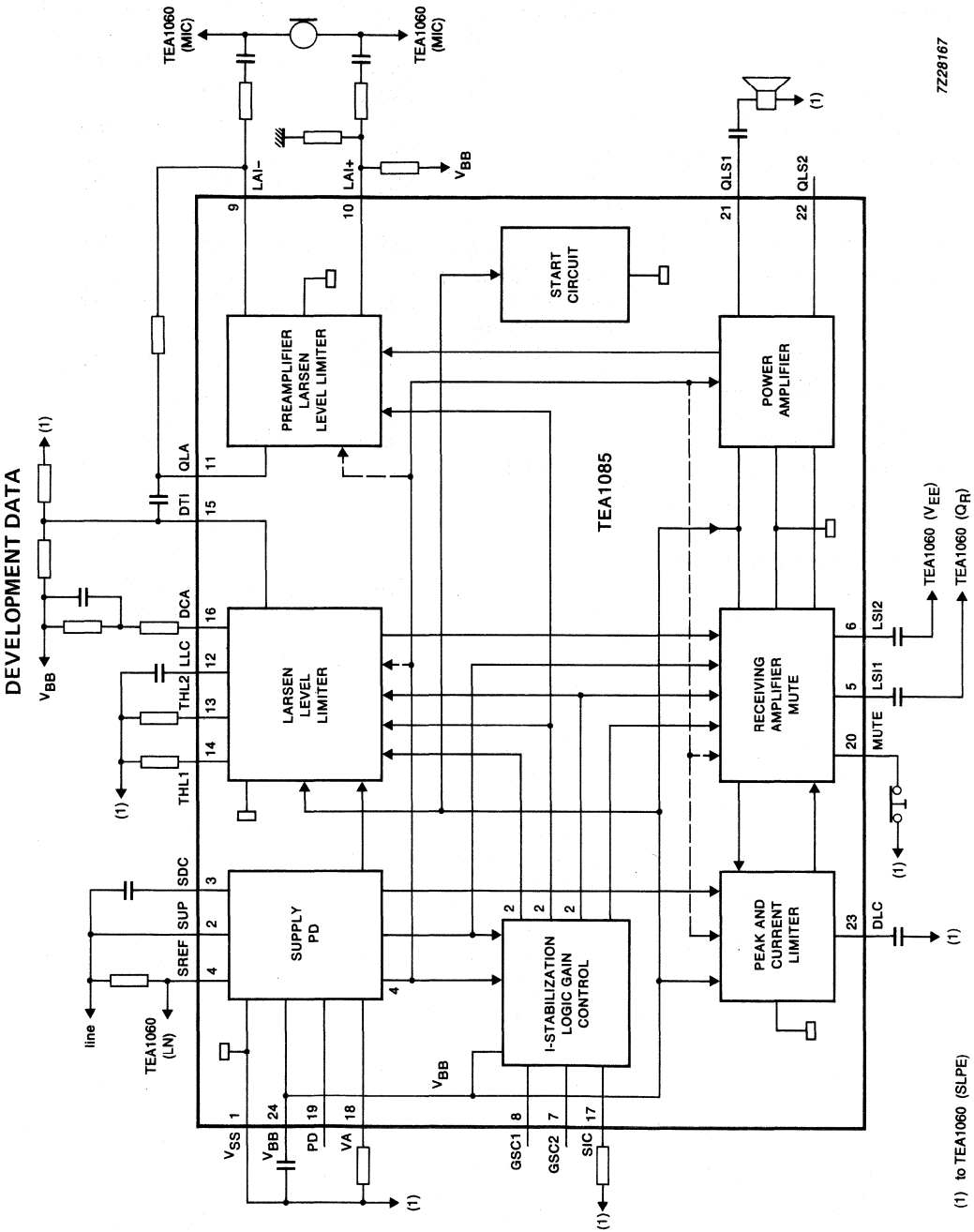


Fig.1 Block diagram.

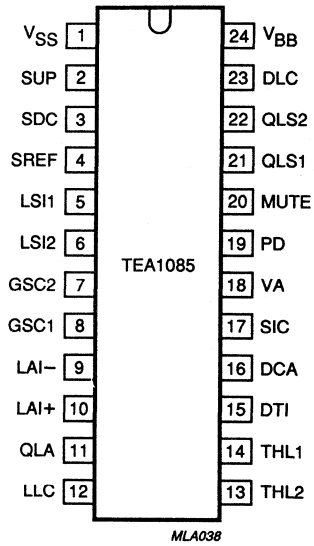


Fig.2 Pinning diagram.

PINNING CONNECTIONS

pin no.	symbol	description
1	V_{SS}	negative supply
2	SUP	positive supply
3	SDC	supply amplifier decoupling
4	SREF	supply reference input
5	LSI1	loudspeaker amplifier input 1
6	LSI2	loudspeaker amplifier input 2
7	GSC2	logic input 2 for gain select
8	GSC1	logic input 1 for gain select
9	LAI−	Larsen limiter preamplifier inverting input
10	LAI+	Larsen limiter preamplifier non-inverting input
11	QLA	Larsen limiter preamplifier output
12	LLC	Larsen limiter capacitor
13	THL2	Larsen limiter residual threshold level
14	THL1	Larsen limiter attack delay threshold level
15	DTI	Larsen limiter detector input
16	DCA	Larsen limiter detector current adjustment
17	SIC	Larsen limiter current stabilizer
18	VA	V_{BB} voltage adjustment
19	PD	Power-down input
20	MUTE	MUTE toggle input
21	QLS1	loudspeaker amplifier output 1
22	QLS2	loudspeaker amplifier output 2
23	DLC	dynamic limiter capacitor
24	V_{BB}	stabilized supply decoupling

FUNCTIONAL DESCRIPTION

Figure 1 illustrates a block diagram of the TEA1085 with external components and connections to the transmission IC.

The TEA1085 is a bipolar IC which has been designed for use in line-powered telephone sets and provides a listening-in facility for the received line signal via a loudspeaker. Nearly all the line current can be used for powering the loudspeaker.

The loudspeaker amplifier consists of a preamplifier, to amplify the earpiece signal from the transmission circuit and, a double push-pull output stage to drive the loudspeaker in the BTL (bridge tied load) or SE (single ended) configuration. The gain of the preamplifier is controlled by a dynamic limiter which prevents high distortion of the loudspeaker signal. This is achieved by preventing clipping of the loudspeaker signal, with respect to the supply voltage, and at too low supply current. Two logic inputs can be used to reduce the gain in 3 steps.

Because of acoustic feedback from the loudspeaker to the microphone, howling signals (Larsen effect) can occur on the telephone line and in the loudspeaker. When the Larsen signal exceeds a voltage and time duration threshold the Larsen level limiter (LLL) will reduce the Larsen signal to a low level within a short period of time by reducing the gain of the receiving preamplifier. This is achieved by using the microphone signal as an input signal which is processed in the LLL via a preamplifier and 3rd-order filter.

The MUTE input can be used to enable or disable the loudspeaker amplifier and is provided with a toggle function to permit the use of a simple push-button switch.

By activating the power-down input the current consumption of the circuit will be reduced, this enables pulse dialling or flash (register recall).

An internal start circuit ensures normal start-up of the transmission IC and start-up of the listening-in IC in the standby mode.

The TEA1085 is intended for use in conjunction with a member of the TEA1060 family and should be connected between LINE and SLPE of the transmission IC. The transmission characteristics (impedance, gain settings etc.) are not affected. The interconnection between the two ICs is illustrated in Fig.3.

DEVELOPMENT DATA

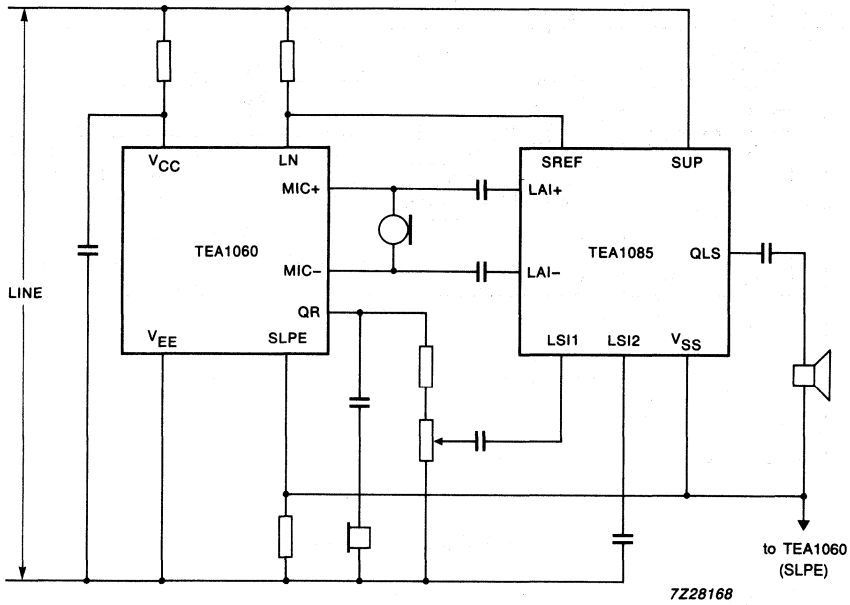


Fig.3 TEA1085/TEA1060 interconnection.

Supply; SUP, SREF, V_{BB}, V_{SS} and VA

The line current is divided into I_{TR} for the TEA1060 and I_{SUP} for the TEA1085. The supply arrangement is illustrated in Fig.4.

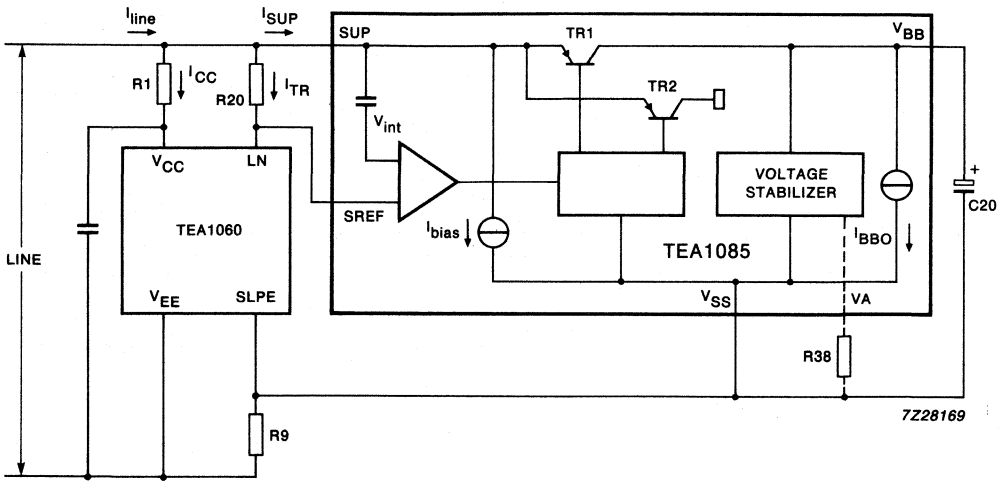


Fig.4 Supply arrangement.

I_{TR} is constant: $I_{TR} = V_{int}/R20$

$I_{SUP} = I_{line} - I_{CC} - I_{TR}$

Where:

V_{int} is an internal temperature compensated reference voltage with a typical value of 315 mV between SUP and SREF

R20 is a resistor between SUP and SREF

I_{CC} is the internal current consumption of the TEA106X ($\approx$ 1 mA)

A practical value for R20 is 150 Ω. This value of resistance produces a value for I_{TR} = 2 mA and $I_{SUP} = I_{LINE} - 3$ mA.

The TEA1085 stabilizes its own supply voltage at V_{BB}. Transistor TR1 provides the supplies for the internal circuits. TR2 is used to minimize the signal distortion on the line by momentarily diverting the input current to V_{SS} whenever the instantaneous value of the voltage V_{SUP} drops below the supply voltage V_{BB}. V_{BB} is fixed to a typical value of 3.6 V but can be increased by means of an external resistor (R38) connected between VA and V_{SS}. The supply at V_{BB} is decoupled by a 470 μF capacitor.

DEVELOPMENT DATA

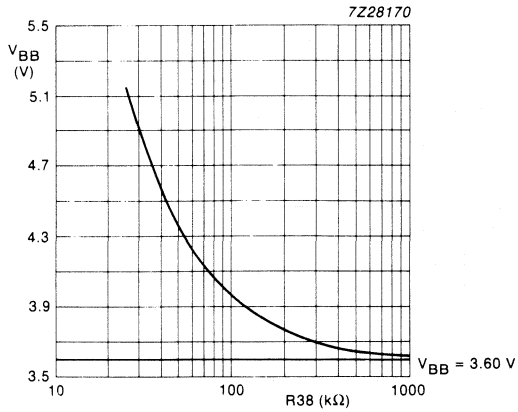


Fig.5 Stabilized supply voltage as a function of R38.

The DC voltage ($V_{SUP} - V_{SS}$) is determined by the transmission IC ($V_{LN-SLPE}$); thus $V_{SUP} - V_{SS} = V_{LN-SLPE} + V_{int}$. The minimum DC voltage that can be applied to the input is $V_{BB(max)} + 0.4$ V: where: $V_{BB(max)}$ is the worst case supply voltage (this depends on the setting of R38, which is connected between VA and V_{SS}).

The internal current consumption of the TEA1085 (I_{SUP0}) is typically 4.2 mA (where $V_{SUP} - V_{SS}$ = 4.5 V, MUTE off). Thus the current available for powering the loudspeaker is $I_{SUP} - I_{SUP0}$.
The current I_{SUP0} consists of a bias current of ≈ 0.4 mA for the circuit connected to SUP and current I_{BBO} of ≈ 3.8 mA which is used for the circuit connected to V_{BB} (see Fig.4).

Supply amplifier stability (SDC) pin 3

To ensure stability of the TEA1085, in combination with a transmission IC of the TEA1060 family, a 47 pF capacitor connected between SDC and SUP and a 150 μH coil connected between SUP and the positive terminal (Fig.16) is required.

Loudspeaker amplifier (LSI1/LSI2 and QLS1/QLS2) pins 5/6, 21/22

The TEA1085 has symmetrical inputs at LSI1 and LSI2. The input signal is normally taken from the earpiece output of the transmission circuit via a resistive attenuator (see Fig.3). The amount of attenuation must be chosen in accordance with the receive gain of the transmission IC (which depends on the sensitivity of the earpiece transducer). The maximum input signal level is 450 mV(rms) at $T_{amb} = +25\ ^{o}C$.
The outputs QLS1 and QLS2 can be used for single ended drive (SE) or bridge tied load drive (BTL). The output stages have been optimized for use with a 50 Ω loudspeaker (eg Philips type AD2071).
The gain of the amplifier is fixed to ≈ 35 dB for the SE drive and ≈ 41 dB for the BTL drive (when the inputs for logic control are left open-circuit or are connected to V_{SS}).
The volume control can be obtained by using a potentiometer at the input and/or by the logic control function.

Logic gain control (GSC1 and GSC2) pins 7 and 8

The logic inputs GSC1 and GSC2 can be used to reduce the gain of the loudspeaker amplifier by means of the logic gain control function in 3 steps of 6 dB.

Table 1 Data for microcontroller drive of logic inputs

GSC2	GSC1	gain (dB)	gain reduction (dB)
0	0	35	0
0	1	29	6
1	0	23	12
1	1	17	18

Where:

0 = connection to V_{SS} or left open-circuit

1 = applying a voltage $\geqslant V_{SS} + 1.5$ V

Dynamic limiter (DLC) pin 23

To prevent distortion of the signal at the loudspeaker outputs the gain of the amplifier is reduced rapidly when:

- the peaks of the signal at the loudspeaker outputs exceed an internally determined threshold (voltage limiter)
- the DC current into SUP is insufficient (current limiter)
- the voltage at V_{BB} decreases below an internally determined threshold, typically 2.9 V (V_{BB} limiter)

The time in which the gain reduction is effected is the 'attack time'; this is very short in the first and third instance and relatively long in the second instance. The circuit will remain in the gain-reduced condition until the peaks of the output signal remain below the threshold level. The gain will then return to a nominal level after a time determined by the capacitor connected to DLC (release time).

MUTE input (MUTE) pin 20

The MUTE function is provided with a toggle function and is designed to switch between the standby condition and the listening-in condition on the rising edge of the input MUTE signal (see Fig.6).
In the basic application the MUTE input must be LOW (connected to V_{SS}). A simple push-button can be used to operate the MUTE toggle (see Fig.7). Debouncing can be realized by means of a small capacitor connected between MUTE and V_{SS}.
An internal start circuit ensures that the circuit always starts up in the standby condition.

DEVELOPMENT DATA

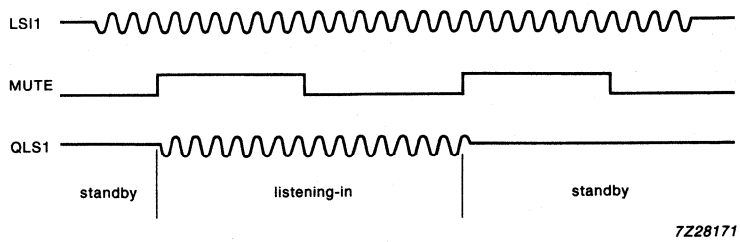
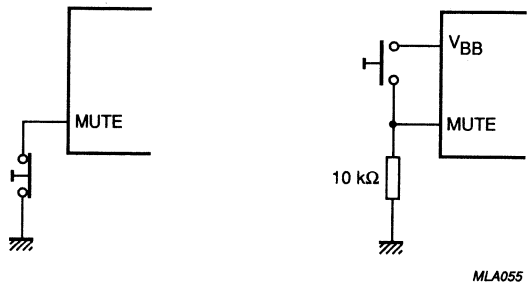


Fig.6 MUTE toggle function.



(a) Break contact. (b) Make contact.

Fig.7 MUTE switch alternatives.

Power down input (PD) pin 19

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, thereby breaking the supply to the transmission and listening-in circuits. The capacitor connected to V_{BB} provides the supply for the listening-in circuit during the supply breaks.
By making the PD input HIGH during the loop break the requirement on the capacitor is eased and, consequently, the internal (standby) current consumption I_{BBO} (Fig.4) at V_{BB} is reduced from 3.8 mA to 400 μA typical. So that the transmission circuit is not affected transistors TR1 and TR2 are inhibited and the bias current is reduced from $\approx$ 0.4 mA to $\approx$ 55 μA with V_{SUP} = 4.5 V in the following equation:

$I_{SUP(PD)} = I_{BIAS(PD)} = (V_{SUP} - 2V_d)/Ra$
(where $4.2\ V < V_{SUP} < V_{BB} + 3\ V$)

$2V_d$ = the voltage drop across 2 internal diodes ($\approx$ 1.3 V)

Ra = an internal resistor of typical 60 kΩ

Larsen limiter current stabilizer (SIC) pin 17

A current reference is set by resistor R36 between SIC and V_{SS}.
The preferred value is 120 kΩ. The internal reference current is given by the following equation:

$I_{SIC} = 1.25/R36$; when R36 = 120 kΩ, I_{SIC} = 10.5 μA

Changing the value of R36 will affect the timing of the Larsen level limiter system.

Larsen limiter preamplifier (LAI1/LAI2 and QLA) pins 9/10 and 11

This circuit amplifies the microphone signal to a level suitable for the Larsen limiter detector. The gain is set by external components (see Fig.8).
Normally the gain is set to the same level as the microphone amplifier of the transmission circuit, this ensures that the output signal level at output QLA is equal to the line signal level.

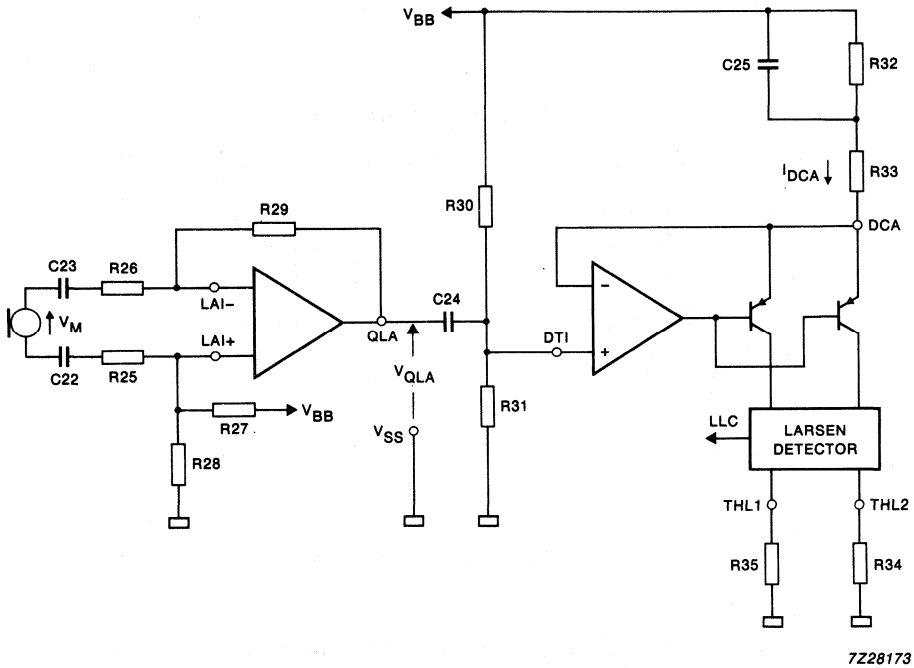


Fig.8 Larsen limiter preamplifier and voltage/current converter.

The gain between QLA and the microphone input is given by the following equation (the highpass filter is not taken into account):

$A_{pre} = V_{QLA}/V_M = R29/R26$; in the basic application R25 = R26 = 10 kΩ.

The gain can be adjusted between 30 dB (R29 = 316 kΩ) and 52 dB (R29 = 4 MΩ). The impedance result of R28 and R27 in parallel must be equal to R29 (e.g. R27 = R28 = 2 x R29).

Larsen limiter detector (DTI and DCA) pins 15 and 16

The QLA output signal is AC coupled to the detector input DTI. DTI is biased by potential divider R30 and R31. The voltage applied to DTI of the Larsen level limiter is converted into a current for further processing in this circuit. Current adjustment is achieved using the network connected between DCA and V_{BB} (see Fig.8).

The equation for DC current is:

$$I_{DCA} = \frac{R30}{R30 + R31} \times V_{BB} \times \frac{1}{R32 + R33}$$

DEVELOPMENT DATA

The equation for AC current is:

$$i_{DCA} = \frac{V_{DTI}}{R33} \text{ for } f >> 1/2\pi R33C25$$

In the basic application:

R30 = 100 kΩ, R31 = 220 kΩ, R33 = 500 Ω, R32 = 100 kΩ and C25 = 330 nF

This results in I_{DCA} = 11 μA and the equation $\frac{i_{DCA}}{V_{DTI}}$ = 2 (mA/V)

High-pass filter

A third order high-pass filter is created between the microphone input voltage and the current flowing into DCA. The cut-off frequencies (see Fig.9) of the three sections are:

$$f1 = \frac{1}{2\pi R_{eq} C24} \text{ where } R_{eq} = \frac{R30R31}{R30 + R31}$$

$$f2 = \frac{1}{2\pi R33C25} \qquad f3 = \frac{1}{2\pi R26C23} = 1/(2\pi R25C22)$$

Where: R25 = R26 and C22 = C23

The filter reduces the sensitivity of the system to own speech.
Normal speech is in the frequency range 300 Hz to 3400 Hz, however, the Larsen signal normally occurs at a frequency > 3 kHz.
With the component values as used in the basic application (see Fig.16); f1 = 500 Hz, f2 = 1 kHz and f3 = 3 kHz.

$$g = \frac{i_{DCA}}{V_m}$$

$$g_O = \frac{A_{pre}}{R33}$$

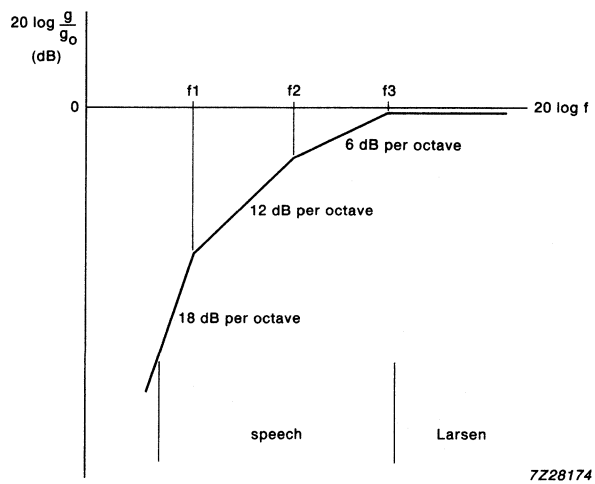


Fig.9 Third-order high-pass filter.

Larsen limiter capacitor (LLC) pin 12

An 1 μF capacitor (C26) is connected externally between V_{SS} and LLC to determine the attack and release timing of the Larsen level limiter in the listen-in and Larsen mode. The timing is also dependent on the value of the resistor connected between SIC and V_{SS}.

Larsen level limiter threshold (THL1 and THL2) pins 13 and 14

When the signal at DTI exceeds the first threshold level the capacitor connected to LLC will start to discharge. The first threshold level is determined by the value of the resistor, R35, connected to THL1 and V_{SS}. The amount of discharge of C26 depends on how much the level of the signal at DTI exceeds the first threshold level (for normal speech the discharge is small).
The Larsen effect is generally defined as a signal level of $\geqslant$ 100 mV (rms) (on line) for a period of greater than 100 ms. The Larsen signal must be reduced to a low level within 200 ms. For Larsen signal levels (f > f3 in Fig.9) of $\geqslant$ 100 mV (rms) at DTI and, with the component values of Fig.16, the system will switch from the listen-in mode to the Larsen mode in a time period of 100 ms to 200 ms; consequently, the initial Larsen affect will last only for a short period of time. This reaction time is the 'attack delay time' and ensures minimal sensitivity of the system for own speech.

The first threshold level at DTI is determined by the equation:

$$V_{DTI1} = \left(\frac{1.25}{R35} - \frac{I_{DCA}}{2}\right) \times 2 \times R33 \text{ (if } f > f3 \text{ in Fig.9)}$$

where: I_{DCA} = the DC current into DCA

With the component values given in Fig.16, I_{DCA} = 11 μA thus V_{DTI1} = 18.8 mV.

Listen-in mode

During normal speech the discharge of the capacitor connected to LLC is not sufficient to reach the threshold level whereby the system switches to the Larsen mode. This is because normal speech is not continuous, the discharge of C26 is slow (attack delay) and the charge is fast.
The slope of V_{LLC} during charge is given in the equation:

$$S_{1i} = \frac{\Delta V_{LLC}}{\Delta_t} = \frac{1.25}{C26 \times R36} \text{ (V/s)}$$

With C26 = 1 μF and R36 = 120 kΩ this results in S_{1i} = 10 V/s.

Discharge of the capacitor at LLC occurs when the signal at DTI exceeds V_{DTI1}, thus for a continuous signal at DTI the attack delay time t_{ad} (see Fig.10) is determined by the equation:

$$t_{ad} = \frac{C26 \times R36}{2 \times (3 \times k\text{-}1)} \qquad \text{Where } k = t1/T$$

The duty cycle is determined by the time in which the first threshold level (V_{DTI1}) is exceeded by the signal level at DTI (see Fig.11) thus for large signals; k $\leqslant$ 0.5.
With the component values given in Fig.16; k $\geqslant$ 0.457 for signals $\geqslant$ 100 mV (rms).
Consequently 120 ms $\leqslant t_{ad} \leqslant$ 160 ms, for $V_{DTI} \geqslant$ 100 mV (rms).

DEVELOPMENT DATA

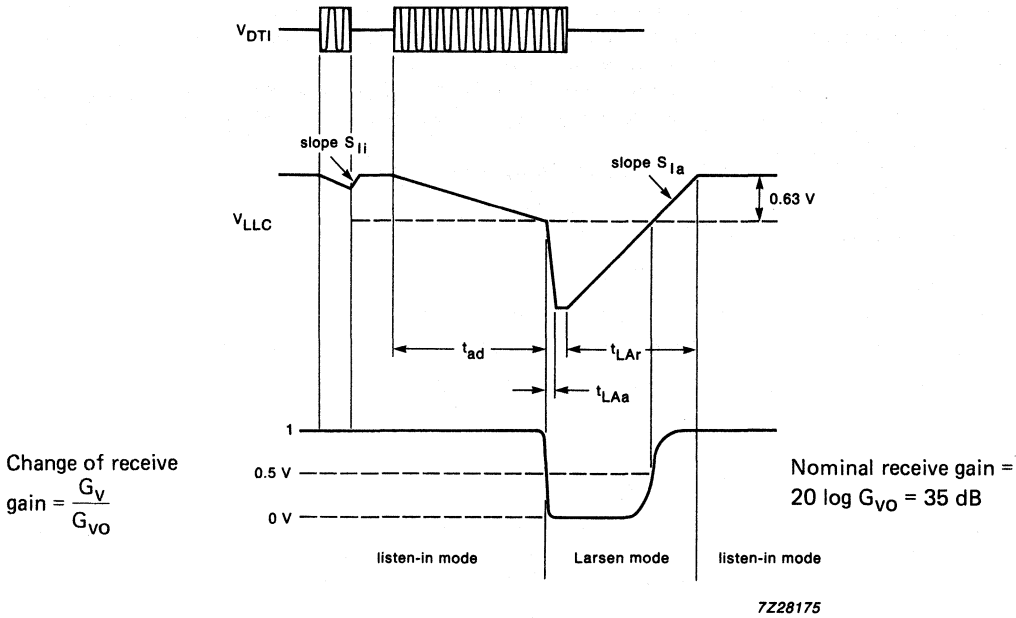


Fig.10 Dynamic behaviour of Larsen limiter (in open-loop condition).

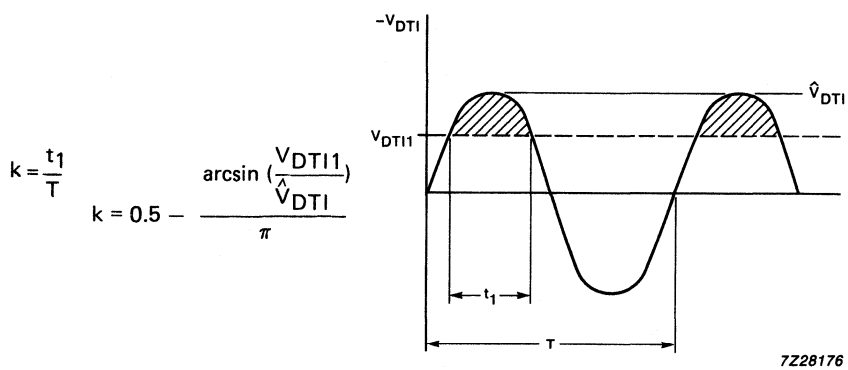


Fig.11 Definition of duty cycle k.

Larsen mode

After the 'attack delay time' the circuit switches from the listen-in mode to the Larsen mode. The gain of the loudspeaker amplifier is reduced quickly to a value (T_{LAa} = Larsen attack time see Fig.10) whereby the residual Larsen signal is determined by a second threshold level. This level can be set by resistor R34 connected between THL2 and V_{SS}. The second threshold level must always be selected at a lower level than the first threshold level thus R34 > R35.
The time taken to effect gain reduction is very short. In the Larsen mode the circuit acts as a dynamic limiter with peak detector and regulates the gain so that the signal level at DTI is determined by the second threshold level V_{DTI2}.
The second threshold level at DTI is determined by the equation:

$$V_{DTI2} = \left(\frac{1.25}{R34} - \frac{I_{DCA}}{2} \right) \times 2 \times R33 \quad (\text{if } f > f3 \text{ in Fig.9})$$

where: I_{DCA} = the DC current into DCA

With the component values given in Fig.16, V_{DTI2} = 6.9 mV.

The charge current in the Larsen mode is reduced to half the charge current in the listen-in mode.

The slope of V_{LLC} during charge (see Fig.10) is given in the equation:

$$S_{la} = \frac{\Delta V_{LLC}}{\Delta_t} = \frac{1.25}{2 \times C26 \times R34} \text{ (V/s)}$$

Where: C26 = 1 μF and R36 = 100 kΩ, S_{la} = 5 V/s

When the Larsen effect stops (total open loop gain < 1) the gain of the loudspeaker amplifier will return to its normal value in a time period known as the 'Larsen release time' (t_{LAr}). This time period is determined by capacitor C26 connected to LLC and resister R36 connected to SIC.

Where: C26 = 1 μF and R26 = 120 kΩ, t_{LAr} = 250 ms

In practice the choice of the threshold levels (determined by R35 and R34) depends on the sensitivity of the microphone and loudspeaker, the send and receive gains, sidetone suppression and the acoustical properties which are determined by the cabinet of the telephone set.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

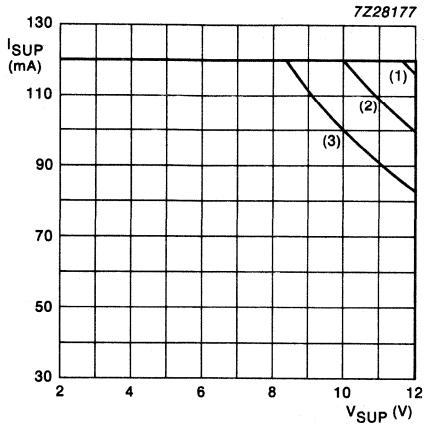
parameter	conditions	symbol	min.	max.	unit
Supply voltage					
continuous		V_{SUP}	–	12	V
during switch-on or line interruption		V_{SUP}	–	13.2	V
Repetitive supply voltage from 1 ms to 5 s with 12 Ω current limiting resistor in series with supply		V_{SUP}	–	28	V
Supply reference voltage		V_{SREF}	V_{SS}–0.5	V_{SUP}+0.5	V
Voltage on all other pins		V	V_{SS}–0.5	V_{BB}+0.5	V
Supply current					
TEA1085	Fig.12	I_{SUP}	–	120	mA
TEA1085T	Fig.13	I_{SUP}	–	120	mA
Total power dissipation	T_{amb} = 75 °C T_j = 125 °C				
TEA1085		P_{tot}	–	1	W
TEA1085T		P_{tot}	–	666	mW
Storage temperature range		T_{stg}	–40	+ 125	°C
Operating ambient temperature range		T_{amb}	–25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

THERMAL RESISTANCE

From junction to ambient in free air

TEA1085 $R_{th\ j\text{-}a}$ = 50 K/W

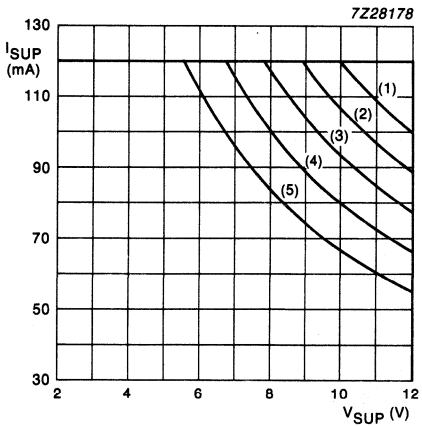
TEA1085T mounted on a glass epoxy board 40.1 x 19.1 x 1.5 mm $R_{th\ j\text{-}a}$ = 75 K/W



	T_{amb}	P_{tot}
(1)	55 °C	1.4 W
(2)	65 °C	1.2 W
(3)	75 °C	1.0 W

Fig.12 TEA1085 safe operating area.

DEVELOPMENT DATA



	T_{amb}	P_{tot}
(1)	35 °C	1.2 W
(2)	45 °C	1.07 W
(3)	55 °C	0.93 W
(4)	65 °C	0.8 W
(5)	75 °C	0.666 W

Fig.13 TEA1085T safe operating area.

CHARACTERISTICS

V_{SREF} = 4.2 V; V_{SS} = 0 V; I_{SUP} = 15 mA; V_{SUP} = 0 V(rms); f = 800 Hz; T_{amb} = 25 °C; PD = LOW; MUTE = OFF (listen-in mode); GSC1 = GSC2 = LOW; 50 Ω loudspeaker; no R38; test circuit Fig.14; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
SUPPLY						
Minimum DC input voltage		V_{SUP}	–	V_{BB}+0.7	–	V
Internal reference voltage		$V_{SUP-SREF}$	275	315	355	mV
Stabilized supply voltage	no R38; I_{SUP} = 15 mA	V_{BB}	3.4	3.6	3.8	V
variation from I_{SUP} = 15 to 120 mA	R38 = 39.2 kΩ between pins V_{SS} and VA; V_{SREF} = 5.2 V; I_{SUP} = 15 mA	ΔV_{BB}	–	10	–	mV
		V_{BB}	4.2	4.45	4.7	V
variation with temperature	no R38; I_{SUP} = 15 mA	$\Delta V_{BB}/\Delta T$	*	−0.2	*	mV/K
Minimum operating current		I_{SUP}	–	4.2	*	mA
Distortion of AC signal on SUP	$V_{SUP(rms)}$ = 1 V	THD	–	0.3	–	%
Noise between SUP and V_{EE}		$V_{no(rms)}$	–	72	–	dBmp
Current consumption in power-down condition	PD = HIGH					
	V_{SUP} = 4.5 V	I_{SUP}	–	55	75	μA
	V_{BB} = 3.6 V	I_{BB}	–	400	*	μA
LOUDSPEAKER AMPLIFIER INPUTS LSI1 AND LSI2						
Input impedance	single ended	$\|Z_i\|$	7.5	9.5	11.5	kΩ
	differential	$\|Z_i\|$	15	19	23	kΩ
Voltage gain with 50 Ω load	I_{SUP} = 15 mA; V_i = 1.8 mV(rms)					
	single ended	G_V	34	35	36	dB
	BTL output	G_V	39.9	40.9	41.9	dB
Variation with signal level	V_i = 1.8 mV(rms) and 14 mV(rms); I_{SUP} = 50 mA;					
	single ended	ΔG_V	–	+ 0.1	0.4	dB
	BTL output	ΔG_V	–	+ 0.2	0.4	dB

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
Variation with frequency referred to 1 kHz	f = 300 Hz and 3400 Hz; V_i = 1.8 mV(rms);					
	single ended	ΔG_V	–	± 0.1	–	dB
	BTL output	ΔG_V	–	± 0.1	–	dB
Variation with temperature referred to 25 °C	T_{amb} = −25 to + 75 °C;					
	single ended	ΔG_V	–	± 0.4	–	dB
	BTL output	ΔG_V	–	± 0.5	–	dB
LOUDSPEAKER OUTPUTS						
QLS1 and QLS2						
Output voltage single ended	V_i = 22 mV(rms); I_{SUP} = 9 mA note 1	$V_{O(p-p)}$	1.2	1.45	–	V
	I_{SUP} = 17 mA note 2	$V_{O(p-p)}$	2.5	2.9	–	V
bridge tied load	I_{SUP} = 23.5 mA note 2	$V_{O(p-p)}$	2.5	2.9	–	V
	I_{SUP} = 32.0 mA note 3	$V_{O(p-p)}$	3.5	4.0	–	V
Total harmonic distortion	V_i = 22 mV(rms);					
single ended	I_{SUP} = 9 mA	THD	–	0.4	2	%
	I_{SUP} = 17 mA	THD	–	0.7	2	%
bridge tied load	I_{SUP} = 23.5 mA	THD	–	0.4	2	%
Output voltage single ended	V_i = 22 mV(rms); I_{SUP} = 17 mA					
	V_{SUP}-V_{EE} = 1 V(rms)	$V_{O(p-p)}$	2.2	2.55	–	V
Dynamic limiter						
Total harmonic distortion	V_i = 22 mV(rms) + 10 dB					
single ended	I_{SUP} = 9 mA	THD	–	0.5	10	%
	I_{SUP} = 17 mA	THD	–	1.2	10	%
bridge tied load	I_{SUP} = 23.5 mA	THD	–	0.6	10	%
Dynamic behaviour of limiter (single ended load)						
Attack time; V_i jumps from 10 mV(rms) to 65 mV(rms)						
voltage limiter	I_{SUP} = 17 mA	t_{att}	–	2	5	ms
current limiter	I_{SUP} = 12 mA	t_{att}	–	500	*	ms
V_{BB} limiter	I_{SUP} = 9 mA	t_{att}	–	10	–	ms

* Value to be fixed.

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Release time; V_i jumps from 65 mV(rms) to 10 mV(rms)	I_{SUP} = 17 mA	t_{rel}	*	75	*	ms
Threshold V_{BB} limiter below which gain reduction starts	I_{SUP} = 9 mA	V_{BBO}	*	2.95	*	V
Noise output voltage	1 kΩ between inputs LSI1, LSI2; psophometrically weighted (P53 curve)					
single ended		$V_{no(rms)}$	–	170	–	μV
bridge tied load		$V_{no(rms)}$	–	350	–	μV
LOGIC GAIN CONTROL						
Reduction of voltage gain	V_I = 1.8 mV(rms)					
GSC2 = 0, GSC1 = 1		ΔG_v	5.8	6.3	6.8	dB
GSC2 = 1, GSC1 = 0		ΔG_v	11.6	12.1	12.6	dB
GSC2 = 1, GSC1 = 1		ΔG_v	17	18	19	dB
LARSEN LIMITER PREAMPLIFIER						
Operational amplifier						
open loop gain		G_{v0}	–	92	–	dB
1st pole		f_{P1}	–	120	–	Hz
2nd pole		f_{P2}	–	3.3	–	MHz
unity gain bandwidth		G_B	–	4	–	MHz
Voltage gain	f = 3 kHz R26 = 10 kΩ R29 = 4 MΩ	G_v	51.5	52.0	52.5	dB
Gain adjustment range		G_v	30	–	52	dB
LARSEN LIMITER DETECTOR						
Voltage to current convertor DC offset voltage	V_{BB}-V_{DTI} = 1 V	V_{DCA}-V_{DTI}	–25	1	+ 25	mV
Voltage gain from DTI to DCA	V_{DTI} = 100 mV(rms); f = 3 kHz	G_v	*	–0.8	*	dB
DC voltage at THL1	R35 = 51 kΩ	V_{THL1}	1.8	1.25	1.33	V
DC voltage at THL2	R34 = 100 kΩ	V_{THL2}	1.8	1.25	1.33	V
Dynamic behaviour with a burst at DTI	f = 3 kHz		see Fig.15			
Listen-in release time	see Fig.15(a)	t_{LIr}	*	40	*	ms

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
Attack delay time V_{DTI} jumps from:	see Fig.15(b)					
0 to 100 mV (RMS value)		t_{ad}	–	160	200	ms
0 to 1 V (RMS value)		t_{ad}	100	120	–	ms
Larsen attack time	see Fig.15(b); V_{DTI} = 100 mV(rms)	t_{LAa}	–	20	*	ms
Larsen release time V_{DTI} jumps from 100 mV to 0 mV (RMS value)		t_{LAr}	*	250	*	ms
DC voltage at LLC	V_{DTI} = 0 V	V_{LLC}	1.8	1.9	2.0	V
Reduction of V_{LLC} to attack Larsen mode		$-\Delta V_{LLC}$	0.59	0.63	0.68	V
Gain reduction	V_{LLC} = 0.7 V	ΔG_v	60	*	*	dB
MUTE INPUT						
(toggle function, positive edge triggered set-reset flip-flop)						
Input voltage LOW		V_{IL}	0	–	0.3	V
Input voltage HIGH		V_{IH}	1.5	–	V_{BB}+0.4	V
Input current	MUTE = LOW	I_{MUTE}	–	–22	–28	μA
Minimum input pulse width		t	–	50	–	μs
Minimum pulse repetition time		P_R	–	2	–	ms
Supply voltage below which MUTE toggle is reset		$V_{BB(MUTE)}$	*	2	*	V
Reduction of gain from LSI1, LSI2 to QLS1, QLS2	MUTE = ON	ΔG_v	60	100	–	dB
POWER DOWN INPUT						
Input voltage LOW		V_{IL}	0	–	0.3	V
Input voltage HIGH		V_{IH}	1.5	–	V_{BB}+0.4	V
Input current	PD = HIGH	I_{PD}	–	2.3	2.8	μA
LOGIC INPUTS						
GSC1 and GSC2						
Input voltage LOW		V_{IL}	0	–	0.3	V
Input voltage HIGH		V_{IH}	1.5	–	V_{BB}+0.4	V
Input current	GSC = HIGH	I_{GSC}	–	6	8	μA

DEVELOPMENT DATA

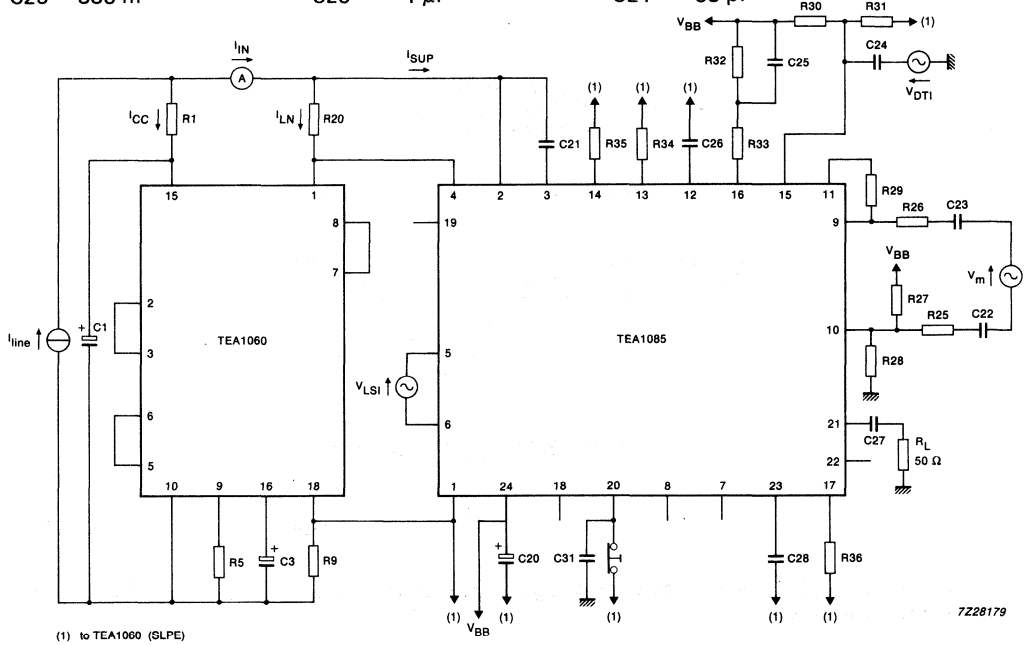
* Value to be fixed.

Notes to the characteristics

1. Typical output power is 5 mW into 50 Ω.
2. Typical output power is 20 mW into 50 Ω.
3. Typical output power is 40 mW into 50 Ω.

Component values for Test circuit in Fig.14

R1 = 620 Ω	R5 = 3.6 kΩ	R9 = 20 Ω
R20 = 150 Ω	R35 = 51 kΩ	R34 = 100 kΩ
R33 = 500 Ω	R32 = 100 kΩ	R30 = 100 kΩ
R31 = 220 kΩ	R29 = 4 MΩ	R36 = 10 kΩ
R25 = 10 kΩ	R27 = 8 MΩ	R28 = 8 MΩ
R36 = 120 kΩ	R24 = 1 kΩ	
C1 = 100 μF	C3 = 4.7 μF	C31 = 10 nF
C20 = 470 μF	C28 = 330 nF	C27 = 220 μF
C22 = 2.2 μF	C23 = 2.2 μF	C24 = 100 nF
C25 = 330 nF	C26 = 1 μF	C21 = 68 pF

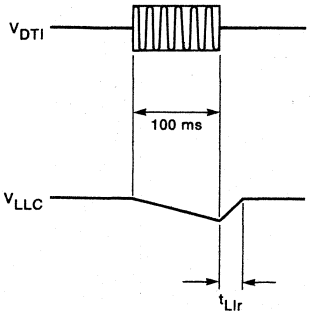


The DC current is divided as follows:

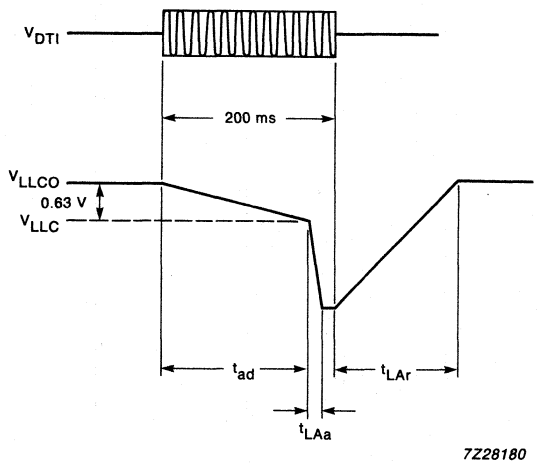
$$I_{SUP} = I_{IN} - \frac{V_{SUP\text{-}SREF}}{R20} \qquad I_{LN} = \frac{V_{SUP\text{-}SREF}}{R20}$$

The pins not shown in the TEA1060 are left open. An impedance in series with pin SUP (e.g. an ammeter) should be avoided as it interferes with the value of I_{LN}.

Fig.14 Test circuit.



(a) Listen-in release time (t_{LIr}); V_{DTI} = 100 mV(rms); f = 3 kHz.



(b) Attack delay (t_{ad}), Larsen attack time (t_{LAa}), Larsen release time (t_{LAr}); V_{DTI} = 100 mV(rms) and 1 V(rms); f = 3 kHz.

Fig.15 Test signals for Larsen level limiter.

APPLICATION INFORMATION

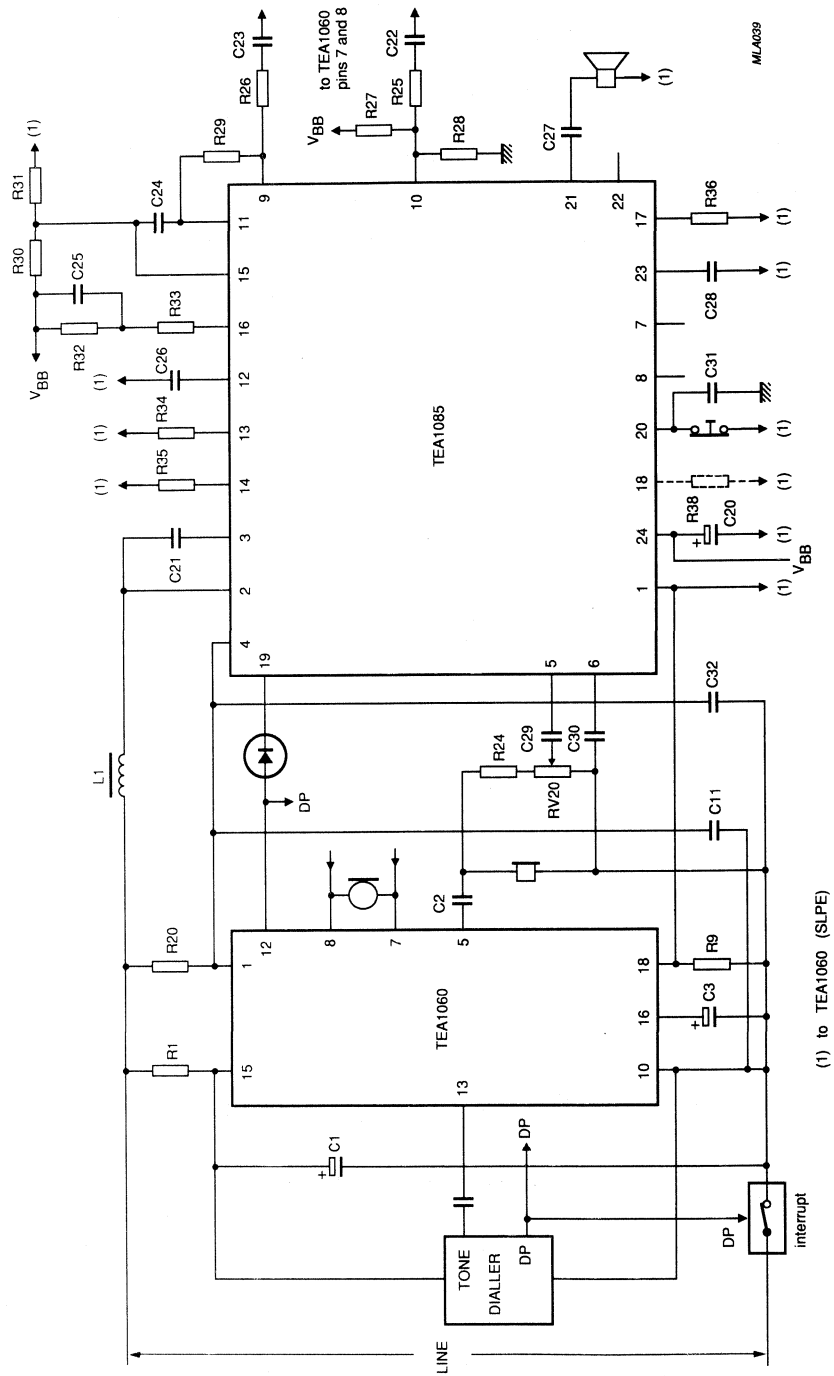


Fig.16 Basic application of TEA1085 and TEA1060.

APPLICATION INFORMATION (continued)

The basic application circuit of the TEA1085 is illustrated in Fig.16. Only the most important components of the TEA1060 part are shown, other components and their values are given in the TEA1060 Data sheet.

The supply pin (V_{BB}) of the TEA1085 can also be used to supply peripheral circuits (e.g. microcontrollers, diallers, etc.).

Further information will be published in the TEA1085 application report.

Component values

R20 = 150 Ω	R35 = 51 kΩ	R34 = 100 kΩ
R33 = 500 Ω	R32 = 100 kΩ	R30 = 100 kΩ
R31 = 220 kΩ	R29 = 1.65 MΩ*	R26 = 10 kΩ
R25 = 10 kΩ	R27 = 3.3 MΩ*	R28 = 3.3 MΩ*
R36 = 120 kΩ	R24 = 1 kΩ*	
C20 = 470 μF	C28 = 330 nF	C27 = 47 μF
C22 = 4.7 nF	C23 = 4.7 nF	C24 = 4.7 nF
C25 = 330 nF	C26 = 1 μF	C21 = 47 pF
C31 = 10 nF	C29 = 220 nF	C30 = 220 nF
C11 = 4.7 nF		
RV20 = 1 kΩ*	L1 = 150 μH	

DEVELOPMENT DATA

* Value depends on the gain setting of the transmission circuit.

LOW POWER DIGITAL PAGING RECEIVER

GENERAL DESCRIPTION

The UAA2033T is a very low power radio receiver circuit for use in VHF paging receivers (30 to 174 MHz) of wide-area digital paging systems employing direct FM non-return-to-zero (NRZ) frequency-shift keying (FSK) modulation.

Used in conjunction with the PCA5000T decoder for POCSAG paging systems, it offers an extremely advanced radio paging concept.

The receiver design is based on the offset receiver principle which gives improved performance, lower power consumption and requires less external components than the two-branch type of receiver architecture found in presently available ICs. The receiver provides fully filtered and squared data to drive the decoder device and can be turned off completely by external inputs.

Features

- Wide operating supply voltage range
- Low current consumption
- Fully compatible with world-wide POCSAG paging systems
- Receiver power externally addressable
- High sensitivity
- Low battery voltage detector
- Uses low cost crystal
- Automatically tracks offsets in the input frequency

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_P = V_{14-15}$	2,0	2,7	3,5	V
Supply current		I_{14}	2,2	2,7	3,3	mA
Sensitivity	10^{-2} bit error rate	EMF/2	–	–	0,3	μV
Operating ambient temperature range		T_{amb}	−10	–	+70	°C

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

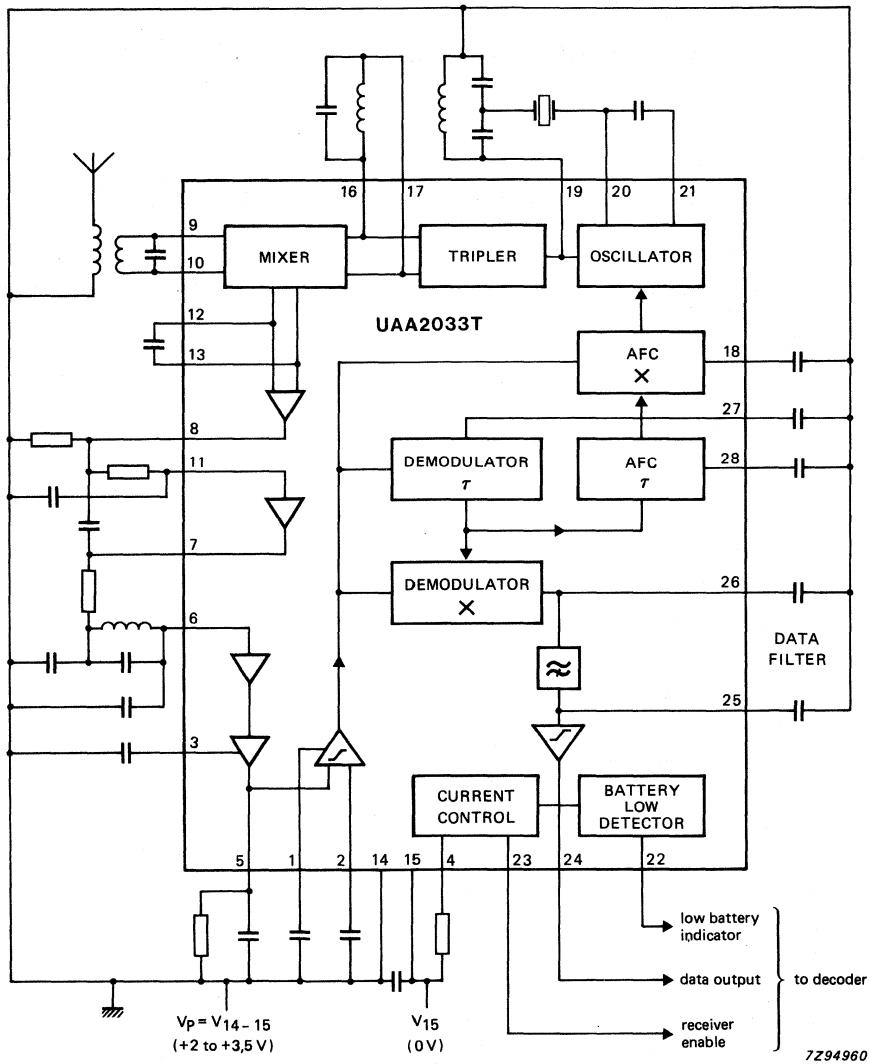


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

pin	description
1	low frequency filter '3' (limiter decoupling '2')
2	low frequency filter '2' (limiter decoupling '1')
3	low frequency filter '1'
4	current control (internal reference)
5	IF filter
6	IF filter
7	IF filter
8	IF filter
9	mixer input '2'
10	mixer input '1'
11	IF filter
12	mixer output 'B'
13	mixer output 'A'
14	supply voltage (positive)
15	supply voltage (negative)
16	tripler coil '2'
17	tripler coil '1'
18	AFC '2'
19	oscillator output
20	oscillator input
21	oscillator AFC range
22	low battery voltage indicator
23	receiver enable
24	data output
25	data filter '2'
26	data filter '1'
27	demodulator centre frequency
28	AFC '1'

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	$V_P = V_{14-15}$	−0,3	8,0	V
Operating ambient temperature range	T_{amb}	−10	+70	°C
Storage temperature range	T_{stg}	−55	+125	°C

DC CHARACTERISTICS

V_P = 2,0 to 3,5 V; T_{amb} = −10 to +70 °C; typical values measured at T_{amb} = 25 °C, V_P = 2,7 V; test circuit as Fig. 3 with L4 short circuited, no RF input and crystal XL1 removed

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_P = V_{14-15}$	2,0	2,7	3,5	V
Supply current	pin 23 = HIGH	I_{14}	2,2	2,7	3,3	mA
	pin 23 = LOW	I_{14}	–	–	1,0	μA
Receiver enable (pin 23)						
Input voltage HIGH		V_{23-15}	V_P–0,6	–	–	V
Input voltage LOW	I_{14} = 1 μA	V_{23-15}	–	–	0,4	V
Input current HIGH		I_{23}	–	+1	–	μA
Input current LOW		I_{23}	–	−1	–	μA
Data output (pin 24)						
Output voltage HIGH		V_{24-15}	V_P–0,7	–	–	V
Output voltage LOW	I_{24} = ±10 μA	V_{24-15}	–	–	0,5	V
Low battery voltage indicator (pin 22)						
Detection voltage	note 1	V_{DET}	2,035	2,135	2,235	V
Output voltage HIGH	I_{22} = ±5 μA	V_{22-15}	V_P–0,5	–	–	V
Output voltage LOW	I_{22} = ±5 μA	V_{22-15}	–	–	0,5	V

AC CHARACTERISTICS

V_P = 2,0 to 3,5 V; T_{amb} = −10 to +70 °C; typical values measured at T_{amb} = 25 °C, V_P = 2,7 V; test circuit as Fig. 3 with f = 173,950 MHz; channel spacing = 25 kHz; deviation = ±4,5 kHz; bit rate = 512 b/s (256 Hz square wave); AFC frequency limits 173,948 and 173,952 MHz; see Tuning Procedure

parameter	conditions	symbol	min.	typ.	max.	unit
RF sensitivity and AFC performance						
Sensitivity for 10^{-2} bit error rate (note 2)	T_{amb} = 25 °C	EMF/2	–	–	0,30	μV
	T_{amb} = −10 to +70 °C	EMF/2	–	–	0,43	μV
Bit error rate	EMF/2 = 1 μV	BER	–	10^{-3}	–	
Data output (pin 24)						
Duty factor	EMF/2 = 100 μV; f = 174 MHz	δ	35	–	55	%
Transition time	EMF/2 = 100 μV; f = 174 MHz; R_L = 1 MΩ; C_L = 100 pF	t_T	–	–	50	μs

Notes to the characteristics

1. V_{22-15} goes HIGH if V_P is less than V_{DET}.
2. Sensitivity measurement.

   A simple digital method of performing an approximate bit error rate (BER) measurement with a counter is shown in Fig. 2. At high signal levels (10 μV) the counter should read the exact frequency of the data input to the signal generator. As the signal level is reduced, errors occur at the receiver output and effectively increase the output frequency read by the counter (error duration is nearly always less than a bit length).

   For a bit error rate of 1 in a 100 on a 512 b/s system, the counted frequency will increase from 256 Hz at high signal levels to 261 Hz when the input signal level is reduced to the 1 in a 100 BER point.

Tuning procedure for AC tests

1. After performing the DC tests, set up the device in the AC test circuit as per Fig. 3.
2. Connect pin 18 to a voltage source of $V_{18-14} = -0{,}59$ V. Measure the oscillator frequency with a counter connected to the link winding of L3.
   Tune C21 (crystal frequency trimmer) to set the crystal oscillator to a frequency of:

$$\frac{\text{received frequency} + 2\text{ kHz}}{3} \pm 100\text{ Hz}.$$

   For a received frequency of 173,950 MHz the oscillator frequency is 57,984 MHz.
3. Remove test voltage source and turn on the signal generator (f = 173,950 MHz, deviation = ± 4,5 kHz, 256 Hz square-wave modulation, RF input level = 3 mV).

   Monitor the audio amplitude at pin 5 using an oscilloscope with an AC sensitivity of at least 2 mV per division.

Note that in the following tests the RF signal generator level should be reduced as the receiver is tuned to ensure that the peak-to-peak audio output voltage at pin 5 lies between 20 mV and 100 mV.

4. Tune C22 (tripler) to obtain peak audio output voltage at pin 5. The tuning will be found to have a discontinuity on one side of the peak response, i.e. the level will drop much faster on one side of the peak than on the other. Therefore when setting C22 ensure that it is not set too close to the discontinuity.
5. Tune C3 (mixer input) to obtain a peak audio output on pin 5.
6. Disconnect the frequency counter from the oscillator output. Measure the voltage on pin 18 and check that it is within the range −0,57 to −0,61 V. If it is outside this range then adjust C21 (oscillator trimmer) until it comes within the limits.
7. Check with an oscilloscope that clean data is appearing on DATA OUTPUT (pin 24) and proceed with the AC tests.

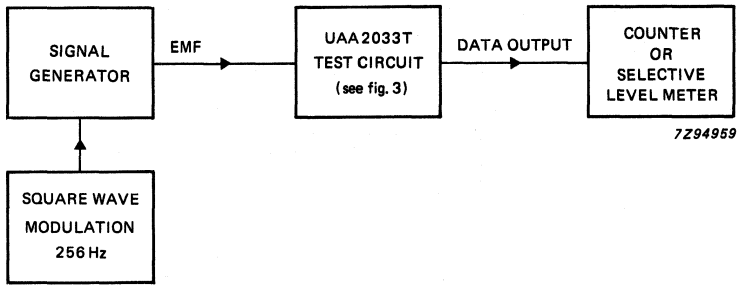


Fig. 2 Bit error rate measurement: signal generator frequency (f) = 173,95 MHz ; input impedance of counter or selective level meter greater than 100 kΩ.

DEVELOPMENT DATA

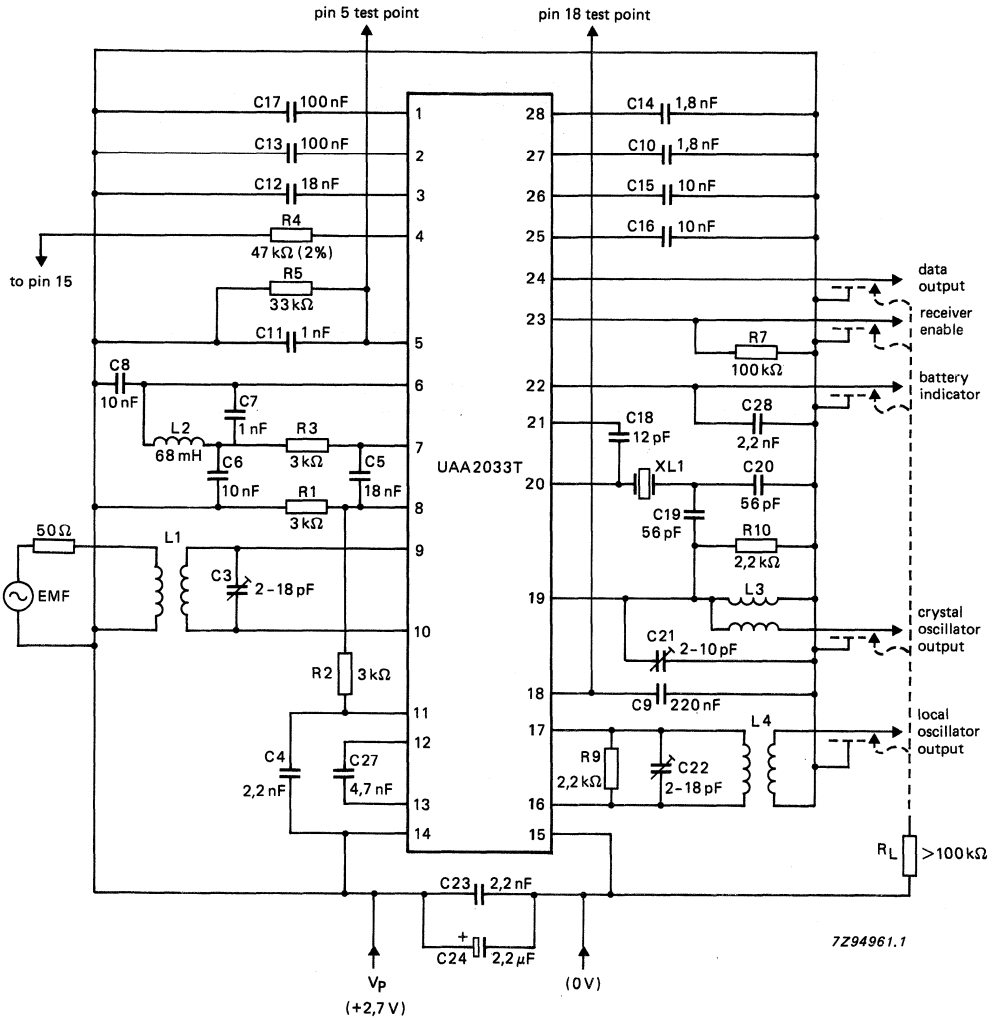


Fig. 3 Test circuit.

Coil data

L1, L3 and L4 wound with 0,315 mm enamelled wire on Toko ϕ 4,5 mm diameter former without pot or core. Screening cans also used.

L1 – 4 turns, one turn/groove. Link winding, 2 turns over the centre of the other winding.
L3 – 6 turns, 2 turns/groove. Link winding, 1 turn at bottom of former.
L4 – 3 turns, 1 turn/groove. Link winding, 1 turn at bottom of former.
L2 – 68 mH inductor. At 10 kHz minimum Q = 10.

Crystal (XL1) frequency 57985,90 kHz

LOW POWER DIGITAL UHF PAGING RECEIVER

GENERAL DESCRIPTION

The UAA2050T is a very low power UHF and VHF radio receiver circuit, primarily intended for use in paging receivers (27 MHz to 470 MHz) for wide-area digital paging systems employing direct FM non-return-to-zero (NRZ) frequency-shift keying (FSK) modulation.

Used in conjunction with the PCA5000T decoder for POCSAG paging systems, it offers an extremely advanced radio paging concept.

The radio receiver design is based on the offset receiver principle. The receiver provides fully filtered and squared data to drive the decoder and can be turned off completely by external inputs.

Features

- Low noise preamplifier ensuring high RF sensitivity
- Few external components required
- Low current consumption
- Wide operating supply voltage range
- Power on/off mode selectable via the enable input (RE)
- Low battery voltage detector
- Crystal controlled receiver frequency (AFC)
- Fully compatible with all FSK modulated systems (512 and 1200 bits/s)
- Uses low cost crystal

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Supply voltage range		$V_P = V_{7-15}$	1.9	–	3.5	V
Supply voltage for preamplifier		$V_{23,24-15}$	1.0	–	3.5	V
Total supply current		I_{tot}	2.25	–	3.76	mA
Supply current OFF		$-I_{OFF}$	–	–	1.0	µA
RF sensitivity (RMS value)	1 x 10^{-2} bit error rate	EMF/2	–	0.18	0.25	µV
Preamplifier noise figure	note 1; f = 470 MHz	NF	–	4.5	–	dB
Operating ambient temperature range		T_{amb}	−10	–	+70	°C

Note to the Quick reference data

1. Including the transforming network.

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

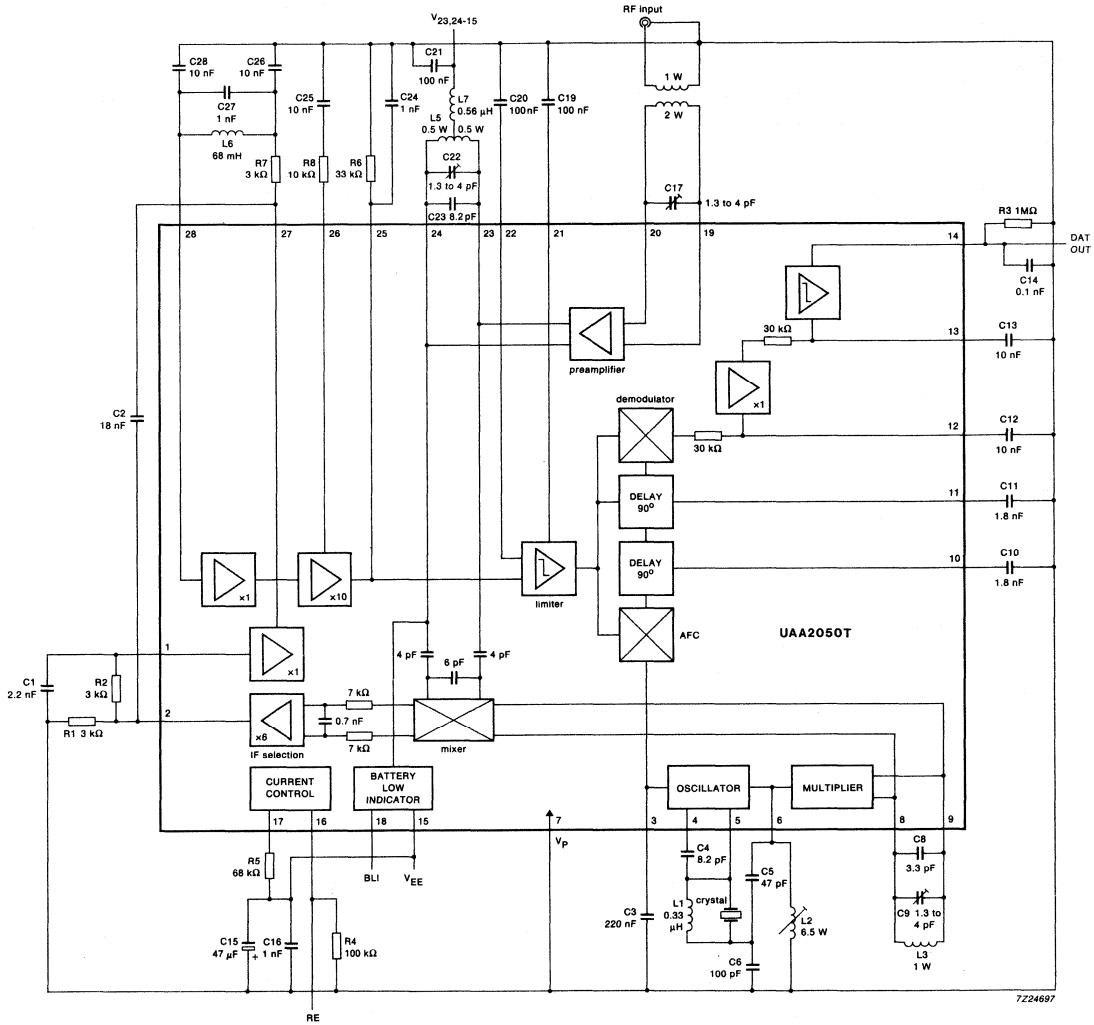


Fig.1 Block diagram (showing UHF external components).

DEVELOPMENT DATA

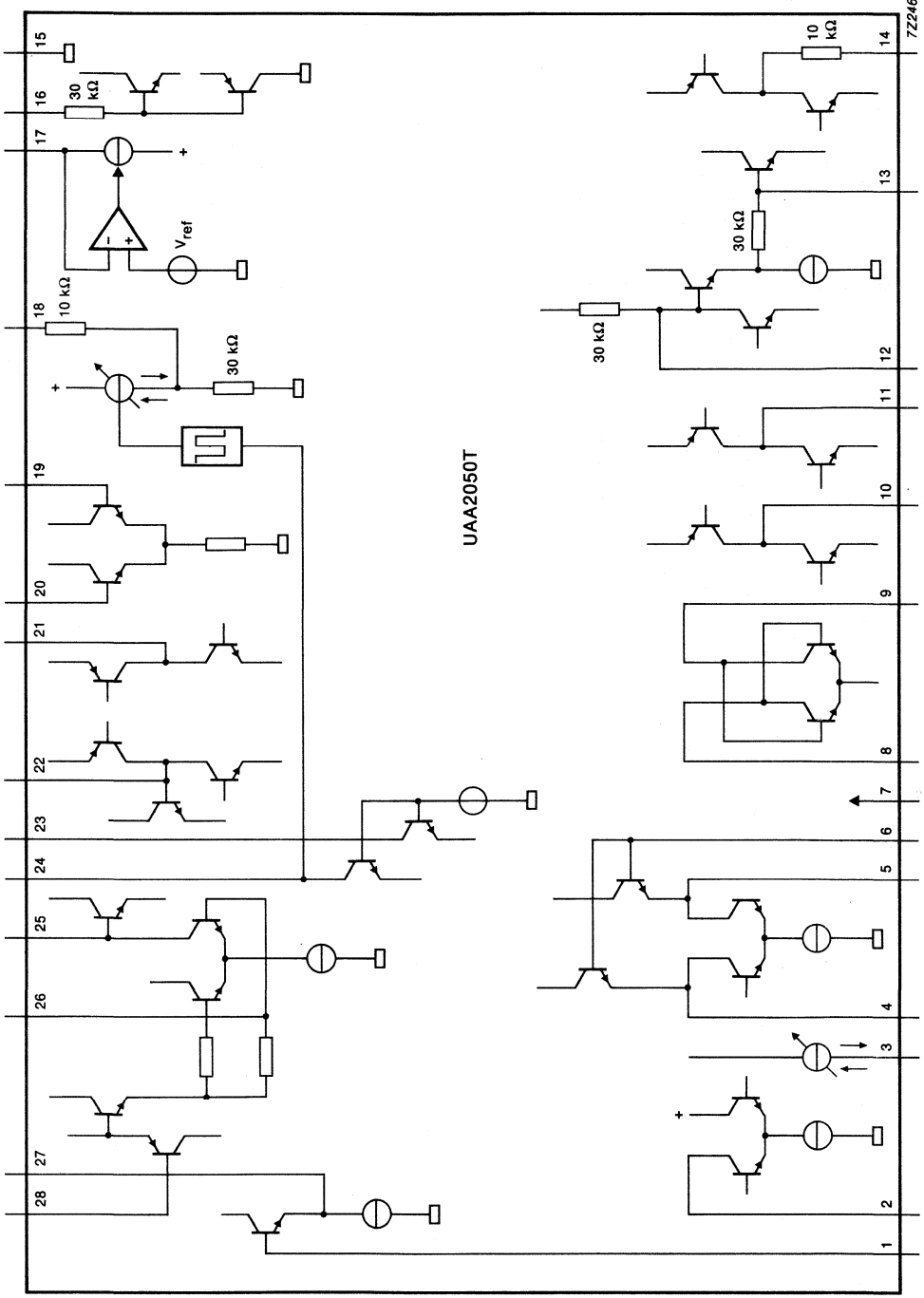


Fig.2 Pinning diagram and equivalent circuits.

PINNING

pin	mnemonic	description
1	IFF2	IF filter 2
2	IFF1	IF filter 1
3	AFC	AFC (test point 1)
4	OSC IN	oscillator input
5	OSC AFC	oscillator AFC range
6	OSC OUT	oscillator output
7	V_P	supply voltage (positive)
8	MC1	multiplier coil
9	MC2	multiplier coil
10	AFCD	AFC delay
11	DEMODD	demodulator delay
12	DAT F1	data filter 1
13	DAT F2	data filter 2
14	DAT OUT	data output
15	V_{EE}	supply voltage (negative)
16	RE	receiver enable input
17	CC	current control input
18	BLI	battery low indicator output
19	PREAMP1	preamplifier input 1
20	PREAMP2	preamplifier input 2
21	LC2	limiter decoupling 2
22	LC1	limiter decoupling 1
23	MIX1	mixer input 1 (preamplifier output)
24	MIX2	mixer input 2 (preamplifier output)
25	LIM IN	limiter input (test point 2)
26	IFF5	IF filter 5
27	IFF3	IF filter 3
28	IFF4	IF filter 4

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

parameter	condition	symbol	min.	max.	unit
Supply voltage		$V_P = V_{7-15}$	−0.3	+5.0	V
Supply voltage for preamplifier		$V_{23,24-15}$	−0.3	+5.0	V
Operating ambient temperature range		T_{amb}	−10	+70	°C
Storage temperature range		T_{stg}	−55	+125	°C
Electrostatic handling; human body model*	except pins 19 and 20	V_{ESD}	−1000	+1000	V
	only pins 19 and 20	V_{ESD}	−500	+1000	V

DEVELOPMENT DATA

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

DC CHARACTERISTICS

V_P = 2.0 V; $V_{23,24-15}$ = 1.1 V; all voltages referenced to V_{EE}; T_{amb} = −10 to +55 °C; typical values measured at T_{amb} = 25 °C; test circuit as Fig.4; L2 and L3 short-circuited; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		$V_P = V_{7-15}$	1.9	2.0	3.5	V
Supply voltage for preamplifier	$V_{23,24-15} \leqslant V_P$	$V_{23,24-15}$	1.0	1.1	3.5	V
Supply current	$V_{RE} \geqslant V_P - 0.6$ V	I_7	1.9	2.5	3.2	mA
Supply current for preamplifier	$V_{RE} \geqslant V_P - 0.6$ V	$I_{23,24}$	0.35	0.45	0.56	mA
Supply current OFF	$V_{RE} \leqslant 0.4$ V	I_{OFF}	–	–	1.0	µA
Receiver enable (RE)						
POWER-OFF MODE:						
input voltage		$V_{RE} = V_{16-15}$	–	–	0.4	V
input current	V_{RE} = 0.4 V	I_{16}	–	–	1.0	µA
POWER-ON MODE:						
input voltage		$V_{RE} = V_{16-15}$	$V_P - 0.6$ V	–	–	V
input current	V_{RE} = 1.4 V	I_{16}	–	1.0	5.0	µA
Data output (DAT OUT)						
Output voltage HIGH	$I_{14} = \pm 10$ µA	V_{14-15}	$V_P - 0.7$ V	–	–	V
Output voltage LOW	$I_{14} = \pm 10$ µA	V_{14-15}	–	–	0.5	V
Battery voltage low indicator						
Detection voltage	see Fig.3	V_{DET} V_{DET}	1.10 1.90	1.17 2.00	1.24 2.10	V V
Output voltage HIGH	1.0 V ⩽ V_{24-15} ⩽ 1.10 V; 1.85 V ⩽ V_{24-15} ⩽ 1.90 V; $I_{18} = \pm 7$ µA	V_{OH}	$V_P - 0.5$ V	–	–	V
Output voltage LOW	1.24 V ⩽ V_{24-15} ⩽ 1.65 V; 2.10 V ⩽ V_{24-15}; $I_{18} = \pm 7$ µA	V_{OL}	–	–	0.5	V

Note to the DC characteristics

1. V_{18-15} goes HIGH if V_{24-15} is less than V_{DET}.

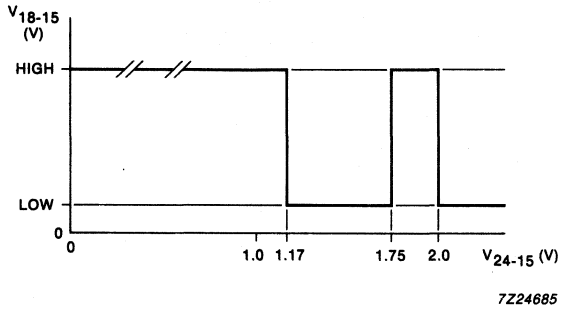


Fig.3 Typical battery low indicator thresholds.

DEVELOPMENT DATA

AC CHARACTERISTICS (UHF)

For AC test procedures refer to section 'TEST INFORMATION'. V_P = 2.0 V; $V_{23,24-15}$ = 1.1 V; all voltages referenced to V_{EE}; T_{amb} = −10 to +55 °C; typical values measured at T_{amb} = 25 °C; test circuit as Fig.4 and printed-circuit board layout as Fig.7; test signal: f = 469.200 MHz: deviation = ±4.5 kHz: modulation = 256 Hz rectangular; channel spacing = 25 kHz; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
UHF sensitivity range (RMS value)	note 1; 1 x 10^{-2} bit error rate	EMF/2	–	0.18	0.25	µV
		EMF/2	–	−122	−119	dBm
	T_{amb} = −10 to +70 °C	EMF/2	–	–	−116	dBm
Adjacent channel selectivity		αa	60	67	–	dB
	T_{amb} = −10 to +70 °C	αa	50	–	–	dB
Co-channel selectivity		αc	8	–	–	dB
Spurious response rejection		αs	55	58	–	dB
Intermodulation response		IM	50	60	–	dB
Blocking	Δf ≥ ±4 MHz	EMF	80	83	–	dBµV
AFC lock-in range		±Δf	3	–	–	kHz
Preamplifier	see Fig.9					
Noise Figure	note 2	NF	–	4.5	–	dB
Third order intercept point		IP3	–	−20	–	dBm
Available power gain		G_p	–	6	–	dB
1 dB compression point (RMS value)		EMF/2	–	10	–	mV
VHF RF sensitivity range (RMS value)	see Fig.10; f = 173.95 MHz; 1 x 10^{-2} bit error rate	EMF/2	–	0.14	–	µV
		EMF/2	–	−124	–	dBm

Notes to the AC characteristics

1. A simple digital method of performing an approximate bit error rate (BER) measurement with a counter is shown in Fig.5. At high signal levels (10 µV) the counter should read the exact frequency of the data input to the signal generator (256 Hz). As the signal level is reduced, errors occur at the receiver output and effectively changes the output frequency read by the counter (error duration is nearly always less than one bit length).
   The input signal level (V_{ref}) is reduced until the bit error rate is ≤ 1 x 10^{-2} (5 bit errors for 512 bit/s system). The frequency from the data output signal will change from 256 Hz (512 bit/s system) to 261 Hz. This RF-level is the reference for the following tests (V_{ref}).

2. Including the transforming network.

TEST INFORMATION

Tuning procedure for AC tests

1. After performing the DC tests, prepare the device for AC testing (as shown in Fig. 4).

2. Connect pin 3 to a voltage source of $V_{3-7} = -0.5$ V. Measure the multiplier frequency with a counter or spectrum analyzer connected to the link winding of L3. Tune L2 to set the crystal oscillator to a frequency of:

   $$\frac{\text{Received frequency} + 2.2\ \text{kHz}}{5} \quad (\pm 100\ \text{Hz})$$

   For a received frequency of f = 469.200 MHz, the oscillator frequency (f_{OSC}) = 93.840 MHz.

3. Remove the test voltage source and turn on the signal generator (f = 469.200 MHz; deviation = ±4.5 kHz; rectangular 256 Hz modulation; RF input level = 1 mV).

   Note During the following tests the RF signal generator level should be reduced as the receiver is tuned, to ensure the peak-to-peak output voltage at pin 25 lies between 20 mV and 100 mV.

4. Tune C9 (multiplier) to obtain a peak audio output voltage on pin 25.

5. Tune C22 (Mixer input) to obtain a peak audio output voltage on pin 25.

6. Disconnect the frequency counter from the multiplier output. Measure the voltage at pin 3 and check if it is within the range of −0.48 V to −0.52 V. If it is outside this range then adjust L2 (oscillator) until it is within the limits.

7. Check with an oscilloscope that clean data is appearing on the data output (pin 14) and proceed with the AC tests.

Test conditions

The data output signal corresponds to the sensitivity definition.

Where:

f_1 is the modulated test signal
f_2 is the unmodulated test signal
f_{cs} is the channel spacing (25 kHz)
V_1 is the signal generator 1 output
V_2 is the signal generator 2 output
V_{ref} is defined in 'Notes to the AC characteristics'.

1. Adjacent channel selectivity (see Fig.6);
   - generator 1: modulated test signal; $V_1 = V_{ref} + 3dB$
   - generator 2: unmodulated test signal; $V_2 = V_1 + 60$ dB ($f_2 = f_1 \pm \Delta f_{cs}$).

2. Co-channel selectivity (see Fig.6);
   - generator 1: modulated test signal; $V_1 = V_{ref} + 3$ dB
   - generator 2: unmodulated test signal; $V_2 = V_1 - 8$ dB ($f_2 = f_1 \pm 3$ kHz maximum).

3. Spurious response rejection (see Fig.6);
   - generator 1: modulated test signal; $V_1 = V_{ref} + 3$ dB
   - generator 2: unmodulated test signal; $V_2 = V_1 + 55$ dB (f_2 =100 kHz to 1 GHz; $|f_2 - f_1| \geqslant 2\Delta f_{cs}$).

4. Intermodulation response (see Fig.6);
   - generator 1: modulated test signal; $f_1 = 469.2$ MHz $\pm 2 \times n \times \Delta f_{cs}$) n = 1 to 4 .
   - generator 2: unmodulated test signal; $f_2 = 469.2$ MHz $\pm n \times \Delta f_{cs}$). n = 1 to 4.

   Output voltages of both generators increase with the same level, until a data output signal corresponding to the sensitivity definition is reached. The level must be 50 dB above the V_{ref} + 3 dB level.

5. Blocking (see Fig.6);
   - generator 1: modulated test signal; V_1 (EMF) = 3 dBμV
   - generator 2: unmodulated test signal; V_2 (EMF) = 80 dBμV ($f_2 = f_1 \pm \Delta f$; $\Delta f \geqslant 4$ MHz)

6. AFC lock-in-range (see Fig.5);
   - generator 1: modulated test signal; $V_1 = V_{ref} + 3$ dB ($f_1 = 469.2$ MHz ± 3 kHz)

DEVELOPMENT DATA

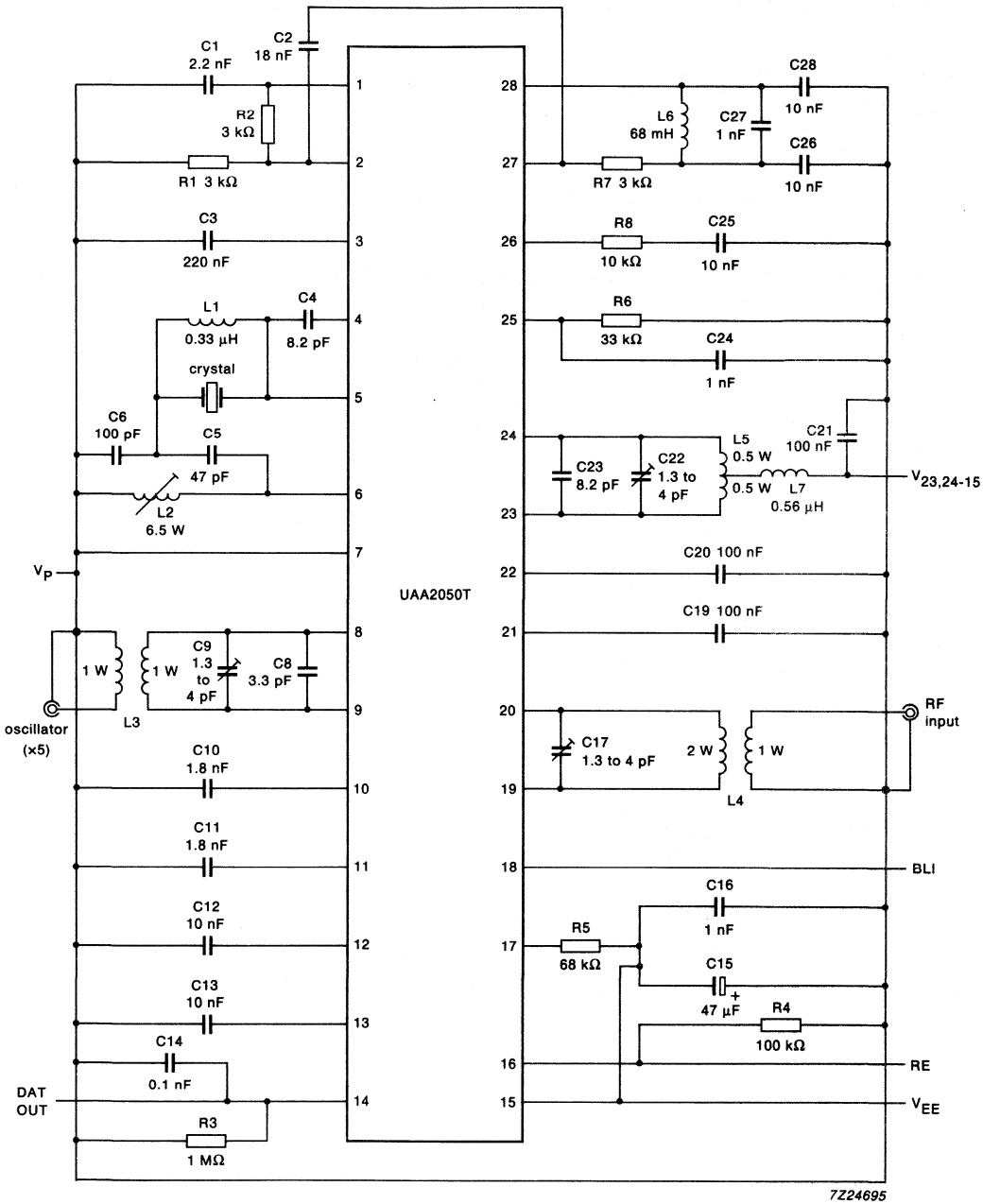


Fig.4 Test circuit (UHF).

Crystal data

Test frequency for the receiver chip is 469.2 MHz, crystal frequency is 93.838 MHz.

Static capacitance C0 (max.) = 4 pF
Dynamic capacitance C1 = 0.4 fF ±20%
Dynamic resistance R1 (max.) = 75 Ω
Temperature drift = $\pm 5 \times 10^{-6}$.

Inductors

L3, L4 and L5: wound with 0.9 mm silvered wire, without pot or core and diameter of 4.5 mm.

L1 = 0.33 μH chip inductor (at 25 MHz minimum value of Q = 12)
L2 = 6.5 turns
L3 = 1 turn
L4 = 2 turns
L5 = 1 turn
L6 = inductor, Philips microchoke (at 10 kHz minimum value of Q = 10)

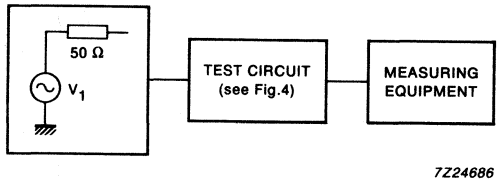


Fig.5 Test figure A.

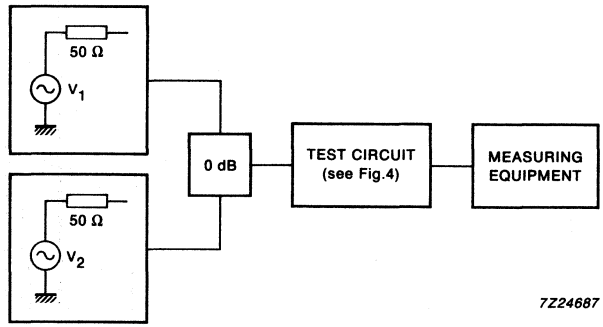
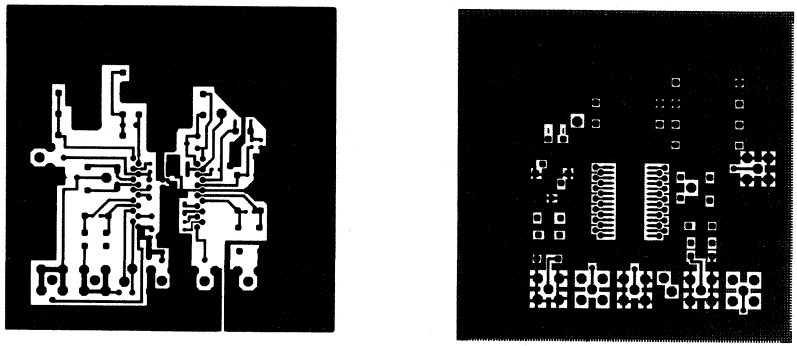


Fig.6 Test figure B.



(a) underside

(b) top side

7Z24689

Fig. 7 Printed-circuit board for UHF range (see Fig.4).

DEVELOPMENT DATA

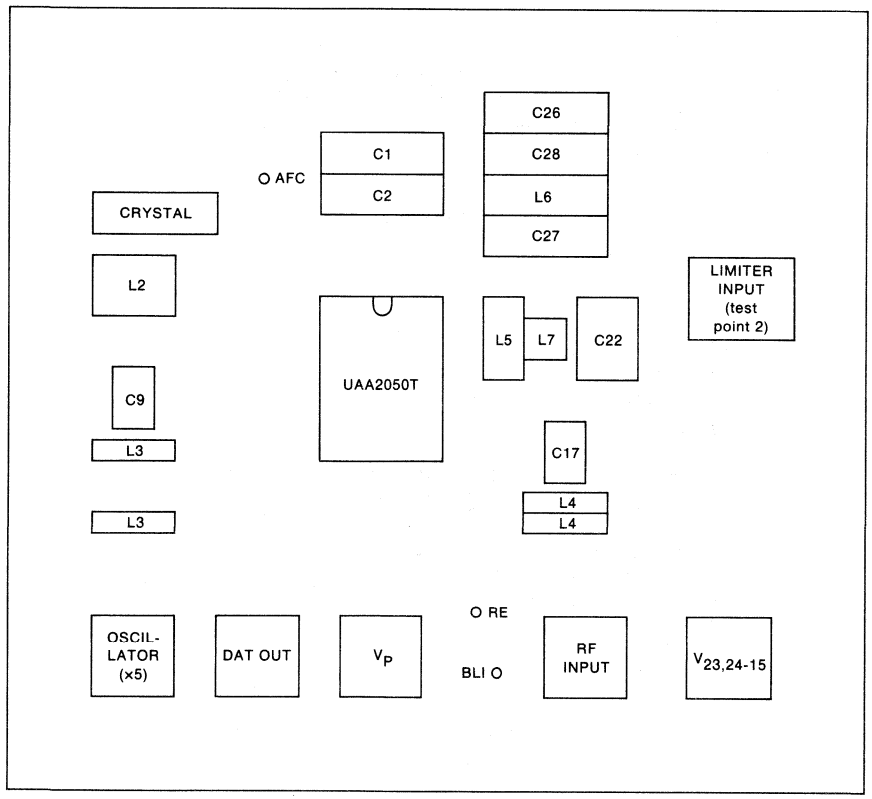


Fig. 8 Printed-circuit board for UHF range (component arrangement).

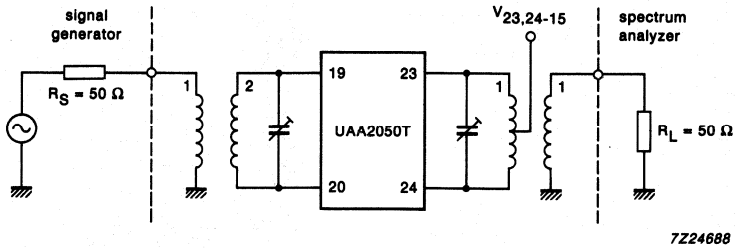


Fig.9 Test circuit for the preamplifier.

DEVELOPMENT DATA

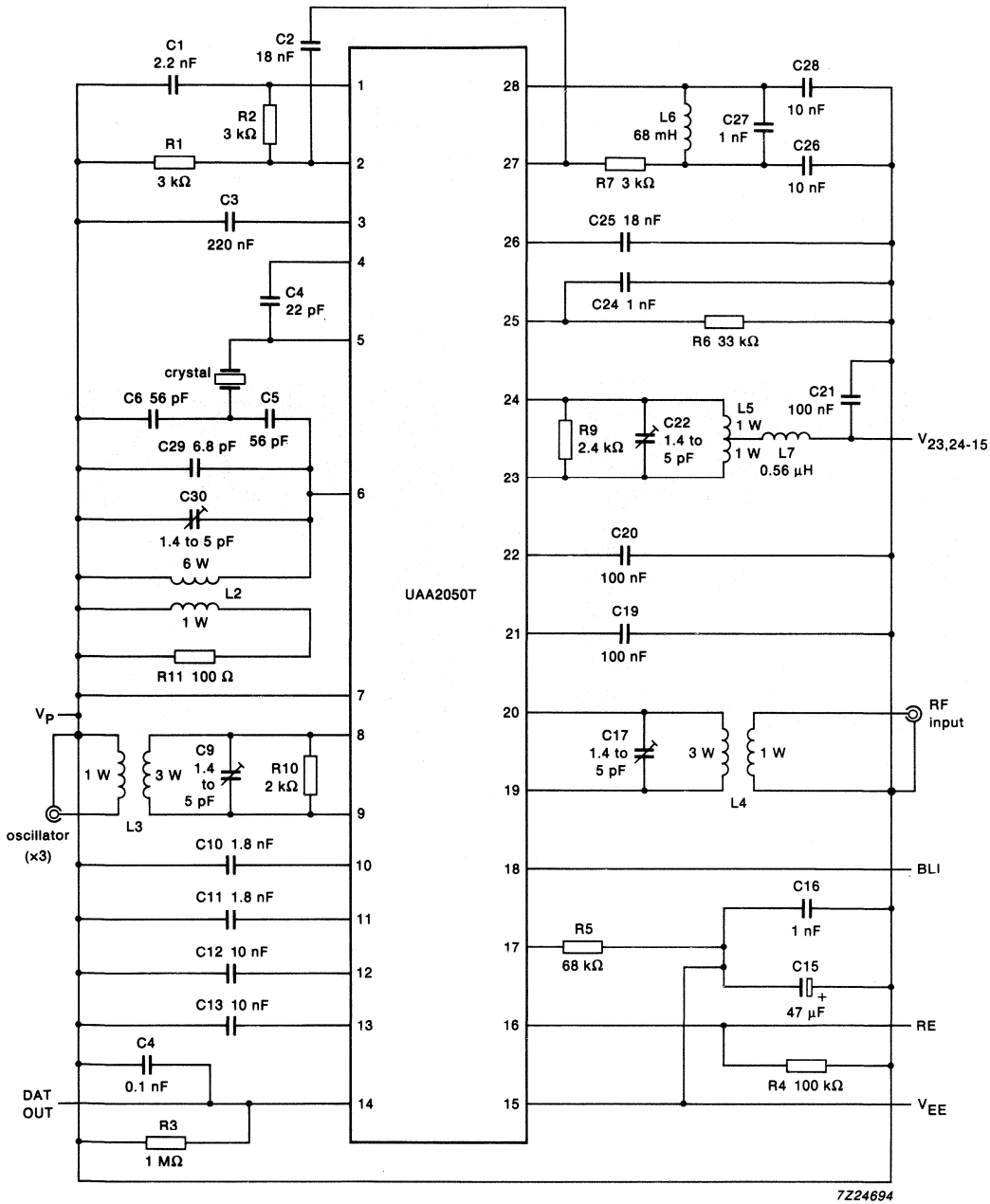


Fig.10 Test circuit (VHF).

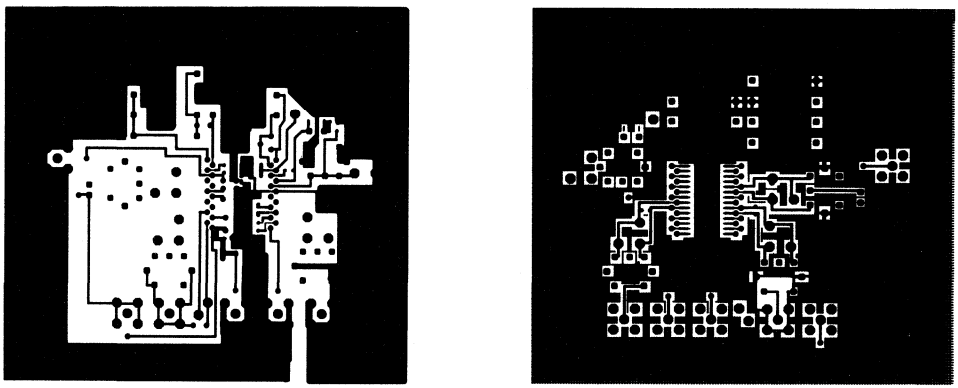
Crystal data

Test frequency for the receiver chip is 173.95 MHz, crystal frequency is 57.9859 MHz.

Inductors

L2, L3, L4 and L5: wound with 0.3 mm enamelled copper wire on Toko 4.5 mm diameter former, without pot or core. Screening cans are also used.

L2 = 6 turns, 2 turns per groove; link winding, 1 turn over the centre of the other winding
L3 = 3 turns, 1 turns per groove; link winding, 1 turn at the bottom of the former
L4 = 3 turns, 1 turns per groove; link winding, 1 turn at the centre of the other winding
L5 = 2 turns
L6 = inductor, Philips microchoke (at 10 kHz minimum value of Q = 10)



(a) underside

(b) top side

7Z24691

Fig. 11 Printed-circuit board for VHF range (see Fig.10).

DEVELOPMENT DATA

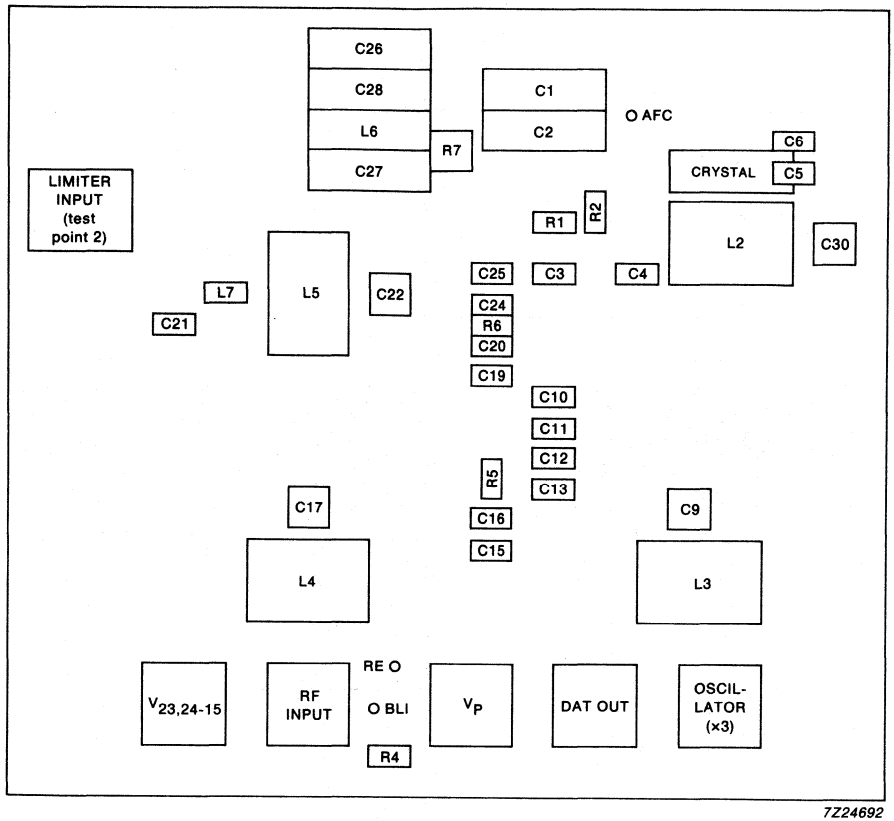


Fig. 12 Printed-circuit board for VHF range (component arrangement).

APPLICATION INFORMATION

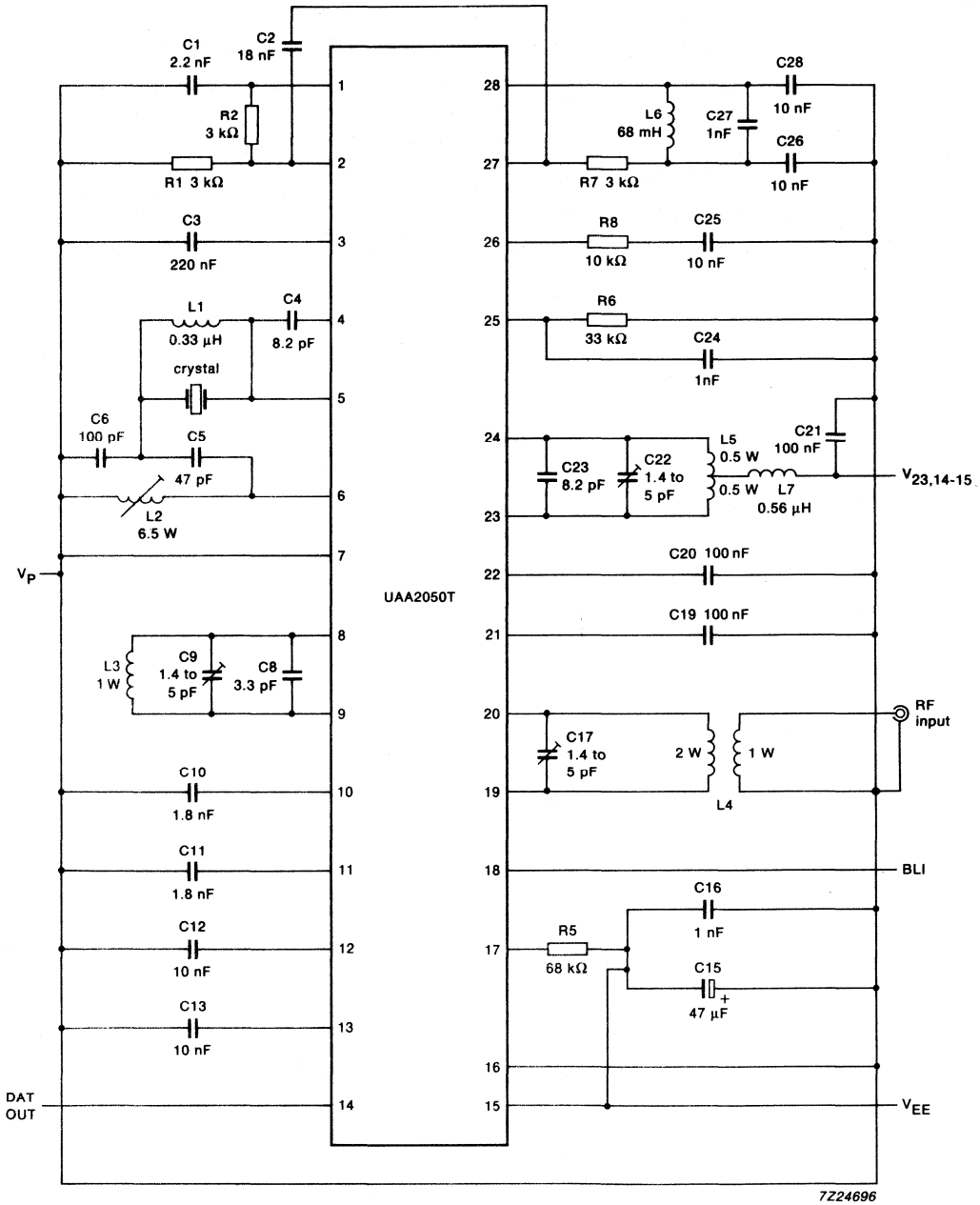


Fig.13 Application diagram (UHF).

Note to Fig.13

For information concerning the crystal oscillator and inductors, refer to Fig.4.

DATA PROCESSOR FOR CELLULAR RADIO (DPROC)

GENERAL DESCRIPTION

The UMA1000T is a low power CMOS LSI device incorporating the data transceiving, data processing, and SAT functions (including on-chip filtering) for an AMPS or TACS hand-held portable cellular radio telephone.

Features

- Single chip solution to all the data handling and supervisory functions
- Configurable to both AMPS and TACS
- I^2C serial bus control
- All analog interface and filtering functions fully implemented on chip
- Error handling in hardware reduces software requirements
- Robust SAT decoding and transponding circuitry
- Low current consumption
- Small physical size
- Minimum external peripheral components required

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 28)	V_{DD}	4.5	5.0	5.5	V
Supply current (pin 28) normal operation	I_{DD}	–	2	–	mA
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

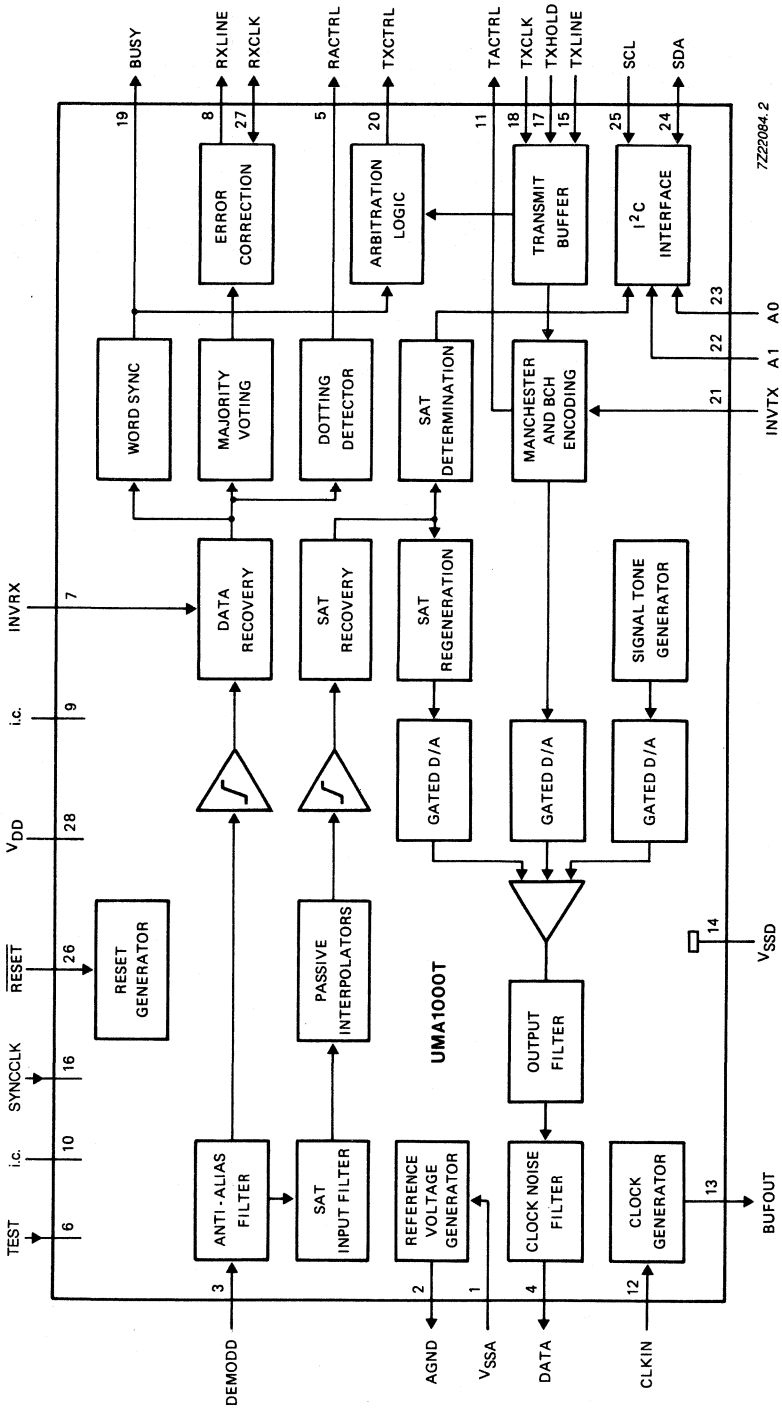


Fig. 1 Block diagram.

DEVELOPMENT DATA

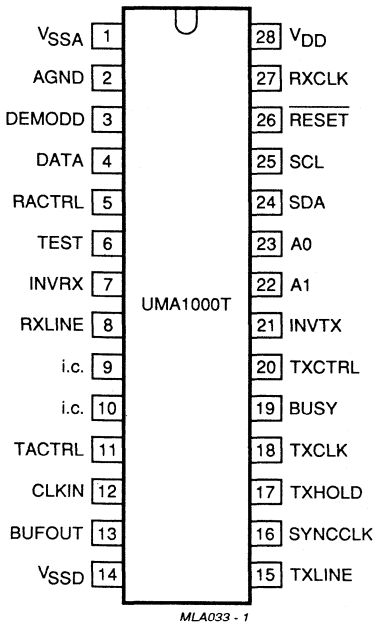


Fig.2 Pinning diagram.

PINNING

1	V_{SSA}	analog negative supply (0 V)	
2	AGND	$(V_{DD} - V_{SSA})/2$ analog reference ground	
3	DEMODD	received data signal input	
4	DATA	transmitted data signal output	
5	RACTRL	received audio control output	
6	TEST	SCAN Control input - used for power on reset	
7	INVRX	inverts sense of received data stream	
8	RXLINE	received data signal output	
9	i.c.	internally connected; must be left open -circuit	
10	i.c.		
11	TACTRL	transmitter audio control output	
12	CLKIN	1.2 MHz external master clock input	
13	BUFOUT	buffered output of internal clock oscillator	
14	V_{SSD}	digital ground	
15	TXLINE	transmitted data signal	
16	SYNCCLK	SCAN CLOCK Control input - used for power-on reset	
17	TXHOLD	holds off transmission of data	
18	TXCLK	transmitted data clock input	
19	BUSY	reverse control channel status output	
20	TXCTRL	transmitter control output	
21	INVTX	inverts sense of transmitted data stream	
22	A1	address input 1 - used for power-on reset	I^2C-bus
23	A0	address input 0	
24	SDA	serial data input/output	
25	SCL	serial clock input	
26	$\overline{RESET}$	master rest input	
27	RXCLK	received data clock input	
28	V_{DD}	positive supply voltage (+ 5 V)	

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	4.5	5.0	5.5	V
Supply current	normal operation	I_{DD}	–	2.0	–	mA
Digital inputs	note 1					
Input voltage LOW		V_{IL}	0	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD} + 0.3	V
Input capacitance		C_I	–	–	6	pF
Digital outputs	note 1					
Output voltage LOW	I_{sink} = 1 mA	V_{OL}	–	–	0.4	V
Output voltage HIGH	I_{source} = 1 mA	V_{OH}	V_{DD} − 0.4	–	–	V
Open-drain outputs	note 2					
Output voltage LOW	I_{sink} = 2 mA	V_{OL}	–	–	0.4	V
Open-drain SDA						
Output voltage LOW	I_{sink} = 3 mA	V_{OL}	–	–	0.4	V

Notes to the characteristics

1. All digital inputs and outputs of DPROC are compatible with standard CMOS devices and the following general characteristics apply.
2. Open-drain outputs have no internal pull-up resistors.

FUNCTIONAL DESCRIPTION

General

The UMA1000T (DPROC) is a single chip CMOS device which handles the data and supervisory functions of an AMPS or TACS subscriber set.
These functions are:

- Data reception and transmission
- Control and voice channel exchanges
- Error detection, correction, decoding and encoding
- Supervisory Audio Tone decoding and transponding
- Signalling Tone generation

In an AMPS or TACS cellular telephone system, mobile stations communicate with a base over full duplex RF channels. A call is initially set up using one out of a number of dedicated control channels. This establishes a duplex voice connection using a pair of voice channels. Any further transmission of control data occurs on these voice channels by briefly blanking the audio and simultaneously transmitting the data. The data burst is brief and barely noticable by the user. A data rate of 10 kbit/s is used in the AMPS system and 8 kbits/s in TACS. The signalling formats for both Forward Channels (base to mobile) and Reverse Channels (mobile to base) are shown in Fig. 3.

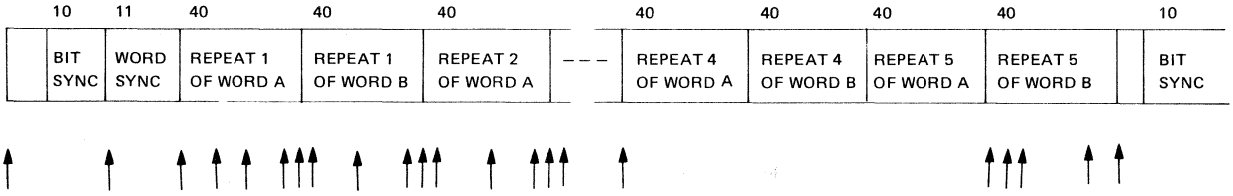
A function known as Supervisory Audio Tone (SAT), a set of 3 audio tones (5970, 6000 and 6030 Hz), is used to indicate the presence of the mobile on the designated voice channel. This signal, which is analagous to the On-Hook signal on land lines, is sent out to the mobile by the base station on the Forward Voice Channel. The signal must be accurately recovered and transponded back to the base station to complete the 'loop'. At the base station this signal is used to ascertain the overall quality of the communication link.

Another voice channel associated signal is Signalling Tone (ST). This tone (8 kHz TACS, 10 kHz AMPS) is generated by the mobile and is sent in conjunction with SAT on the Reverse Voice Channel to serve as an acknowledgement signal to a number of system orders.

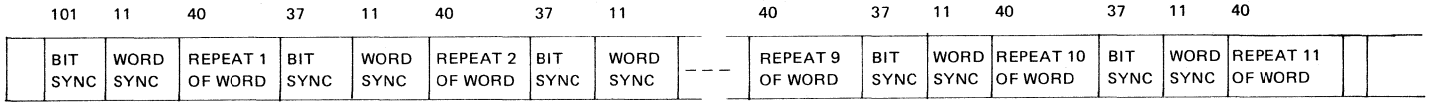
The key requirements of a hand held portable cellular set are:

- small physical size
- minimum number of interconnections (serial bus)
- low power consumption
- low cost

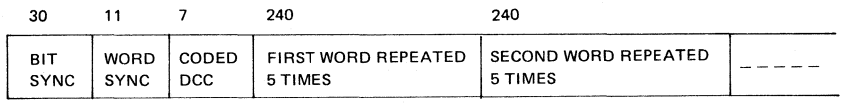
The DPROC is a member of our Cellular Radio chipset, based on the I^2C-bus, which meets these requirements. A cellular radio system schematic using the chip set is shown in Fig. 4.



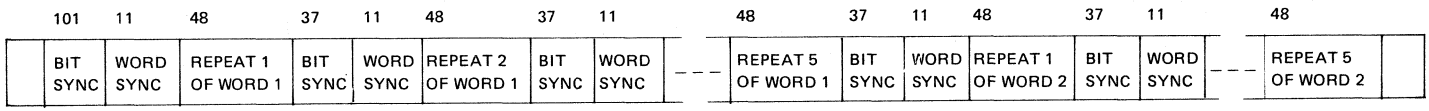
(a) forward control channel



(b) forward voice channel



(c) reverse control channel



(d) reverse voice channel

Fig. 3 Signalling formats.

DEVELOPMENT DATA

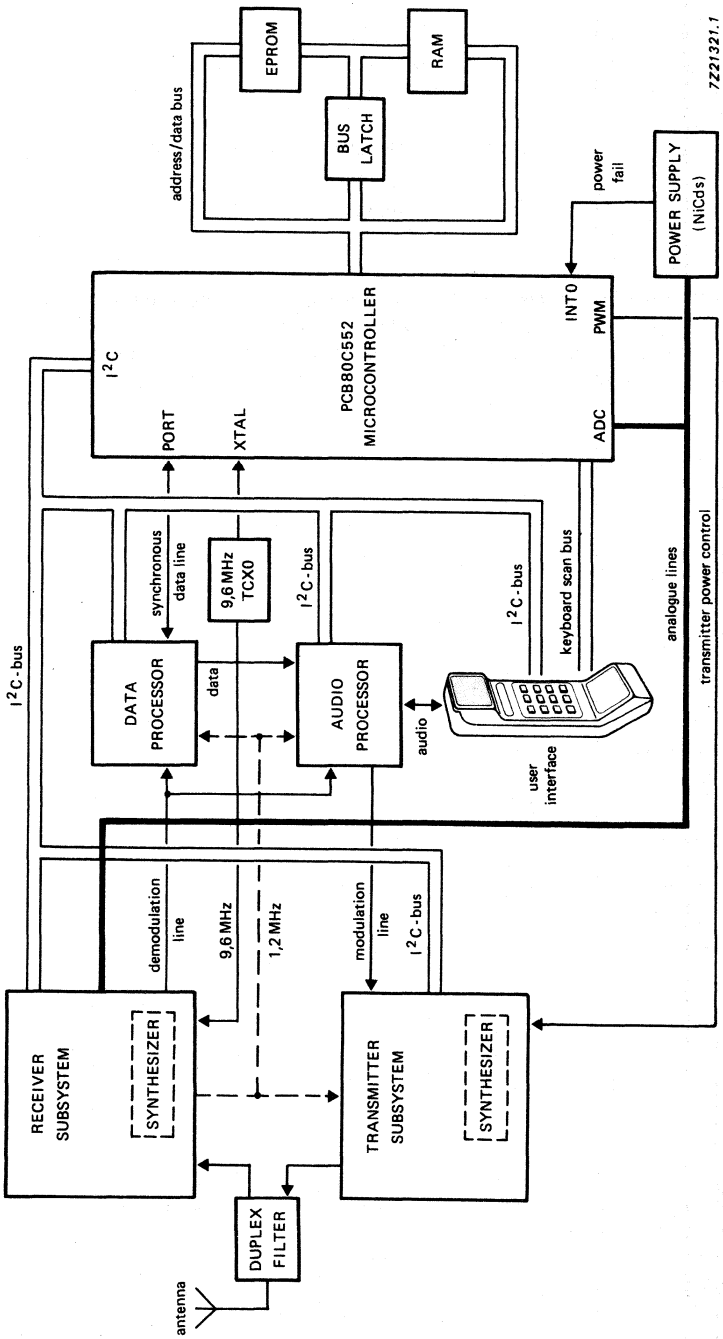


Fig. 4 Cellular radio system schematic.

EXTERNAL PIN DESCRIPTION

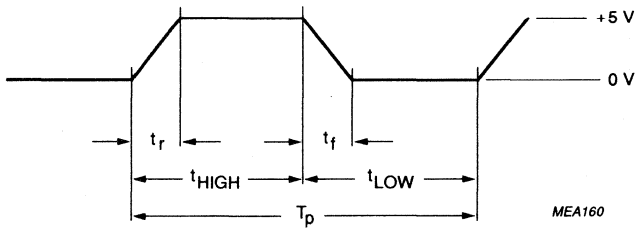
Supply (V_{DD}; V_{SSA}; V_{SSD}; AGND)

V_{DD} : Positive supply voltage for digital and analog circuitry (± 5 V +10%)
V_{SSA} : Negative supply voltage for analog circuitry (0 V)
V_{SSD} : Digital ground (0 V)
AGND: Internally generated reference ground used by internal analog circuitry. Voltage level $(V_{DD} - V_{SSA})/2$ ± 2%.

Both V_{SSA} and V_{SSD} must be connected to common ground.

System clock (CLKIN; BUFOUT)

CLKIN is a digital input for the externally generated 1.2 MHz master clock. This signal should be accurate to 100 x 10^{-6} and have a worst case of 60 : 40 mark-space ratio. BUFOUT is the buffered output of the clock oscillator and provides the option of generating the clock signal on chip by connecting a 1.2 MHz crystal between BUFOUT and CLKIN.



parameter	symbol	min.	typ.	max.	unit
Clock period time	T_p	833.25	833.33	833.42	ns
HIGH time	t_{HIGH}	40%	50%	60%	T_p
LOW time	t_{LOW}	–	T_p-t_{HIGH}	–	
Rise time	t_r	–	50	–	ns
Fall time	t_f	–	50	–	ns

I^2C serial data link (SDA; SCL)

SDA is the bi-directional data line; SCL the clock input from an I^2C master. These constitute a typical I^2C link and conform to standard characteristics as defined in the I^2C-bus specification.

- data rate: up to 100 kbit/s

Slave Address Select (A0; A1)

Selection of the device slave address is achieved by connecting A0 to either V_{SSD} or V_{DD} and connecting A1 to either pin 16 and pin 6 or to V_{DD}. The slave address is defined in accordance with the I^2C specifications as shown in Fig. 5.

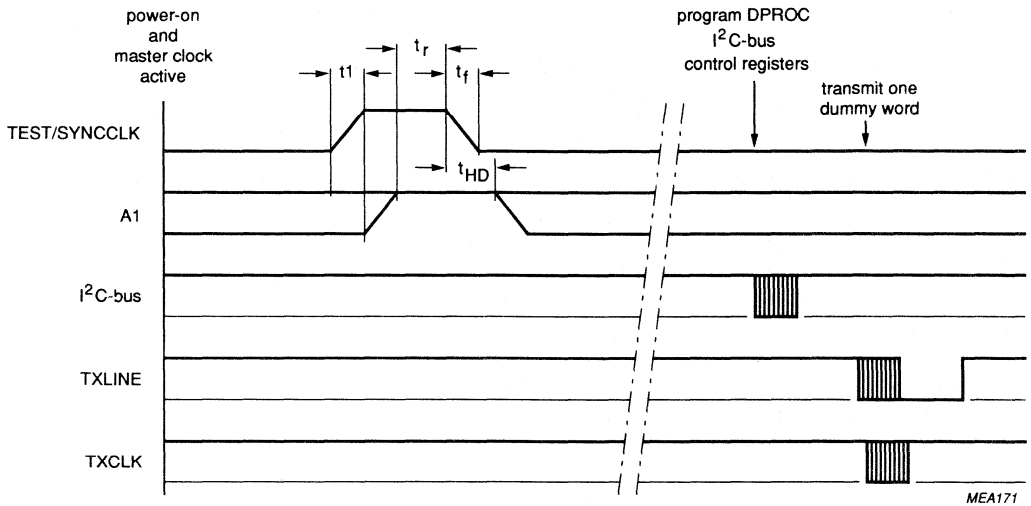
1	1	0	1	1	A1	A0	R/$\overline{W}$

Fig. 5 Device slave address.

Power-up state

DPROC will not respond reliably to any inputs (including $\overline{\text{RESET}}$) until 100 μs after the power supply has settled within the specified tolerance. The analog sections of the device will have stabilized within 5 ms. No power-on-reset is provided, therefore before the device can enter normal operation TEST and SYNCCLK must be pulsed HIGH. The reset pulse on these pins must have a minimum period of 250 μs and the fall time of the negative going edge must be faster than 1 μs. Pin A1 must remain HIGH during this reset period therefore if the A1 bit of the I^2C address is required to be logic 0. A1 may be connected to TEST and SYNCCLK. If it is required to be at logic 1 then A1 may be permanently connected to V_{DD}. If it is required that A0 = logic 1, then a normal master reset (pin 26) sequence must follow the power-on-reset sequence to get the internal registers in the defined state.

After the power-on-reset a dummy transmission should be made to initiate internal DPROC counters. This transmission should be made with arbitration (ABREN) disabled and the RF transmitter stage switched OFF. Figure 6 shows the power-on reset sequence.



Where:

t1 = time not critical.
t_r = reset time = 250 μs max.
t_f = pulse fall time = 1 μs max.
t_{HD} = AI hold time = 0 μs min.

Note

The RF transmitter is OFF during reset sequence.

Fig.6 Power-on reset programming sequence.

Master reset ($\overline{\text{RESET}}$)

$\overline{\text{RESET}}$ is an asynchronous active LOW master reset input, with a minimum active pulse width of 2 μs which may be used to reset certain logic within DPROC to a predefined state as illustrated in Tables 1 and 2. Alternatively, DPROC may be set into a known initial state be setting the I^2C control register as required. The internal reset sequence after a negative pulse on $\overline{\text{RESET}}$ takes 250 μs.

EXTERNAL PIN DESCRIPTION (continued)

Table 1 Predefined state of the digital output pins

output	state
RXLINE	HIGH
TXCTRL	HIGH
TACTRL	HIGH
RACTRL	HIGH
BUSY	HIGH

Table 2 Predefined state of the I^2C registers

register	bit							
	7	6	5	4	3	2	1	0
control	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
SATD	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
TST	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

Data Transfer Link (RXLINE; TXLINE; TXHOLD; TXCLK and RXCLK)

RXLINE, TXLINE, TXCLK and RXCLK provide a dedicated serial data link for the transfer of system data messages between DPROC and the system controller at variable rates of up to 200 kbits/s. TXHOLD allows the system controller to preload the DPROC transmit register with one word without the data being transmitted. DPROC then starts transmitting the instant TXHOLD is driven LOW.

- RXCLK : clock input from system controller
- RXLINE : data output from DPROC to system controller
- TXCLK : clock input from system controller
- TXLINE : open drain data bi-directional line to the system controller
- TXHOLD : (HIGH) holds off transmission of data
- data rate : up to 200 kbit/s

Note

A minimum mean data transfer rate for the received data of 2.1 kbits/s (AMPS) and 1.7 kbits/s (TACS) is required to ensure contiguity of message words.

The format for received and transmitted data words is shown in Fig. 14 (a) and Fig. 14 (b) respectively. The receive and transmit data timing is illustrated in Fig. 15 (a) and Fig. 15 (b) respectively.

Transmitter Control (TXCTRL)

TXCTRL is an open-drain output used to disable the transmitter during a Reverse Control Channel access failure.

- output level HIGH : RF enable
- output level LOW : RF disable

Transmitter Audio Enable (TACTRL)

TACTRL is an open-drain digital output signal used to blank the audio path and enable the data path to the modulator during data bursts on the Reverse Voice Channel.

- output level HIGH : audio enabled
- output level LOW : audio muted

Receiver Audio Enable (RACTRL)

RACTRL is an open-drain digital output used to blank the audio path to the earpiece when a sequence of dotting and word sync is detected.

RACTRL and TACTRL functions can be combined using one line.

- output level HIGH : audio enabled
- output level LOW : audio muted

Reverse Control Channel Status (BUSY)

BUSY is a digital output giving the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy-Idle bits and has the following logic levels:

- output level HIGH : channel busy
- output level LOW : channel idle

On a voice channel BUSY indicates channel idle.

Invert Receive Data (INVRX)

Enables an additional inverter in the receive data path. This allows RF demodulators with high or low local oscillators to be used. The TACS and AMPS specifications define a NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the demodulated data stream into DPROC depends on the receiver local oscillator.

- input HIGH : data inverted
- input LOW : data normal

Invert Transmit Data (INVTX)

Enables an additional inverter in the transmit data path. This allows RF modulators with high or low local oscillators to be used. The TACS and AMPS specifications define a NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the modulated data stream depends on the transmitter local oscillator.

- input HIGH : data inverted
- input LOW : data normal

Transmitted Data Output (DATA)

Data is an analog output which provides Manchester encoded and filtered data signal SAT and signalling tone. This signal should normally be AC coupled into the Audio/Data summer.

- DC level : analog ground (AGND)
- signal level : 2 V (p-p) * for signalling tone
- signal tolerance : 2% + supply voltage variation (ΔV_{DD})
- minimum load impedance : 10 kΩ
- maximum load capacitance : 2 nF
- maximum output impedance : 50 Ω

Received Data Input (DEMODD)

Demodd inputs analog data and SAT signals from the RF demodulator. This pin should normally be AC coupled (characteristics for UMA1000T/F4 upwards).

- DC level : analog ground (AGND)
- maximum data level : 1 V (p-p)
- nominal data level : 250 mV (p-p)
- minimum data level : 200 mV (p-p)
- minimum SAT level : 50 mV (p-p)
- input impedance : > 1 MΩ

* Signal level with filtered data signal.

DEVELOPMENT DATA

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

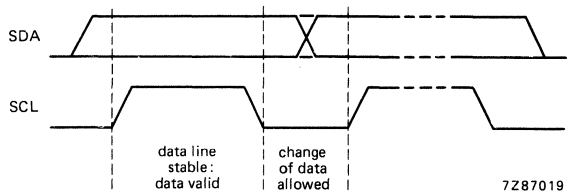


Fig. 7 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

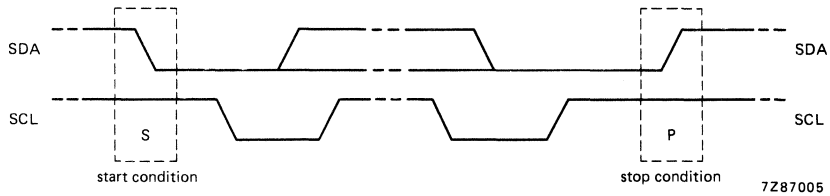


Fig. 8 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

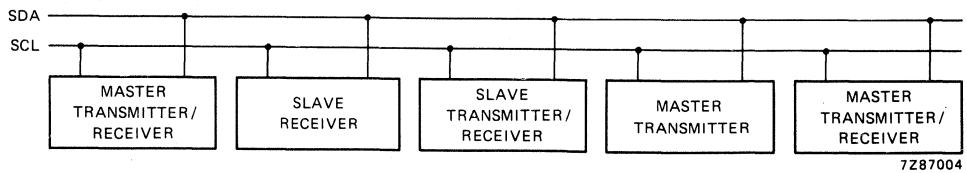


Fig. 9 System configuration.

CHARACTERISTICS OF THE I²C BUS (continued)

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

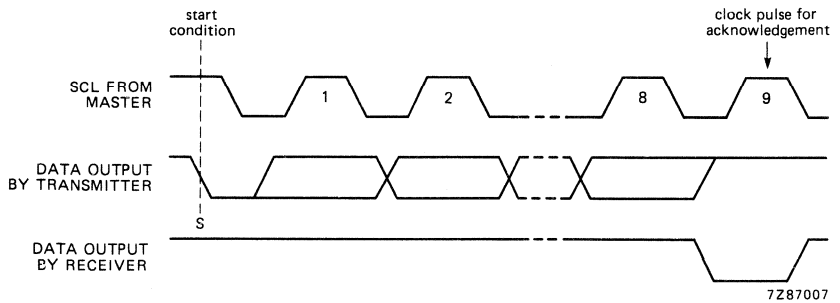


Fig. 10 Acknowledgement on the I²C bus.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 11.

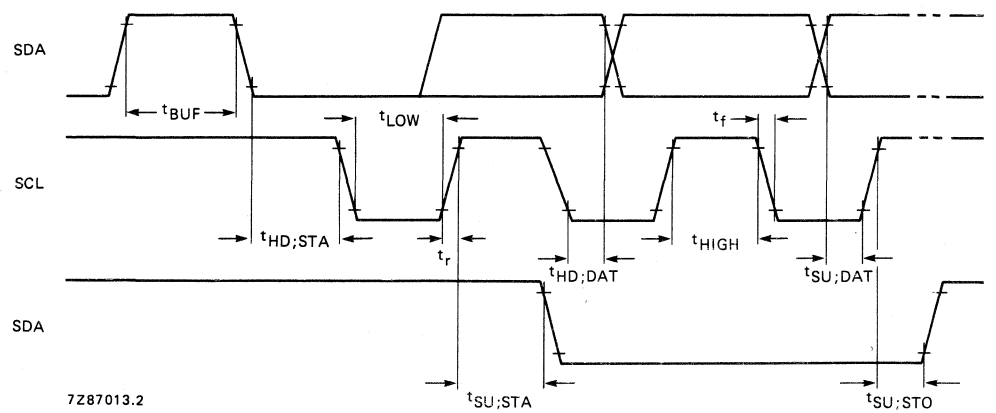


Fig. 11 Timing.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4.7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS}.

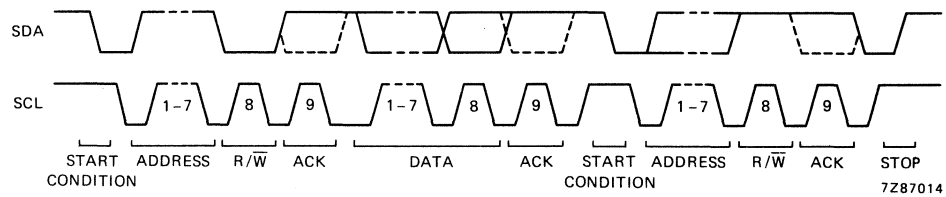


Fig. 12 Complete data transfer.

Where:

Clock t_{LOWmin}	4.7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Max. number of bytes	Unrestricted
Premature termination of transfer	Allowed by generation of STOP condition
Acknowledge clock bit	Must be provided by the master

I²C REGISTERS

General

The I²C register block resides internally within the I²C interface block and contains various items of status and control information which are transferred to and from DPROC via the I²C-bus. The block is organized into four 8-bit registers:

- Status Register — contains read only items
- Control Register
- SAT Programmable Phase Shift Register — contain write only items
- TEST Register

Note

In normal operation the SAT delay register and the TEST register require programming only after a device reset.

Table 3 Register map

register	bit 7	6	5	4	3	2	1	0
status	–	–	WSYNC	BUSY	TXABRT	TXIP	MSCC1	MSCC0
control	–	SERV	STS	TXRST	ABREN	FVC	STEN	SATEN
SATD	<---------- SAT delay data ---------->							

S	DPROC ADR	R	A	STATUS	A	P

(a) read from DPROC status register

S	DPROC ADR	W	A	CONTROL	A	P

(b) write to DPROC control register

S	DPROC ADR	W	A	CONTROL	A	SAT DELAY	A	TEST	A	P

(c) write to all DPROC registers

Where:

S	: START condition
W	: read/write bit (logic 0 = write)
R	: read/write bit (logic 1 = read)
A	: acknowledge bit
P	: STOP condition
DPROC ADR	: slave address of DPROC
TEST	: must be programmed to logic 0 for normal operation

Fig. 13 I²C data format.

Status Register

This is a read only register containing DPROC status information.

Measured SAT Colour Code (MSCC1; MSCC0)

MSCC1 and MSCC0 provide information about the current measured SAT colour code in accordance with Table 4.

Table 4 Measured SAT Colour Code

MSCC1	MSCC0	SAT frequency (Hz)
0	0	5970
0	1	6000
1	0	6030
1	1	no valid SAT

Transmission In Progress (TXIP)

TXIP indicates whether DPROC is currently accessing the Reverse Control or Voice Channels.

- logic 1 : data transmission in progress
- logic 0 : transmission not in progress

Transmission Abort Status (TXABRT)

TXABRT indicates that a Reverse Control Channel Access Attempt has been aborted by DPROC without successful message transmission.

- logic 1 : transmission attempt aborted
- logic 0 : no access collision detected

Reverse Control Channel Status (BUSY)

BUSY gives the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy-Idle bits on the Forward Control Channel.

- logic 1 : channel busy
- logic 0 : channel idle

On a voice channel the BUSY bit defaults to the set state.

Note

This signal is also routed to the BUSY output pin.

Word Synchronization Indicator (WSYNC)

WSYNC indicates whether DPROC has acquired frame synchronization according to the Forward Control Channel format.

- logic 1 : frame synchronization acquired
- logic 0 : no frame synchronization

I²C REGISTERS (continued)

Control Register

This is a write only register containing DPROC control information.

SAT Path Enable (SATEN)

SATEN enables the SAT transponded signal to be output on external pin DATA.

- logic 1 : SAT tone enabled
- logic 0 : SAT tone inhibited

Signalling Tone (ST) Path Enable (STEN)

STEN enables the Signalling Tone to be output on external pin Data.

- logic 1 : ST enabled
- logic 0 : ST inhibited

Channel Format Select (FVC)

FVC selects the required channel format.

- logic 1 : Voice channel format
- logic 0 : Control channel format

Transmission Abort Permission (ABREN)

ABREN indicates whether DPROC has permission to abort data transmission and disable RF on the Reverse Control Channel following the detection of a channel access attempt collision.

- logic 1 : RF disable allowed
- logic 0 : RF disable inhibited

Message Transmission Abort (TXRST)

TXRST terminates a message being transmitted on the reverse channel. It is a monostable signal which when activated causes a reset of the message transmission circuitry and causes TXABRT and TXIP I²C signals to be reset.

This signal does not clear the DPROC transmit register; therefore if a word has been loaded into DPROC after a TXABRT has occured the control line TXHOLD should be held LOW to allow the word to be cleared from the DPROC input register.

- logic 1 : reset active
- logic 0 : reset inactive

System Type Select (STS)

STS selects required system format.

- logic 1 : AMPS
- logic 0 : TACS

Note

Toggling this signal also resets the receive logic in DPROC.

Serving System Select (SERV)

SERV selects which of the serving system data streams (A or B) is accepted.

- logic 1 : system A selected
- logic 0 : system B selected

DEVELOPMENT DATA

SAT Programmable Delay Register (SATD)

SATD programs the value of phase shift which is applied to the SAT tones in the SAT Regeneration Block. This value will be determined and programmed into the System Controller during manufacture. The recovered SAT is delayed in time by approximately 0.8 μs x value in the register which corresponds to approximately 1,8 degrees x value in the register. The total phase shift is limited to 360 degrees.

The ability to adjust SAT phase angle is not necessary in current AMPS and TACS systems. Therefore this register should normally be in AMPS and TACS, this function is not necessary and should programmed to zero.

DIGITAL CIRCUIT BLOCKS

General

The majority of the digital circuitry within the DPROC device is identical for both AMPS and TACS. The device has little additional redundancy to implement both systems. The functions of these blocks are described in the following sections and relate to those shown in Fig. 1.

Data Recovery

The Data Recovery Block receives wideband Manchester encoded data in sampled and sliced form from the Strobed Comparator Block, on which it performs the following functions:

- clock recovery
- Manchester decoding
- data regeneration

The Clock Recovery Block extracts an 8 or 10 kHz (TACS or AMPS) phase locked clock signal from the Manchester encoded data stream. This is implemented using a digital-phase-locked-loop (PLL) which has an adjustable "bandwidth" to provide both fast acquisition and low jitter.

Manchester decoding is performed by exclusive ORing the recovered Manchester encoded data with the recovered clock.

The NRZ data regeneration is performed by a digital integrate and dump circuit. This consists of an up/down counter that counts 1.2 MHz cycles during the data period. The sense of the count is determined by the result of the Manchester Decoder output. The number of counts is sampled at the end of a data period. If this number exceeds a threshold the data is latched as a 1 otherwise it is latched as a 0.

SAT Processing

The Supervisory Audio Tone processing consists of the following functions:

- SAT recovery
- SAT determination
- SAT regeneration

SAT recovery

The SAT Recovery Block receives a filtered and sliced SAT signal which must be recovered before being routed to the Determination and Regeneration Blocks.
The recovery is performed using a digital phase-locked-loop.

SAT determination

The SAT Determination Block indicates which, if any, of the valid SAT tones is detected from the recovered SAT. The AMPS and TACS specifications require that a determination is made at least every 250 ms. Determination involves counting the number of cycles of the regenerated SAT in this time period. This count is then compared to a set of four known counts which define the boundaries between the SAT frequencies and the SAT not valid events. The result is then coded into the I^2C status registers MSCC0 and MSCC1 as shown in Table 5.

DIGITAL CIRCUIT BLOCKS (continued)

Table 5 Status registers MSCC0, MSCC1; decoded SAT frequencies

register		SAT frequency band (Hz ± 4 Hz)	decoded SAT (Hz)
MSCC0	MSCC1		
1	1	< 5956	not valid
0	0	5956 to 5986	5970
0	1	5986 to 6014	6000
1	0	6014 to 6046	6030
1	1	> 6046	not valid

SAT regeneration

The SAT Regeneration Block generates a digital SAT stream from the recovered SAT stream for transponding back to the base station. The AMPS and TACS specifications require the SAT to be transponded with a maximum phase shift of 20 degrees between the point the modulated RF signal enters the mobile from the base station, and the point the modulated RF leaves the mobile. A variable phase compensation circuit is provided in DPROC to shift the recovered SAT through 0 to 360 degrees before being passed to the output summing network. The degree of phase shift is determined during manufacture of the set and the required additional phase shift is stored in non-volatile RAM and programmed via I^2C at each power-on cycle. The phase correction is performed by a counter delay method using signals which are phase locked to the recovered SAT.

Dotting Detector

The Dotting Detector Block determines whether a data inversion (dotting) pattern has been received on the Forward Voice Channel. The detection of 32 bits of data inversion indicates that the Clock Recovery Block has acquired bit synchronization and that the narrow bandwidth mode on the clock recovery phase-locked-loop is selected. This signal is also used to indicate that a data burst is expected and activates the audio mute RACTRL, after a Word Synchronization Block has been received, for the duration of the burst.

Word Synchronization Detector

The Word Synchronization Block performs the following functions:

- Frame synchronization
- Reverse Control Channel status (B/I determination)
- Valid Serving System determination

These functions are associated solely with the Forward Control Channel and have no meaning on the Forward Voice Channel.

Information in a data stream is identified by its position with respect to a unique synchronization word. This synchronization word is an 11 bit-Barker code which has a low probability of simulation in an error environment, and can be easily detected. Data received is only considered valid at times when DPROC has achieved frame synchronization. In this condition the block leaves its search mode and enters its lock mode. This is indicated by bit WSYNC being set HIGH. In order to achieve this two consecutive synchronization words separated by 463 bits must be detected. Once in lock mode, the synchronization word detector is examined every 463 bits and only loses frame synchronization after 5 consecutive unsuccessful attempts at detecting the synchronization word have been made. At this point bit WSYNC is cleared and the device is returned to its search mode. On the Forward Voice Channel detection of the synchronization word indicates that the following 40 bits are valid data. Information detailing the status of the Reverse Control Channel is given by the Busy/Idle bits. These occur at intervals of 11 bits within the frame, the first occurring immediately following the synchronization word. The status of the channel is determined by a majority decision on the last three consecutive Busy/Idle bits.

Majority Voting Block

The Majority Voting Block performs the following functions:

- identifying position and validity of frames in the received data stream
- extracting 5 repeats of each word from a valid frame
- performing a bit-wise majority decision on the five repeats of the data word

The validity of the frames is determined by setting a counter in operation which times out and resets the circuitry after 920 or 463 bit periods from detecting valid word synchronization. The time out period selected depends on whether DPROC is monitoring the Forward Voice or Control Channel respectively.

Up to five repeats of the message word are searched for and extracted by DPROC. On the forward Voice Channel DPROC will extract the first five words that occur for which a correct synchronization word is found. These words can occur in any position in the frame. A serial majority vote is performed as the fifth word is being extracted.

Error Correction Block

The Error Correction Block performs the following functions:

- extraction of a valid message from the Majority-Voted Word
- computation of the S1 and S3 syndromes
- correction of up to one error in the word
- communication of received data to the System Controller via the Received Data Serial Link.

Interpretation of parity of a received word is obtained from knowledge of the syndromes of the word. The syndromes are calculated using feedback shift registers with two characteristic equations:

$$1 + X + X^6 \text{ and } 1 + X + X^2 + X^4 + X^6$$

Once the syndromes of a received word are known, it is possible to determine if a correctable error is present. DPROC only corrects up to one error although the code used has a Hamming distance of five. The occurence of two or more errors is signalled by setting the BCH error flag, which is communicated to the System Controller via the Received Data Serial Link.

DIGITAL CIRCUIT BLOCKS (continued)

Received Data Serial Link

The Received Data Serial Link transfers data and control information from DPROC to the System Controller. The data is transferred on RXLINE under control of a clock signal RXCLK, generated by the System Controller. The system controller is informed of the arrival of a decoded data word in the DPROC output register by RXLINE being driven LOW. If the system controller chooses to ignore the received data or only partially clock the data out, the DPROC will reset the receive buffer for the next word after the period RWIN (see Fig. 15).

Data Format

Each Received Data word consists of 4 bytes. The word format is shown in Fig. 14 (a). The sense and function of the fields is shown in Table 6.

Table 6 Received Data word

bit	title	sense	function
31	start	LOW	identifies start of word
30	BCH error	active HIGH	indicates that an uncorrected BCH error is associated with the word
29 to 2	received data	binary data	received data word
1	RXLINE error	LOW	if detected as HIGH indicates that a transmission error has occured on the microprocessor to DPROC serial link
0	stop	HIGH	identifies end of the word

Link Protocol

The Received Data protocol is described by the timing diagram Fig. 15 (a) and has the following parameters:

- maximum receive window (RWIN)
  Control Channel (TACS) = 47 ms
  Control Channel (AMPS) = 37 ms
- minimum clock period ($t_{CLK(min)}$ = 2 μs
- minimum clock hold-off (t_{WAIT}) = 100 μs

Transmit Data Serial Interface

The Transmit Data Serial Link performs reception of data from the System Controller to DPROC over a dedicated line TXLINE. The transfer of data is synchronous with a clock signal TXCLK, generated by the System Controller.

Data Format

Each Transmit Data word consists of 5 bytes. The word format is shown in Fig. 14 (b). The sense and function of the fields is shown in Table 7.

Table 7 Transmit Data word

bit	title	sense	function
39	start	LOW	identifies start of word
38, 37	DCC	binary data	digital colour code
36 to 1	transmit data	binary data	transmit data word
0	stop	HIGH	identifies end of the word

DEVELOPMENT DATA

Link Protocol

Messages are normally up to 5 words in length on the Reverse Control Channel and up to 2 words in length on the Reverse Voice Channel. However, DPROC will transmit messages of any word length. These must be transmitted on the data stream without interruption. To avoid the need for large buffer areas, a flexible protocol is used to allow DPROC to control the transfer of data words. DPROC has an on-chip buffer which can hold one complete word of a message. Whilst new words are being loaded into DPROC, within the time period Buffer clear to end of TWIN, DPROC will maintain uninterrupted data transmission. The System Controller can abort the transmission of a message at any point activating the I^2C signal TXRST. This signal causes the interface to return to its power-up state and resets TXIP and TXABRT (see Table 3). On completion of these tasks TXRST will return to its inactive state. The Transmit Data Protocol is described by the timing diagram shown in Fig. 15(b) and has the following parameters:

- maximum transmit window (TWIN)
  - voice channel (TACS) = 60 ms
  - voice channel (AMPS) = 48 ms
  - control channel (TACS) = 29 ms
  - control channel (AMPS) = 23 ms
- minimum clock period ($t_{CLK(min)}$) = 2 μs

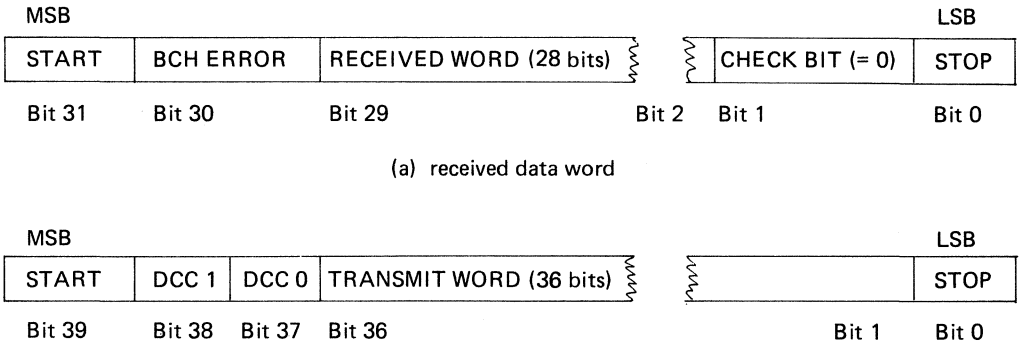
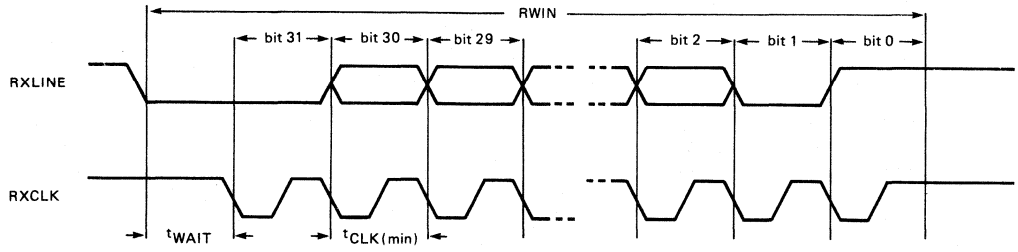
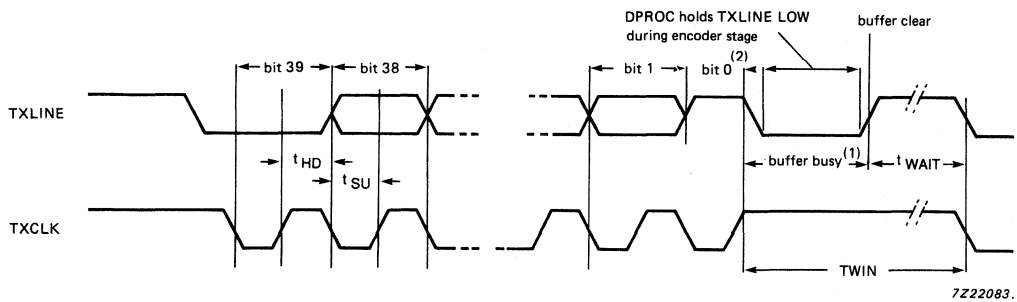


Fig. 14 Data word formats.

DIGITAL CIRCUIT BLOCKS (continued)



(a) DPROC to microcontroller link; receive data timing.



Where:

t_{HD} = 100 ns minimum
t_{SU} = 0 ns minimum
t_{WAIT} = 0 ns minimum

(b) Microcontroller to DPROC link; transmit data timing.

(1) The buffer busy time depends on whether the first or subsequent words are being loaded.

(2) The system controller should monitor the TXLINE during bit 0, if the status of TXLINE does not change from a HIGH to a LOW on the rising edge of TXCLK, then a framing error has occured. This can be caused by glitches on the clock line or if an arbitration error occured while the DPROC transmit register was being loaded. The system controller should recover the situation by holding TXLINE HIGH and supplying clocks on TXCLK until TXLINE goes LOW. Then the situation should be treated as a normal channel arbitration failure as described in **Reverse Control Channel Access Arbitration** – Abort Procedure.

Fig. 15 Data timing diagrams.

DEVELOPMENT DATA

BCH and Manchester Encoding Block

The functions performed by this circuit block include:

- reception of data from the System Controller
- parity generation
- message construction
- Manchester encoding

Each 36-bit Information Word sent on the Reverse Voice and Control Channels is coded into a 48 bit code word. The code word consists of the 36-bit word followed by 12 parity bits. These parity bits are formed by clocking the information word into a 12-bit feedback shift register with characteristic equation:

$$1 + X^3 + X^4 + X^5 + X^8 + X^{10} + X^{12}$$

The BCH Encoder Block constructs the Reverse Voice and Control Channel data streams from the information it receives from the System Controller.
The streams are formed out of the four possible field types:

- Dotting (data inversions)
- 11-bit Synchronization Word
- Digital Colour Code
- 48-bit code word

The 2 bits of DCC received from the System Controller are coded into a 7-bit word as shown in Table 8.

Table 8 Digital Colour Code; 7-bit word

DCC1	DCC0	Coded DCC						
0	0	0	0	0	0	0	0	0
0	1	0	0	1	1	1	1	1
1	0	1	1	0	0	0	1	1
1	1	1	1	1	1	1	0	0
		DCC1		DCC0			DCC1.EXOR.DCC0	

The data sense for Manchester Encoding has a NRZ logic 1 encoded as a 0-to-1 transition and a NRZ logic 0 encoded as a 1-to-0 transition.

DIGITAL CIRCUIT BLOCKS (continued)

Reverse Control Channel Access Arbitration

The AMPS and TACS specifications require a method of arbitration on the Reverse Control Channel to prevent two mobiles from transmitting on the same channel at the same time. This function is performed by DPROC monitoring the Busy/Idle stream sent on the Forward Control Channel.

The AMPS and TACS specifications state that once the mobile has commenced transmitting on the Reverse Control Channel it must monitor the Busy/Idle stream. If this stream becomes active outside a predetermined 'window', measured from the start of the transmission of the message, the mobile must terminate its transmission and disable the transmitter immediately.

In the Cellular Radio chip-set there are two levels of control of the RF transmitter; the first is absolute control by the System Controller, the second is conditional by other devices in the set. In DPROC the conditional control of the transmitter is performed via the output TXCTRL. This line is effectively wired ANDed together, using open-drain outputs, with other devices which may wish to control the transmitter. When these devices do not wish to disable the transmitter their output is in a HIGH impedance state.

An exception to this procedure occurs when the Serving System instructs the mobile not to monitor the Busy/Idle bits. In this event the arbitration logic can be disabled by clearing I^2C register bit ABREN.

The flow of events during a Control Channel Access attempt is as follows:

DEVELOPMENT DATA

Initial State

- transmitter power off via I^2C
- DPROC transmit circuitry in power-up state
- TXCTRL line HIGH

Access Attempt Procedure

1. System Controller decides to send message (note 1).
2. System Controller drives TXCTRL low directly.
3. System Controller switches transmitter power on and waits for power-up for the transmitter module (RF transmitter is still disabled by TXCTRL).
4. System Controller sets TXRST via I^2C to DPROC.
5. System Controller sets ABREN via I^2C (if required) allowing DPROC to control the transmitter.
6. System Controller determines status of Reverse Control Channel by monitoring the Busy/Idle bit. If busy, waits a random time then tries again.
7. System Controller releases TXCTRL allowing it to be pulled HIGH enabling the transmitter output.
8. System Controller transfers the first word of the message to DPROC via serial link (note 1).
9. DPROC sets I^2C signal TXIP and starts sending message while monitoring Busy/Idle status.
10. If channel becomes busy before 56 bits and ABREN is set then perform Abort Procedure.
11. If channel remains idle after 104 bits and ABREN is set then perform Abort Procedure.
12. System controller loads the subsequent words of the message into DPROC when the buffer becomes clear (Fig.15b).
13. On completion of entire message DPROC clears TXIP and 25 ms later the System Controller disables transmitter via I^2C.
14. System Controller finally sends TXRST to prepare DPROC for next transmission.

Note to the Access Attempt Procedure

1. At stage 1 the system controller may choose to preload DPROC with the first word of the message and hold it from transmission until stage 7 using the TXHOLD line. This gives a lower time overhead between detecting an IDLE channel and commencing the transmission. To use this feature TXHOLD must be driven HIGH before the last bit of data has been transferred into DPROC.
   Figure 16 illustrates the DPROC data transmission timing.

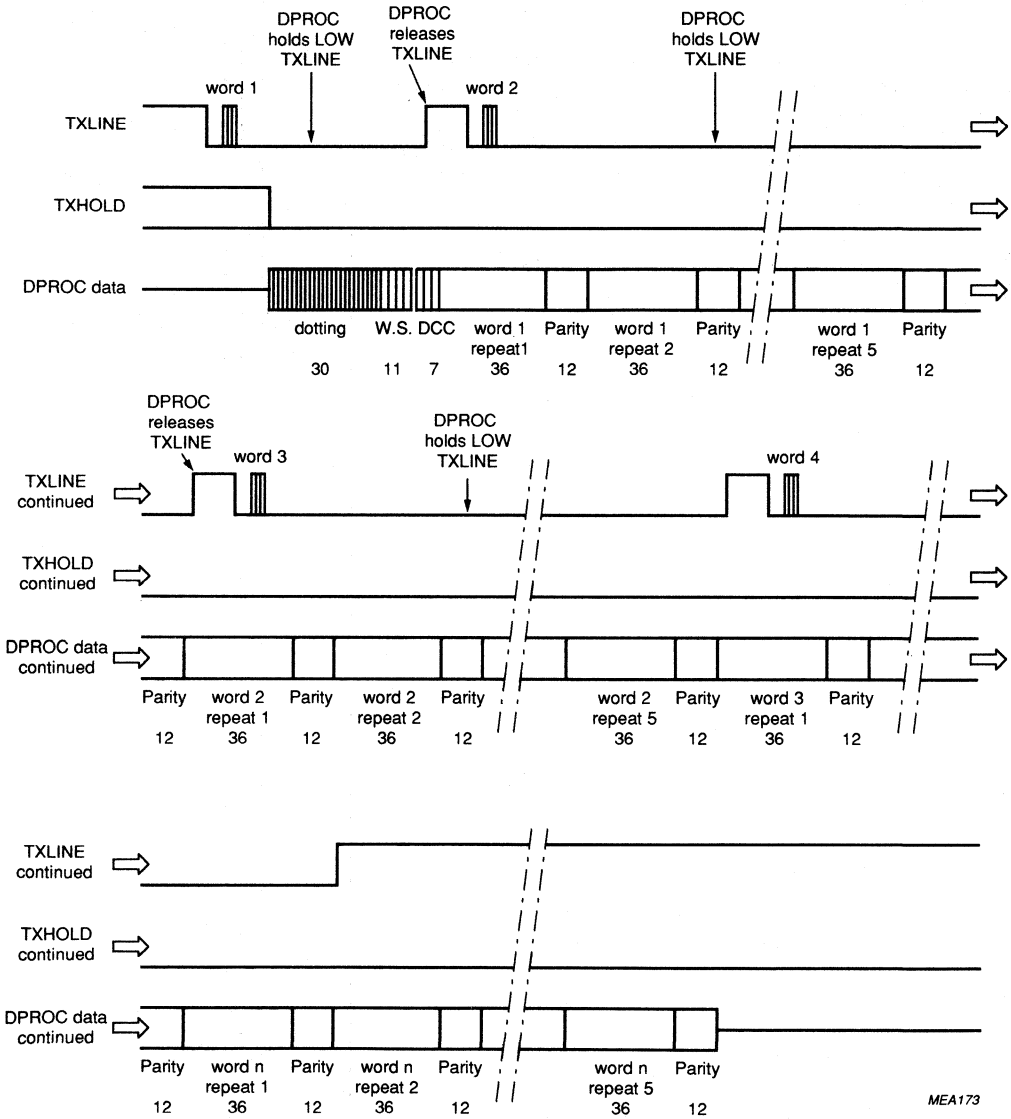


Fig. 16 DPROC data transmission timing/microcontroller interface.

DIGITAL CIRCUIT BLOCKS (continued)

Abort Procedure (see Fig. 17)

1. DPROC immediately disables transmitter output by driving TXCTRL low.
2. DPROC sets TXABRT.
3. System Controller detects failure by monitoring TXCTRL and TXABRT.
4. System Controller disables transmitter via RF power amplifier.
5. System Controller sends TXRST to prepare DPROC for next transmission.

Note

If a message is loaded into DPROC after a TXABRT has occured this word will remain in the DPROC transmit register and will not be cleared to TXRST.
If this situation arises the method of clearing the buffer ready for a second access attempt is to leave TXHOLD LOW and then send a TXRST prior to setting up a new transmission after TXLINE goes HIGH; this will clear any residual data in the buffer.

Signal Tone Generation (ST)

The 8 or 10 kHz (TACS or AMPS) tone generated from the Manchester Encoding Block is used as the Signalling Tone stream.

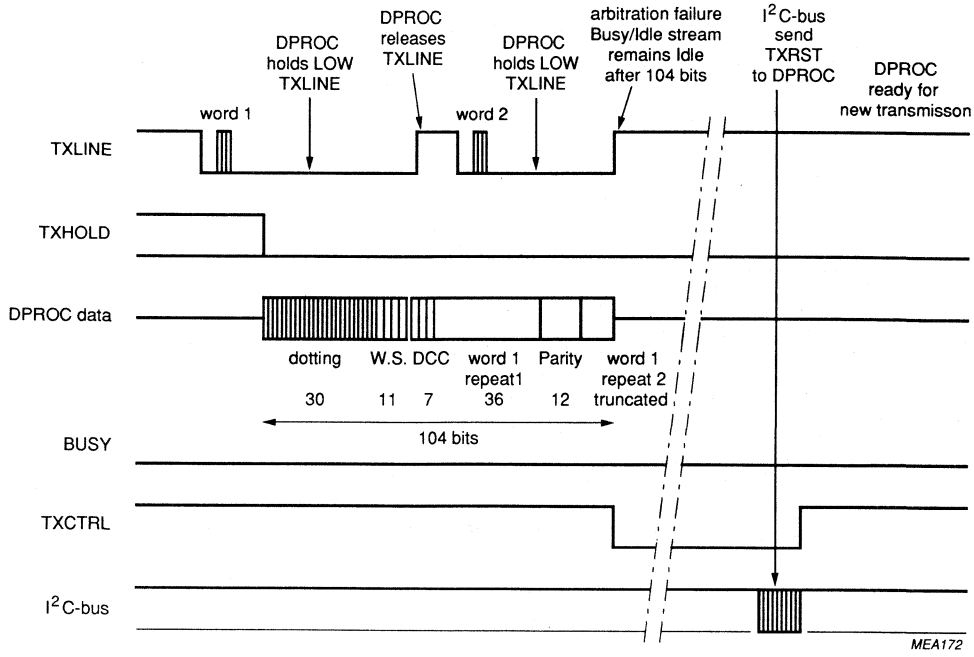


Fig. 17 DPROC data transmission timing/microcontroller interface during arbitration failure.

ANALOG CIRCUIT BLOCKS

General

The analog signal processing functions on DPROC are implemented using switched-capacitor techniques. The main filtering functions are operated at 300 kHz, and these circuits are 'interfaced' to the continuous time and sampled digital domains by distributed RC active filters, passive interpolators and comparators.

The distributed RC sections, the Anti-Alias Filter and the Clock Noise Filter, are non-critical and are designed to tolerate process spreads. The critical filtering in the SAT Filter and the Output Filter, is performed by 300 kHz switched-capacitor circuitry. The Passive Interpolators increase the sampling rate from 300 kHz to 1.2 MHz. The sampled analog signals from the Passive Interpolators are converted to sampled 2-state digital signals by the Strobed Comparators. The Gated Digital-to-Analog converters and Analog Summer blocks perform resynchronization and sub-sampling of the digitally generated DPROC output signals, and conversion to the sampled analog domain.

These analog section of the device are shown in Fig. 1.

Reference Voltage Generator

The Reference Voltage Generator generates the analog ground reference voltage (AGND) used internally within the DPROC device. To minimize noise AGND must be externally decoupled to V_{SSA} as shown in Fig. 18.

Anti-Alias Filter

The Anti-Alias Filter is placed before the SAT sampling block to prevent any unwanted signals or high-frequency noise present on the DEMODD pin being aliased into the pass-band by the sampling action of the switched-capacitor filter. To achieve this the Anti-Alias Filter is a continuous time-distributed RC-active low-pass filter.

SAT Input Filter

The SAT Input Filter is a switched-capacitor filter which provides band-pass filtering of the SAT signals from the DEMODD pin to improve the SAT signal-to-noise ratio prior to recovery and transponding.

Passive Interpolator

The function of the Passive Interpolator is to increase the sampling rate at the output of the switched-capacitor filters. This reduces the coarseness of the zero crossing information which would otherwise cause unacceptable isochronous distortion in the recovered signal.

Strobed Comparators

The Strobed Comparators form the analog-to-digital interface for the received data and SAT signals from the DEMODD pin. These comparators act as limiting amplifiers wich convert the filtered sampled analog signals into 2-state sampled digital signals containing only the zero-crossing information from the analog signal.

Gated Digital-to-Analog and Analog Summer

The Gated Digital-to-Analog converters and Analog Summer form the interface between the digital and analog circuitry on the transmit path of DPROC. It is at this point that the three sampled digital signals, containing SAT, ST and encoded digital data, are combined to form a composite signal.
The data streams are enabled by the I²C signals STEN, SATEN and the internal signal DATAEN respectively (DATAEN disables SAT and ST when data is being transmitted). The digital-to-analog conversion and sub-sampling operation is performed by the Gated Digital-to-Analog converters and Analog Summer. The relative signal weights applied in the summer (with respect to the data path) are shown in Table 9.

Table 9 Relative signal weights

signal	relative output level AMPS and TACS
ST	1.0
SAT	0.25
DATA	1.0

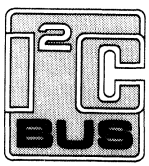
Output Filter

The Output Filter is a switched-capacitor filter which performs band-limiting of the DPROC output signals in accordance with the AMPS and TACS specifications. The required below band roll-off is achieved via external AC coupling from the DATA pin.

Clock Noise Filter

The filter is a non-critical continuous time-distributed RC-active low-pass filter used to remove any switching transient residues from the output signal.

DEVELOPMENT DATA



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

APPLICATION INFORMATION

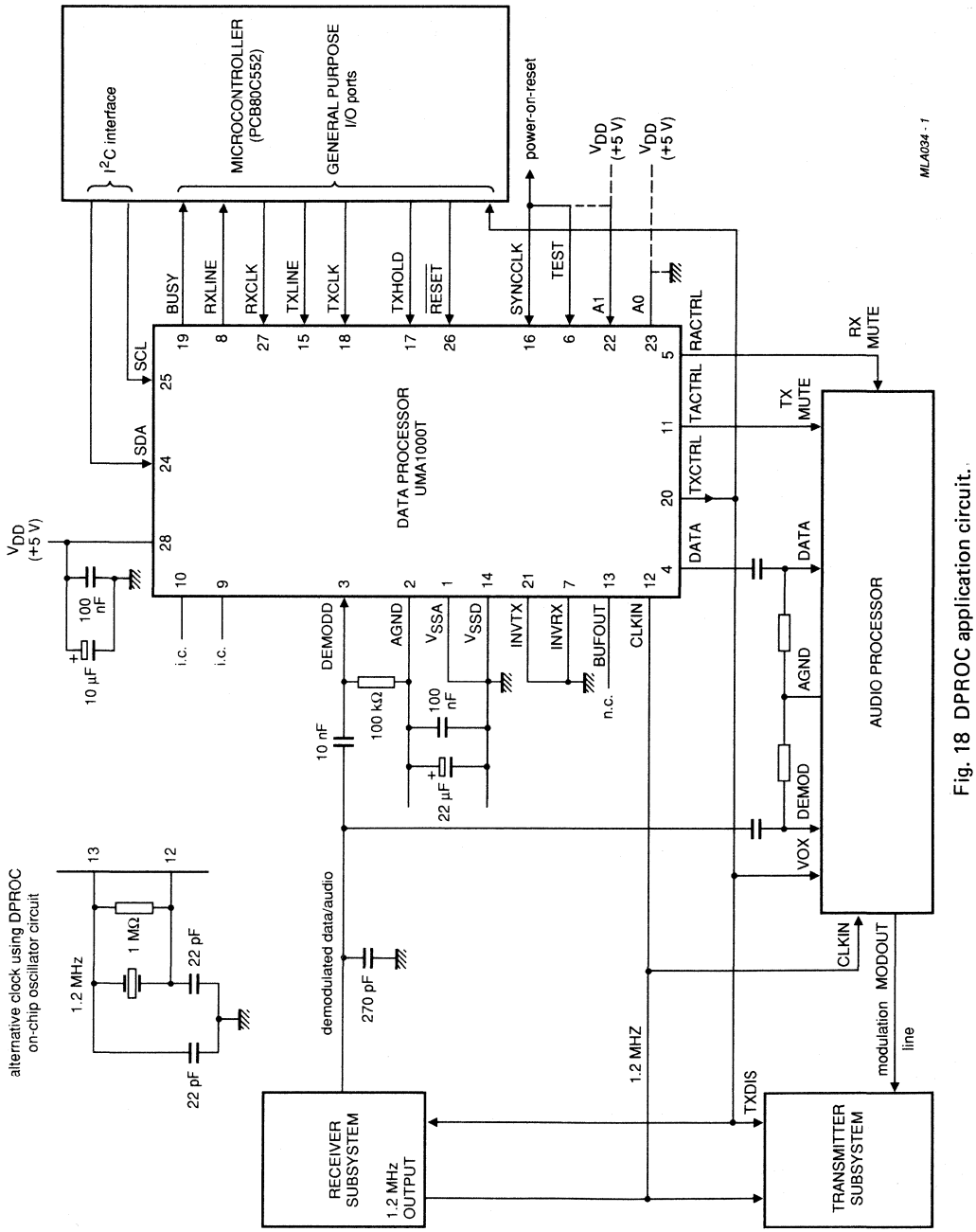


Fig. 18 DPROC application circuit.

LOW-POWER UNIVERSAL SYNTHESIZER FOR RADIO COMMUNICATION

DESCRIPTION

The UMA1010T is a low-power universal synthesizer for radio communication. The IC is manufactured in bipolar technology and is designed to achieve 10 kHz to 100 kHz channel spacing in the frequency band of 400 MHz to 1.15 GHz.
The channel is selected via the standard I^2C-two line serial bus.
The UMA1010T has an integrated low-power prescaler (up to 1150 MHz), a low-noise 5 to 15 V amplifier for the loop filter and a programmable reference divider oscillator.
Power down circuitry enables the device to be idled.

Features

- Fully programmable RF divider from 400 MHz to 1150 MHz
- I^2C-bus interface for two-line serial data transfer
- On-chip crystal oscillator from 3 MHz to 16 MHz; circuit can be used with a crystal or a temperature compensated crystal oscillator (TCXO)
- A frequency divider generates a reference frequency between 5 kHz and 50 kHz with a large number of crystal frequencies
- Crystal frequency divide-by-eight output
- Digital comparator that provides a wide pull-in range
- High gain sample-and-hold phase comparator to achieve a low noise and a high reference rejection
- On-chip out-of-lock indication
- Two extra VCO control outputs
- Latched synthesizer alarm signal output
- Status register including out-of-lock and power failure indication
- On-chip power-on-reset presetting the registers
- Low-noise high-voltage operational amplifier allowing a large tuning range at the VCO
- Programmable phase comparator gain
- Power down possibilities via the I^2C-bus or the $\overline{HPD}$ pin

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage ranges					
digital + 5 V	V_P	4.5	5.0	5.5	V
analog + 5 to 15 V	V_{P1}	4.5	–	16.5	V
analog + 5 V	V_{P2}	4.5	5.0	5.5	V
Operating current					
V_P (digital) = 5 V	I_P	–	13.5	–	mA
V_{P1} (analog) = + 5 to 15 V	I_{P1}	–	1.0	–	mA
V_{P2} (analog) = 5 V	I_{P2}	–	1.0	–	mA
Total current in power down mode	$I_P + I_{P1} + I_{P2}$	–	3.5	–	mA
RF input frequency range	f_{RFI}	400	–	1150	MHz
Crystal frequency range	f_{XTAL}	3	–	16	MHz
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

PACKAGE OUTLINE

28-lead mini-pack; plastic (SOT136A).

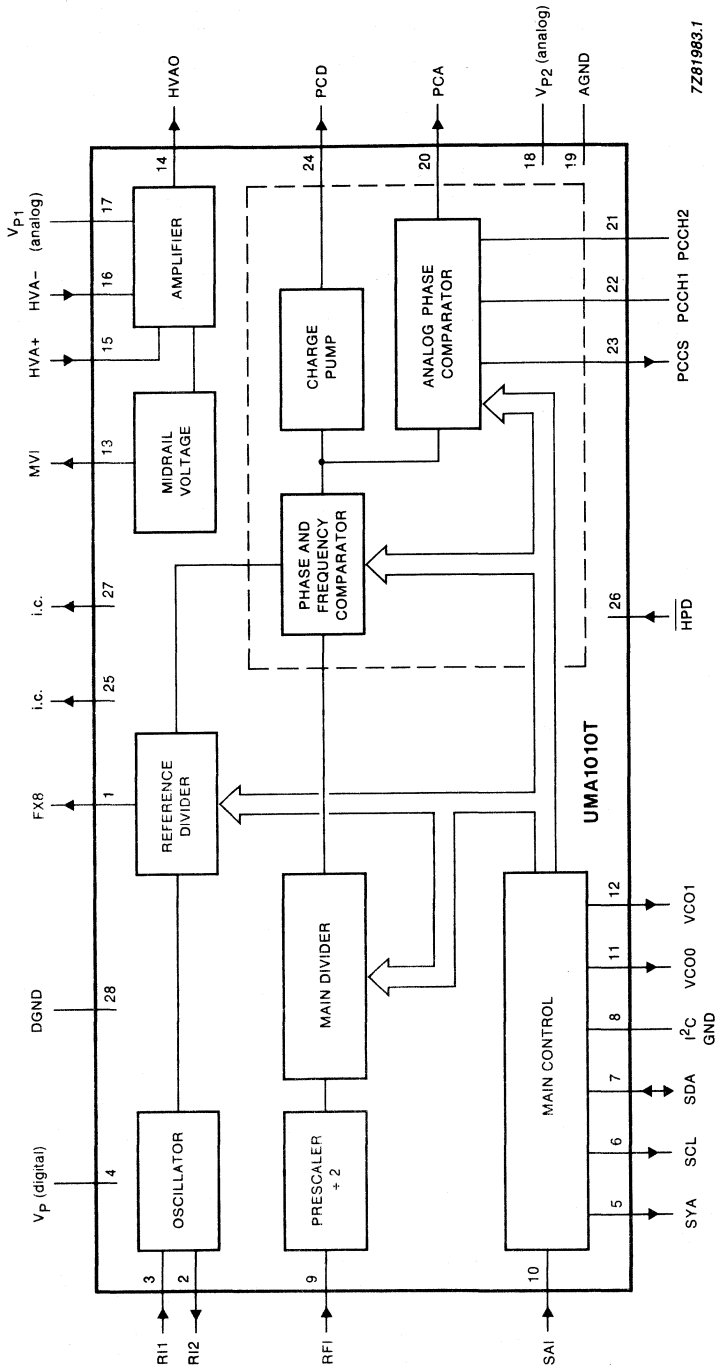


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

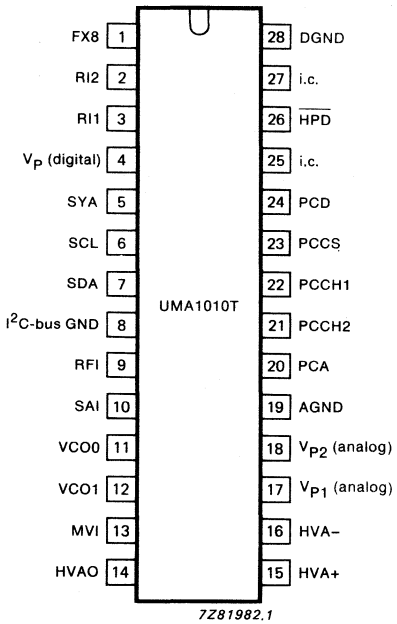
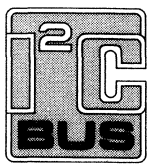


Fig. 2 Pinning diagram.

1	FX8	Output reference prescaler	
2	RI2	Reference input 2	
3	RI1	Reference input 1	
4	V_P	Digital + 5 V supply	
5	SYA	Synthesizer alarm	
6	SCL	Serial clock line	I²C-bus
7	SDA	Serial data line; input/output	I²C-bus
8	IGND	Ground for I²C-bus	
9	RFI	RF input	
10	SA1	Slave address select input	
11	VCO0	Oscillator buffer switch output 0	
12	VCO1	Oscillator buffer switch output 1	
13	MV1	Mid-rail voltage (not buffered)	
14	HVAO	Output high-voltage amplifier	
15	HVA+	Non-inverting input high-voltage amplifier	
16	HVA−	Inverting input high voltage amplifier	
17	V_{P1}	Analog + 5 to + 15 V supply	
18	V_{P2}	Analog + 5 V supply	
19	AGND	Analog ground	
20	PCA	Analog phase comparator output	
21	PCCH2	Phase comparator external hold capacitor node 2	
22	PCCH1	Phase comparator external hold capacitor node 1	
23	PCCS	Phase comparator external sampling capacitor node	
24	PCD	Digital phase comparator output	
25	i.c.	Internally connected	
26	$\overline{HPD}$	Inverting hardware power-down input	
27	i.c.	Internally connected	
28	DGND	Digital ground	



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

FUNCTIONAL DESCRIPTION

Power supply

V_P (digital) is the + 5 V supply which feeds the dividers, the control and the digital part of the comparator. V_{P1} (analog) is the + 5 to + 15 V supply for the amplifier output stage. The + 5 V analog supply is V_{P2} (analog) which should be very clean to prevent spurious signal on the VCO control voltage.

Main divider

The main divider is a fully programmable divider. The division ratio range is from 2048 to 262142 in steps of two. It is sufficient for 10 kHz channel spacing with an input of 1050 MHz. Due to the fixed divide-by-two prescaler, half of the ratio is programmed via the I^2C-bus in the Registers C, D and E (see Table 1).

Table 1 1/2 ratio in binary form

MSB															LSB
0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
C ←				D			→	←				E			→	

The new programmed ratio is only updated after programming Register E. If the programmed ratio is less than 2048 then 2048 will be added to it.

Oscillator

To provide the reference frequency, two modes of operation exist:

- Use an external resonator connected between RI1 and RI2
- Use an external reference source such as a TCXO on R11

Reference divider

Table 2 Division ratios as a function of the program

	RD0	0	1	0	1
	RD1	0	0	1	1
RD3	RD2				
0	0	128	160	192	240
0	1	256	320	384	480
1	0	512	640	768	960
1	1	1024	1280	1536	1920

One eighth of the frequency is available on pin 1 (FX8). It can be used as a reference frequency input for other circuits.

Phase comparator

The phase comparator includes two comparators:

- Digital 3-state comparator with charge pump output (PCD) which provides a wide pull-in range
- High-gain sample-and-hold analog phase comparator output (PCA) gives the possibility of high performance.

The analog phase comparator gives an "out-of-lock" indication when the loop phase error is outside its linear range or if one of its inputs is missing. In the event of one of these, PCA is 3-state and PCD pushes or pulls 300 μA for the duration of the phase error.

$$\text{PCD gain} = \frac{300\ \mu A}{2 \times \pi}\ (A/rad)$$

Under "in-lock" condition PCD goes to 3-state and PCA becomes active. If the bit PCD select is set PCD remains active, this is used in systems which need minimum complexity. The sampling capacitor (C_{pccs}) is connected between PCCS and GND. CC fixes the gain of the phase comparator.

$$\text{PCA gain} = \frac{2 \times I_{pccs}}{\pi \times C_{pccs} \times f_{ref}}\ (V/rad)$$

where C_{pccs} is the sampling capacitor and f_{ref} is the reference frequency and I_{pccs} is the output current on PCCS depending on the gain.
Four output current values of I_{pccs} can be selected via the I^2C-bus which correspond to the following gain factors; + 6 dB, + 2 dB, −2 dB and −6 dB. The nominal value at 0 dB is 300 μA. The output current at −2 dB is given in the characteristics.

The hold capacitor is connected between PCCH1 and PCCH2. The sample-and-hold is designed to suppress the reference frequency at the output of the phase comparator.

Main control

Two formats for the I^2C-bus protocol have been implemented on the UMA1010T:

- Burst mode, this includes subaddressing and selectable auto-increment for writing information to the synthesizer
- Single byte without subaddressing for reading the status register of the synthesizer.

The status register contains information related to the synthesizer alarm (SYA) as shown in Table 3.

Table 3 Status register

MSB							LSB
0	0	0	00L	0	L00L	LPD	DI

Where: 00L = momentarily out of lock
L00L = latched out of lock
LPD = latched power dip
DI = disable interrupt

The alarm is generated by an "out-of-lock" or a power dip and is reset when the register is read. If one of these conditions occurs SYA is forced LOW.

DEVELOPMENT DATA

I²C-BUS DEFINITION BIT ALLOCATION

The I²C-bus data format to write on the synthesizer has the following form:

START – address – subaddress – data 1 – data 2 – . . . – data n – STOP where:

address 1 1 0 0 0 0 SA1 R/$\overline{W}$

SA1 is logic level on pin SA1
R/$\overline{W}$ is read/not write

subaddress 0 0 0 DI AVI SB2 SB1 SB0

DI is disable interrupt, DI = 1 disables the alarm on SYA.
AVI is auto value increment, AVI = 1 allows increment of the register pointer.
SB3 – SB0 is register pointer, it indicates the register number where data 1 will be written. The pointer value is 0 for Register A up to 4 for Register E.

data n (n up to 5)

register	pointer	bit allocation								preset values		
		7	6	5	4	3	2	1	0	decimal	binary	hexa-decimal
A	000	PD	X	X	PCD	RD3	RD2	RD1	RD0	14	00001110	0E
B	001	VCO1	X	X	VCO0	X	X	X	X	16	00010000	10
C	010	X	0	X	X	1	PCG2	PCG1	MD16	173	10101101	A0
D	011	MD15	MD14	MD13	MD12	MD11	MD10	MD9	MD8	56	00111000	38
E	100	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	128	10000000	80

Register A is: PD (Power down), PD = 0 is normal operation.
PCD (PCD select), PCD = 1 PCD is always active.
RD3 . . . RD0 (reference division ratio), see Table 2 preset 1536

Register B is: VCO1 set VCO1 pin.
VCO0 set VCO0 pin, VCO0 is forced LOW during an "out-of-lock" indication.

Register C is: PCG2, PCG1, i.e. sets the gain of the phase comparator;
preset + 2 dB
00 –6 dB
01 –2 dB
10 + 2 dB
11 + 6 dB
MD16, MSB of the main division ratio.

Register D is: MD15 to MD8, division ratio bit 15 to 8.

Register E is: MD7 to MD0, division ratio bit 7 to 0. Preset 160000.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage ranges				
digital + 5 V	V_P	4.5	5.5	V
analog + 5 to + 15 V	V_{P1}	4.5	16.5	V
analog + 5 V	V_{P2}	4.5	5.5	V
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	−40	+ 125	°C

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 5 V; V_{P1} = 15 V; V_{P2} = 5 V; unless otherwise specified

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
SUPPLY						
Supply voltage ranges						
digital + 5 V		V_P	4.5	5	5.5	V
analog + 5 to + 15 V		V_{P1}	4.5	–	16.5	V
analog + 5 V		V_{P2}	4.5	5	5.5	V
Supply current ranges						
digital + 5 V		I_P	–	13.5	19	mA
analog + 5 to + 15 V		I_{P1}	–	1.0	1.5	mA
analog + 5 V		I_{P2}	–	1.0	1.5	mA
Power down + 5 V		I_{pd}	–	3.5	4.5	mA
MAIN DIVIDER						
Division ratio	step = 2		2048	–	262142	
RF input (RFI)						
Frequency range		f_{RFI}	400	–	1150	MHz
Input voltage level (RMS value)	Fig.3	$V_{i(rms)}$	50	–	150	mV
Input impedance	note 1	R_{RFI}	–	–	–	Ω
Shunt resistance	f_{RFI} = 500 MHz	R_S	–	800	–	Ω
	f_{RFI} = 700 MHz	R_S	–	400	–	Ω
	f_{RFI} = 1000 MHz	R_S	–	310	–	Ω
Shunt capacitance	f_{RFI} = 500 MHz	C_S	–	1.5	–	pF
	f_{RFI} = 700 MHz	C_S	–	1.3	–	pF
	f_{RFI} = 1000 MHz	C_S	–	1.2	–	pF

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
MAIN CONTROL						
Serial clock input (SCL)						
Serial data input (SDA)						
Clock frequency		f_{CLK}	0	–	100	kHz
Input voltage HIGH		V_{IH}	3	–	–	V
Input voltage LOW		V_{IL}	–	–	1.0	V
Input current HIGH		I_{IH}	–	0.1	3.0	μA
Input current LOW		I_{IL}	−3	−1	–	μA
Input capacitance		C_I	–	20	–	pF
SDA sink current	V_{OL} = 0.4 V	I_{OL}	–	–	3	mA
Slave address select input (SA1)	note 2					
Input voltage HIGH		V_{IH}	3	–	–	V
Input voltage LOW		V_{IL}	–	–	0.4	V
Input current HIGH		I_{IH}	–	–	0.2	μA
Input current LOW		I_{IL}	−3.0	−1.5	–	μA
Oscillator buffer switch output 0 (VCO0)	note 3					
Output voltage LOW		V_{OL}	–	–	0.2	V
Sink current LOW		I_{OL}	–	–	400	μA
Oscillator buffer switch output 1 (VCO1)						
Output voltage LOW		V_{OL}	–	–	0.2	V
Sink current LOW		I_{OL}	–	–	400	μA
Inverting hardware power down input ($\overline{HPD}$)	note 2					
Input voltage HIGH		V_{IH}	3	–	–	V
Input voltage LOW		V_{IL}	–	–	0.4	V
Input current HIGH		I_{IH}	–	0.1	0.3	μA
Input current LOW		I_{IL}	−15	−8	–	μA
Synthesizer alarm (SYA)	note 4					
Output voltage LOW		V_{OL}	–	–	0.2	V
Output current LOW		I_{OL}	–	–	400	μA

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
OSCILLATOR						
Reference input 1 (RI1)						
Frequency range	crystal	f_{ref1}	3	–	16	MHz
	TCXO	f_{ref1}	1	–	16	MHz
Input level (RMS value)	sinewave	$V_{ref1(rms)}$	0.1	–	2	V
Input level (peak-to-peak value)	square wave	$V_{ref1(p-p)}$	0.3	–	5	V
Reference input 2 (RI2)	note 5					
Frequency range	crystal	f_{ref2}	3	–	16	MHz
	TCXO	f_{ref2}	1	–	16	MHz
Output impedance		Z_o	–	2	–	kΩ
REFERENCE DIVIDER						
Division ratio			128	–	1920	
Input frequency range		f_i	1	–	16	MHz
Output frequency range		f_o	5	–	50	kHz
Output reference prescaler (FX8)	note 6					
Voltage output LOW		V_{OL}	–	–	0.5	V
Sink current LOW		I_{OL}	–	–	1.5	mA
PHASE COMPARATOR						
Frequency range		f	5	–	50	kHz
Digital phase comparator output (PCD)	note 7					
Output source current		I_O	−250	−300	−400	μA
Output sink current		I_O	250	300	400	μA
Output leakage current	$V_{pcd} = 2.5$ V	$\|I_{LO}\|$	–	1	70	nA
Phase comparator external sampling capacitor node (PCCS)	note 8					
Capacitance to ground		C_{PCCS}	60	–	200	pF
Output leakage current	$V_{pccs} = 2.5$ V	$\|I_{LO}\|$	–	1	70	nA
Phase comparator external hold capacitor nodes 1 and 2 (PCCH1; PCCH2)						
Hold capacitor		C_{HOLD}	–	1	–	nF

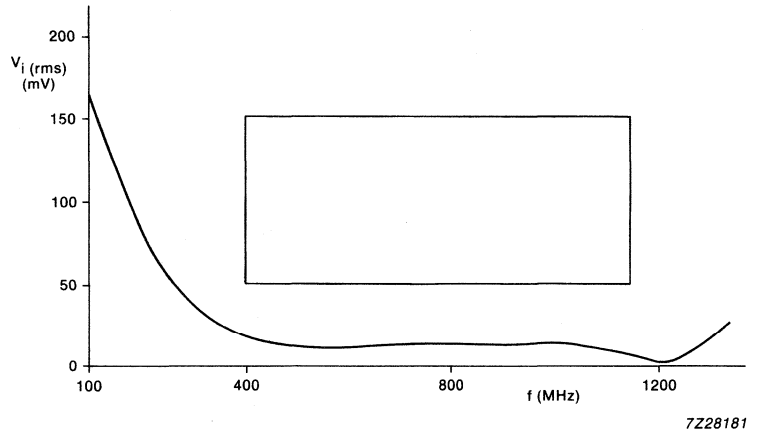
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Analog comparator output (PCA)						
Output source current		$-I_O$	−300	–	–	μA
Output sink current		I_O	–	–	300	μA
Output leakage current	V_{PCA} = 2.5 V	I_{LO}	–	–	250	nA
Gain	f_o = 6.24 kHz; C_{pccs} = 100 pF; PCG = + 2 dB	G_v	–	387	–	V/rad
Output source/sink current	PCG = + 2 dB	I_{pccs}	330	380	430	μA
LOOP AMPLIFIER						
Mid-rail voltage; not buffered (MV1)						
AC decoupling		C_{MV1}	–	47	–	μF
Non-inverting high voltage amplifier input (HVA+)	note 9					
AC decoupling		C_{HVA}	–	1	–	nF
Inverting high voltage amplifier input (HVA−)						
Input impedance	0 to 10 kHz	Z_i	–	1	–	mΩ
Input noise	0.3 to 3 kHz	N_{af}	–	10	–	nV/√Hz
Bias current		I_B	–	15	–	nA
High voltage amplifier output (HVAO)						
Open loop voltage gain		G_{ol}	30	60	–	dB
Output voltage		V_O	2	–	$V_{P1}-0.4$	V
Unity gain bandwidth		B_G = 1	–	2	–	MHz
Open loop output resistance		R_O	–	70	–	kΩ
Output current		I_O	300	350	–	μA

Notes to the characteristics

1. The input impedance is given as the parallel combination of shunt resistance and shunt capacitance.
2. When left open is HIGH.
3. During out-of-lock the VCO0 pin is forced LOW.
4. This pin is an open-collector output.
5. If a TCXO is used this pin is to remain open or be used as a reference frequency output.
6. This pin is an open-collector output of the reference frequency divided by eight.
7. This pin is active when out-of-lock is indicated and will be 3-state when the analog phase comparator takes over after the in-lock indication.
8. The capacitor on this pin fixes the gain of the analog phase comparator.
9. This pin is connected internally, via a buffer, to MVI.

DEVELOPMENT DATA



▭ Operation of the device is guaranteed for input levels in this region over the full operating voltage and temperature range.

—— Typical measurement at V_P = 5 V; T_{amb} = 25 °C.

Fig.3 Input sensitivity.

APPLICATION INFORMATION

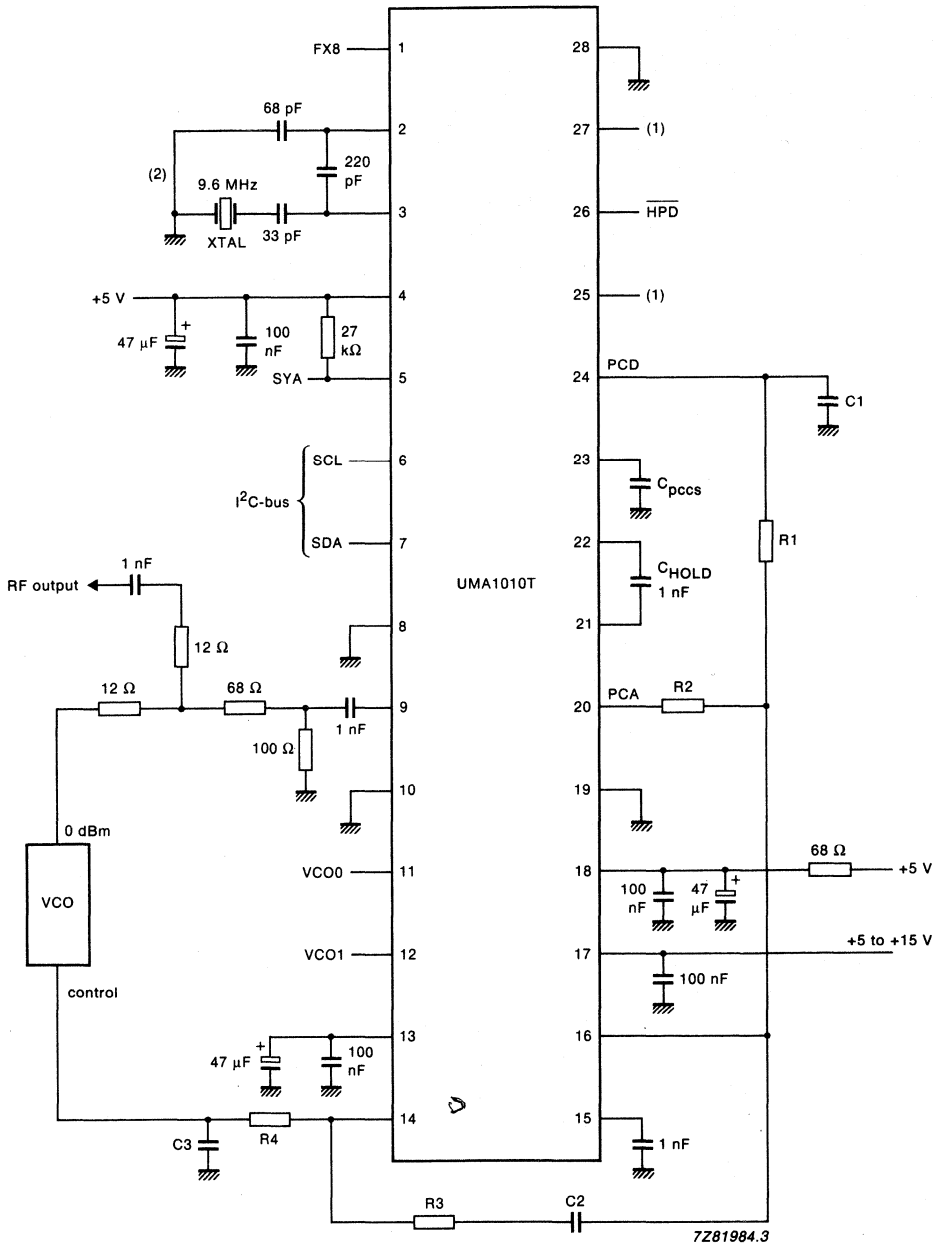


Fig.4 Synthesizer application.

(1) not to be connected.

(2) for an application using a temperature compensated crystal oscillator (TCXO), only pin 3 should be connected to TCXO and pin 2 should be left open circuit.

DEVELOPMENT DATA

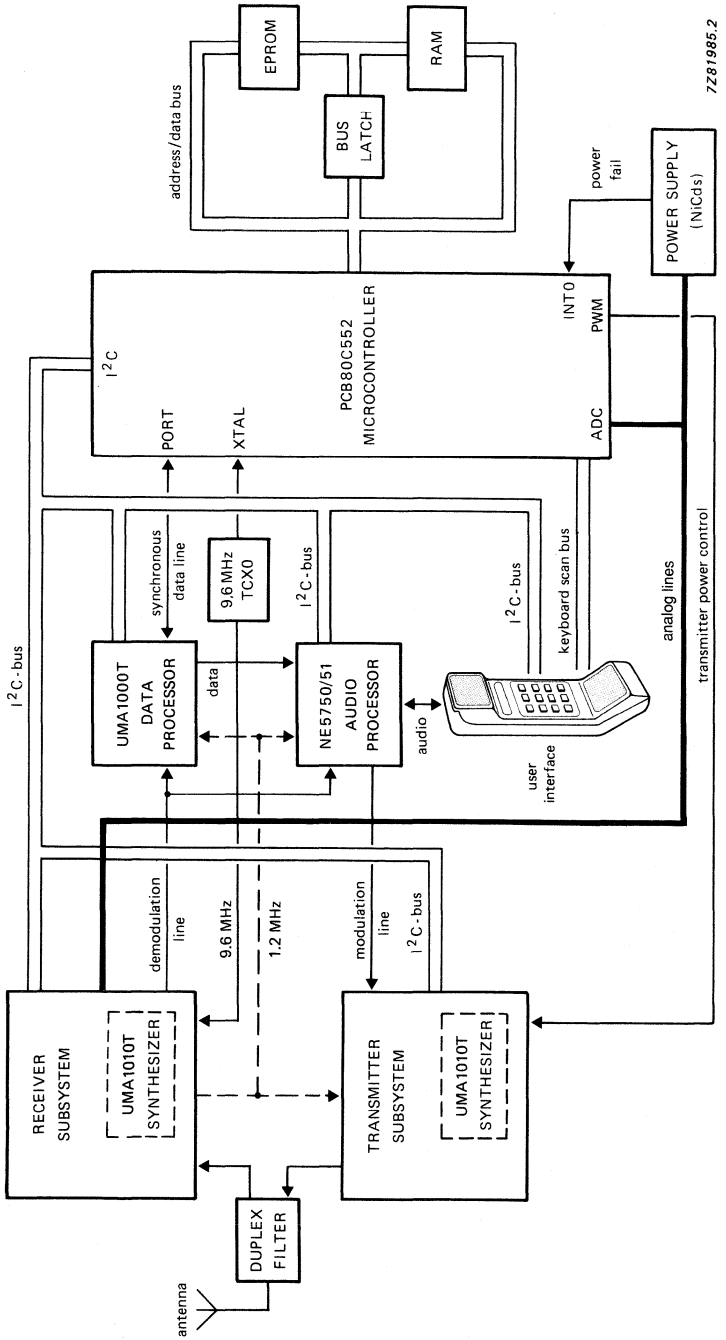


Fig.5 Cellular radio system schematic.

The UM1010T is a member of our Cellular Radio chipset, based on the I²C-bus, which meets the key requirements of a hand-held portable cellular set:

- small physical size
- minimum number of interconnections (serial bus)
- low power consumption
- low cost

LOW-POWER UNIVERSAL SYNTHESIZER FOR RADIO COMMUNICATION

DESCRIPTION

The UMA1012T is a low-power universal synthesizer for radio communication. The IC is manufactured in bipolar technology and is designed to achieve 5 kHz to 50 kHz channel spacing in the frequency band of 20 MHz to 600 MHz.
The channel is selected via the standard I^2C-two-line serial bus.
The UMA1012T has an integrated low-noise + 5 to + 15 V amplifier for the loop filter and a programmable reference divider oscillator.
Power down circuitry enables the device to be idled.

Features

- Fully programmable RF divider from 20 MHz to 600 MHz
- I^2C-bus interface for two-line serial data transfer
- On-chip crystal oscillator from 3 MHz to 16 MHz; circuit can be used with a crystal or a temperature compensated crystal oscillator (TCXO)
- A frequency divider that generates a reference frequency between 5 kHz and 50 kHz with a large number of crystal frequencies
- Crystal frequency divide-by-eight output
- Digital comparator that provides a wide pull-in range
- High gain sample-and-hold phase comparator to achieve a low noise and a high reference rejection
- On-chip out-of-lock indication
- Two extra VCO control outputs
- Latched synthesizer alarm signal output
- Status register including out-of-lock and power failure indication
- On-chip power-on-reset presetting the registers
- Low-noise high-voltage operational amplifier allowing a large tuning range at the VCO
- Programmable phase comparator gain
- Power down possibilities via the I^2C-bus or the $\overline{HPD}$ pin

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage ranges					
digital + 5 V	V_P	4.5	5.0	5.5	V
analog + 5 to + 15 V	V_{P1}	4.5	–	16.5	V
analog + 5 V	V_{P2}	4.5	5.0	5.5	V
Operating currents					
V_P(digital) = 5 V	I_P	–	13.5	–	mA
V_{P1} (analog) = + 5 to + 15 V	I_{P1}	–	1	–	mA
V_{P2} (analog) = 5 V	I_{P2}	–	1	–	mA
Total current in power down mode	$I_P + I_{P1} + I_{P2}$	–	3.5	–	mA
RF input frequency range	f_{RFI}	20	–	600	MHz
Crystal frequency range	f_{XTAL}	3	–	16	MHz
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

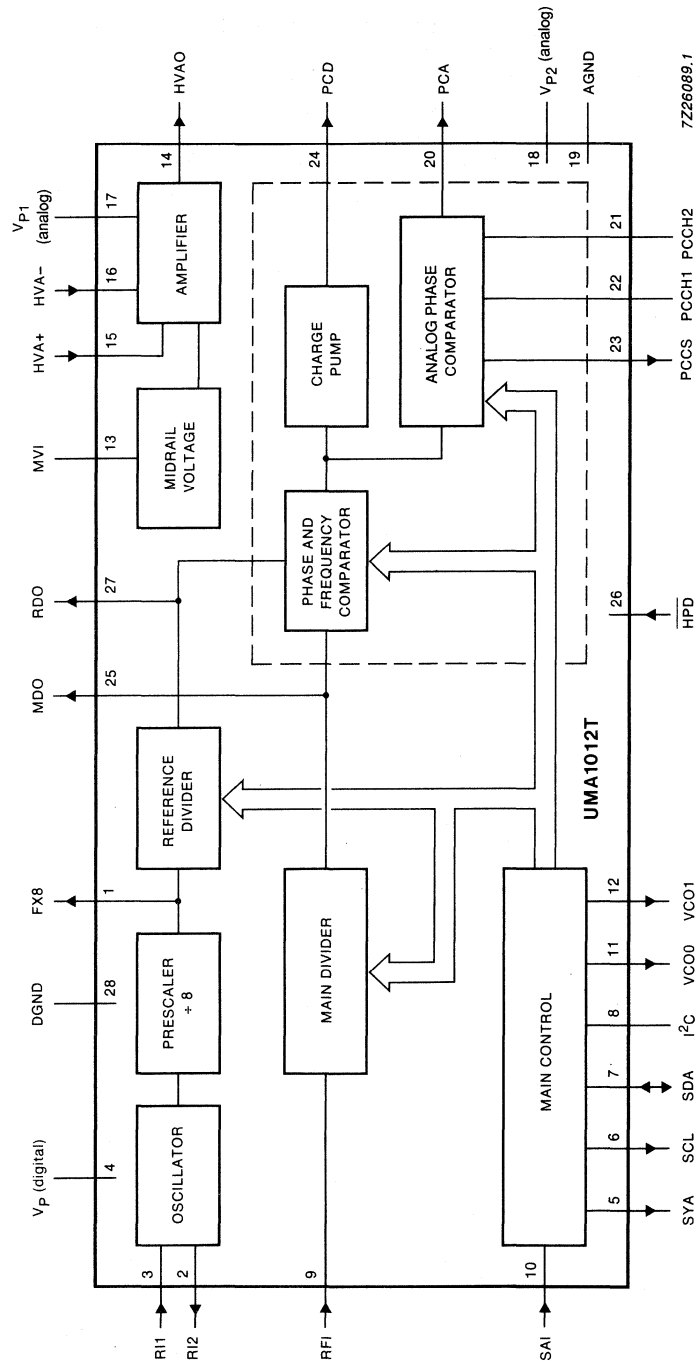


Fig.1 Block diagram.

DEVELOPMENT DATA

PINNING

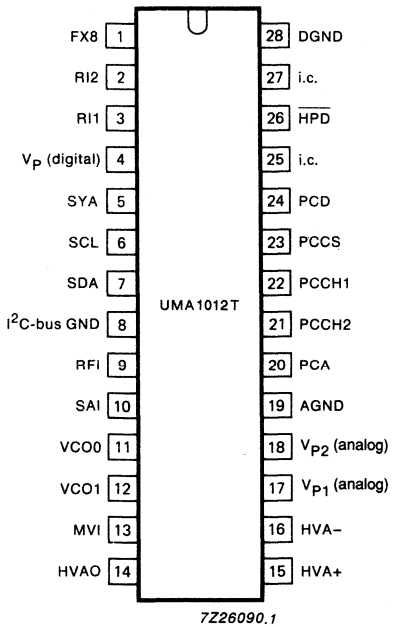


Fig.2 Pinning diagram.

1	FX8	Output reference prescaler
2	RI2	Reference input 2
3	RI1	Reference input 1
4	V_P	Digital + 5 V supply
5	SYA	Synthesizer alarm
6	SCL	Serial clock line (I^2C-bus)
7	SDA	Serial data line; input/output (I^2C-bus)
8	I^2C-bus GND	Ground for I^2C-bus
9	RFI	RF input
10	SA1	Slave address select input
11	VCO0	Oscillator buffer switch output 0
12	VCO1	Oscillator buffer switch output 1
13	MV1	Mid-rail voltage (not buffered)
14	HVAO	Output high-voltage amplifier
15	HVA+	Non-inverting input high-voltage amplifier
16	HVA−	Inverting input high voltage amplifier
17	V_{P1}	Analog + 5 to + 15 V supply
18	V_{P2}	Analog + 5 V supply
19	AGND	Analog ground
20	PCA	Analog phase comparator output
21	PCCH2	Phase comparator external hold capacitor node 2
22	PCCH1	Phase comparator external hold capacitor node 1
23	PCCS	Phase comparator external sampling capacitor node
24	PCD	Digital phase comparator output
25	i.c.	Internally connected
26	$\overline{HPD}$	Inverting hardware power-down input
27	i.c.	Internally connected
28	DGND	Digital ground

FUNCTIONAL DESCRIPTION

Power supply

V_P (digital) is the + 5 V supply which feeds the dividers, the control and the digital part of the comparator. V_{P1} (analog) is the + 5 to + 15 V supply for the amplifier output stage. The + 5 V analog supply is V_{P2} (analog) which should be very clean to prevent spurious signal on the VCO control voltage.

Main divider

The main divider is a fully programmable divider. The division range is from 1024 to 131071. It is sufficient for 5 kHz channel spacing with an input of 500 MHz. The ratio is programmed via the I^2C-bus in the Registers C, D and E (see Table 1).

Table 1 Ratio in binary form

MSB															LSB
0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
C ←				D				→	←			E				→

The new programmed ratio is only updated after programming Register E. If the programmed ratio is less than 2048, then 2048 will be added to it.

Oscillator

To provide the reference frequency, two modes of operation exist:

- Use an external resonator connected between RI1 and RI2
- Use an external reference source such as a TCXO on RI1

Reference divider

Table 2 Division ratios as a function of the program

	RD0	0	1	0	1
	RD1	0	0	1	1
RD3	RD2				
0	0	128	160	192	240
0	1	256	320	384	480
1	0	512	640	768	960
1	1	1024	1280	1536	1920

One eighth of the crystal frequency is available on pin 1 (FX8). It can be used as a reference frequency input for other circuits.

Phase comparator

The phase comparator includes two comparators:

- Digital 3-state comparator with charge pump output (PCD) which provides a wide pull-in range
- High-gain sample-and-hold analog phase comparator output (PCA) gives the possibility of high performance.

The analog phase comparator gives an "out-of-lock" indication when the loop phase error is outside its linear range or if one of its inputs is missing. In the event of one of these, PCA is 3-state and PCD pushes or pulls 300 μA for the duration of the phase error.

$$\text{PCD gain} = \frac{300\ \mu A}{2 \times \pi}\ (\text{A/rad})$$

Under "in-lock" condition PCD goes to 3-state and PCA becomes active. If the bit PCD select is set PCD remains active, this is used in systems which need minimum complexity. The sampling capacitor (C_{pccs}) is connected between PCCS and GND. CC fixes the gain of the phase comparator.

$$\text{PCA gain} = \frac{2 \times I_{pccs}}{\pi \times C_{pccs} \times f_{ref}}\ (\text{V/rad})$$

where C_{pccs} is the sampling capacitor and f_o is the reference frequency and I_{pccs} is the output current on PCCS depending on the gain.
Four output current values of I_{pccs} can be selected via the I^2C-bus which correspond to the following gain factors; + 6 dB, + 2 dB, −2 dB and −6 dB. The nominal value at 0 dB is 300 μA. The output current at −2 dB is given in the characteristics.

The hold capacitor is connected between PCCH1 and PCCH2. The sample-and-hold is designed to suppress the reference frequency at the output of the phase comparator.

Main control

Two formats for the I^2C-bus protocol have been implemented on the UMA1012T:

- Burst mode, this includes subaddressing and selectable auto-increment for writing information to the synthesizer
- Single byte without subaddressing for reading the status register of the synthesizer

The status register contains information related to the synthesizer alarm (SYA) as shown in Table 3.

Table 3 Status register

MSB							LSB
0	0	0	00L	0	L00L	LPD	DI

Where: 00L = momentarily out of lock
L00L = latched out of lock
LPD = latched power dip
DI = disable interrupt

The alarm is generated by an "out-of-lock" or a power dip and is reset when the register is read. If one of these conditions occurs SYA is forced LOW.

DEVELOPMENT DATA

I²C-BUS DEFINITION BIT ALLOCATION

The I²C-bus data format to write on the synthesizer has the following form:

START – address – subaddress – data 1 – data 2 – . . . – data n – STOP where:

address 1 1 0 0 0 0 SA1 R/$\overline{W}$

SA1 is logic level on pin SA1
R/$\overline{W}$ is read/not write

subaddress 0 0 0 DI AVI SB2 SB1 SB0

DI is disable interrupt, DI = 1 disables the alarm on SYA.
AVI is auto value increment, AVI = 1 allows increment of the register pointer.
SB3 – SB0 is register pointer, it indicates the register number where data 1 will be written. The pointer value is 0 for Register A up to 4 for Register E.

data n (n up to 5)

register	pointer	bit allocation								preset values		
		7	6	5	4	3	2	1	0	decimal	binary	hexa-decimal
A	000	PD	X	X	PCD	RD3	RD2	RD1	RD0	14	00001110	0E
B	001	VCO1	X	X	VCO0	X	X	X	X	16	00010000	10
C	010	X	0	X	X	1	PCG2	PCG1	MD16	173	10101101	AD
D	011	MD15	MD14	MD13	MD12	MD11	MD10	MD9	MD8	56	00111000	38
E	100	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	128	10000000	80

Register A is: PD (Power down), PD = 0 is normal operation.
PCD (PCD select), PCD = 1 PCD is always active.
RD3 . . . RD0 (reference division ratio), see Table 2 preset 1536.

Register B is: VCO1 set VCO1 pin.
VCO0 set VCO0 pin, VCO0 is forced LOW during an "out-of-lock" indication.

Register C is: PCG2, PCG1, sets the gain of the phase comparator.
preset + 2 dB
00 –6 dB
01 –2 dB
10 +2 dB
11 +6 dB
MD16, MSB of the main division ratio.

Register D is: MD15 to MD8, division ratio bit 15 to 8.

Register E is: MD7 to MD0, division ratio bit 7 to 0. Preset 80000.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage ranges				
digital + 5 V	V_P	4.5	5.5	V
analog + 5 to + 15 V	V_{P1}	4.5	16.5	V
analog + 5 V	V_{P2}	4.5	5.5	V
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	−40	+ 125	°C
Total power dissipation				
V_P = 5 V	P_{tot}	–	70	mW
power down	P_{tot}	–	16	mW

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 5 V; V_{P1} = 15 V; V_{P2} = 5 V; unless otherwise specified

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
SUPPLY						
Supply voltage ranges						
digital + 5 V		V_P	4.5	5	5.5	V
analog + 5 to + 15 V		V_{P1}	4.5	–	16.5	V
analog + 5 V		V_{P2}	4.5	5	5.5	V
Supply current ranges						
digital + 5 V		I_P	–	13.5	19	mA
analog + 5 to + 15 V		I_{P1}	–	1.0	1.5	mA
analog + 5 V		I_{P2}	–	1.0	1.5	mA
Power down + 5 V		I_{pd}	–	3.5	4.5	mA
MAIN DIVIDER						
Division ratio			1024	–	131071	
RF input (RFI)						
Frequency range		f_{RFI}	20	–	600	MHz
Input voltage level (RMS value)	Fig.3	$V_{i(rms)}$	50	–	150	mV
Input impedance	note 1					
shunt resistance	f_{RFI} = 100 MHz	R_S	–	1100	–	Ω
	f_{RFI} = 600 MHz	R_S	–	320	–	Ω
shunt capacitance	f_{RFI} = 100 MHz	C_S	–	1.8	–	pF
	f_{RFI} = 600 MHz	C_S	–	1.8	–	pF

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
MAIN CONTROL						
Serial clock input (SCL)						
Serial data input (SDA)						
Clock frequency		f_{CLK}	0	–	100	kHz
Input voltage HIGH		V_{IH}	3	–	–	V
Input voltage LOW		V_{IL}	–	–	1.0	V
Input current HIGH		I_{IH}	–	0.1	3.0	μA
Input current LOW		I_{IL}	−3	−1	–	μA
Input capacitance		C_I	–	20	–	pF
SDA sink current	V_{OL} = 0.4 V	I_{OL}	–	–	3	mA
Slave address select input (SA1)	note 2					
Input voltage HIGH		V_{IH}	3	–	–	V
Input voltage LOW		V_{IL}	–	–	0.4	V
Input current HIGH		I_{IH}	–	–	0.2	μA
Input current LOW		I_{IL}	−3.0	−1.5	–	μA
Oscillator buffer switch output 0 (VCO0)	note 3					
Output voltage LOW		V_{OL}	–	–	0.2	V
Sink current LOW		I_{OL}	–	–	400	μA
Oscillator buffer switch output 1 (VCO1)						
Output voltage LOW		V_{OL}	–	–	0.2	V
Sink current LOW		I_{OL}	–	–	400	μA
Inverting hardware power down input ($\overline{HPD}$)	note 2					
Input voltage HIGH		V_{IH}	3	–	–	V
Input voltage LOW		V_{IL}	–	–	0.4	V
Input current HIGH		I_{IH}	–	0.1	0.3	μA
Input current LOW		I_{IL}	−15	−8	–	μA
Synthesizer alarm (SYA)	note 4					
Output voltage LOW		V_{OL}	–	–	0.2	V
Output current LOW		I_{OL}	–	–	400	μA

parameter	conditions	symbol	min.	typ.	max.	unit
OSCILLATOR						
Reference input 1 (RI1)						
Frequency range	crystal	f_{ref1}	3	–	16	MHz
	TCXO	f_{ref1}	1	–	16	MHz
Input level (RMS level)	sinewave	$V_{ref1(rms)}$	0.1	–	2	V
Input level (peak-to-peak value)	square wave	$V_{ref1(p-p)}$	0.3	–	5	V
Reference input 2 (RI2)	note 5					
Frequency range						
	crystal	f_{ref2}	3	–	16	MHz
	TCXO	f_{ref2}	1	–	16	MHz
Output impedance		Z_o	–	2	–	kΩ
REFERENCE DIVIDER						
Division ratio			128	–	1920	
Input frequency range		f_i	1	–	16	MHz
Output frequency range		f_o	5	–	50	kHz
Output reference prescaler (FX8)	note 6					
Voltage output LOW		V_{OL}	–	–	0.5	V
Sink current LOW		I_{OL}	–	–	1.5	mA

DEVELOPMENT DATA

CHARACTERISTICS (continued)

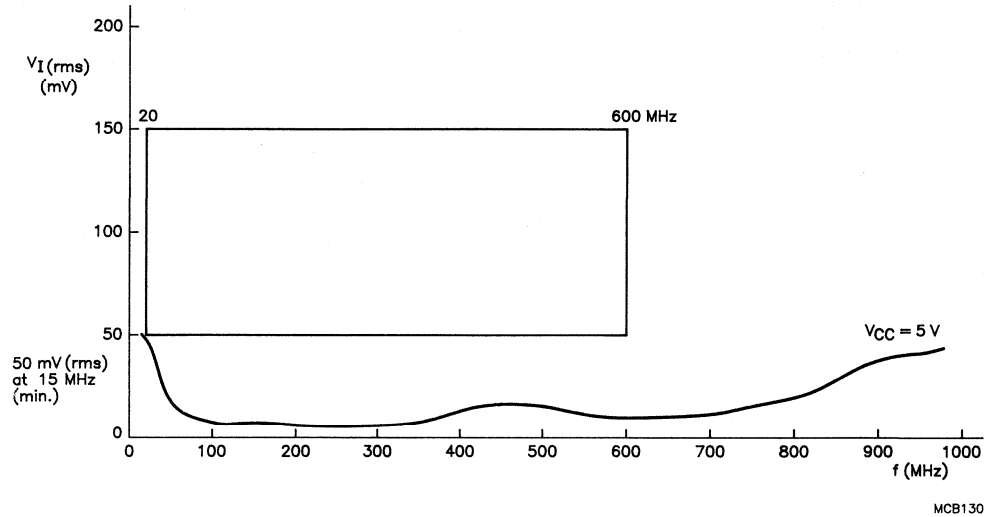
parameter	conditions	symbol	min.	typ.	max.	unit
PHASE COMPARATOR						
Frequency range		f	5	–	50	kHz
Digital phase comparator output (PCD)	note 7					
Output source current		I_O	–250	–300	–400	μA
Output sink current		I_O	250	300	400	μA
Output leakage current	V_{pcd} = 2.5 V	$\|I_{LO}\|$	–	1	70	nA
Phase comparator external sampling capacitor node (PCCS)	note 8					
Capacitance to ground		C_{pccs}	60	–	200	pF
Output leakage current	V_{pccs} = 2.5 V	$\|I_{LO}\|$	–	1	70	nA
Phase comparator external hold capacitor nodes 1 and 2 (PCCH1; PCCH2)						
Hold capacitor		C_{HOLD}	–	1	–	nF
Analog comparator output (PCA)						
Output source current		$-I_O$	–300	–	–	μA
Output sink current		I_O	–	–	300	μA
Output leakage current	V_{PCA} = 2.5 V	I_{LO}	–	–	250	nA
Gain	f_o = 6.24 kHz; C_{pccs} = 100 pF; PCG = + 2 dB	G_v	–	387	–	V/rad
Output source/sink current	PCG = + 2 dB	I_{pccs}	330	380	430	μA
LOOP AMPLIFIER						
Mid-rail voltage; not buffered (MV1)						
AC decoupling		C_{MV1}	–	47	–	μF

parameter	conditions	symbol	min.	typ.	max.	unit
Non-inverting high voltage amplifier input (HVA+)	note 9					
AC decoupling		C_{HVA}	–	1	–	nF
Inverting high voltage amplifier input (HVA–)						
Input impedance	0 to 10 kHz	Z_i	–	1	–	MΩ
Input noise (0.3 to 3 kHz)		N_{af}	–	10	–	$nV/\sqrt{Hz}$
Bias current		I_B	–	15	–	nA
High voltage amplifier output (HVAO)						
Open loop voltage gain		G_{ol}	30	60	–	dB
Output voltage		V_O	2	–	$V_{P1}-0.4$	V
Unity gain bandwidth		$B_G = 1$	–	2	–	MHz
Open loop output resistance		R_O	–	70	–	kΩ
Output current		I_O	300	350	–	μA

DEVELOPMENT DATA

Notes to the characteristics

1. The input impedance is given as the parallel combination of shunt resistance and shunt capacitance.
2. When left open is HIGH.
3. During out-of-lock the VCO0 pin is forced LOW.
4. This pin is an open-collector output.
5. If a TCXO is used this pin is to remain open or be used as a reference frequency output.
6. This pin is an open-collector output of the reference frequency divided by eight.
7. This pin is active when out-of-lock is indicated and will be 3-state when analog phase comparator takes over after the in-lock indication.
8. The capacitor on this pin fixes the gain of the analog phase comparator.
9. This pin is connected internally, via a buffer, to MVI.



▭ Operation of the device is guaranteed for input levels in this region over the full operating voltage and temperature range.

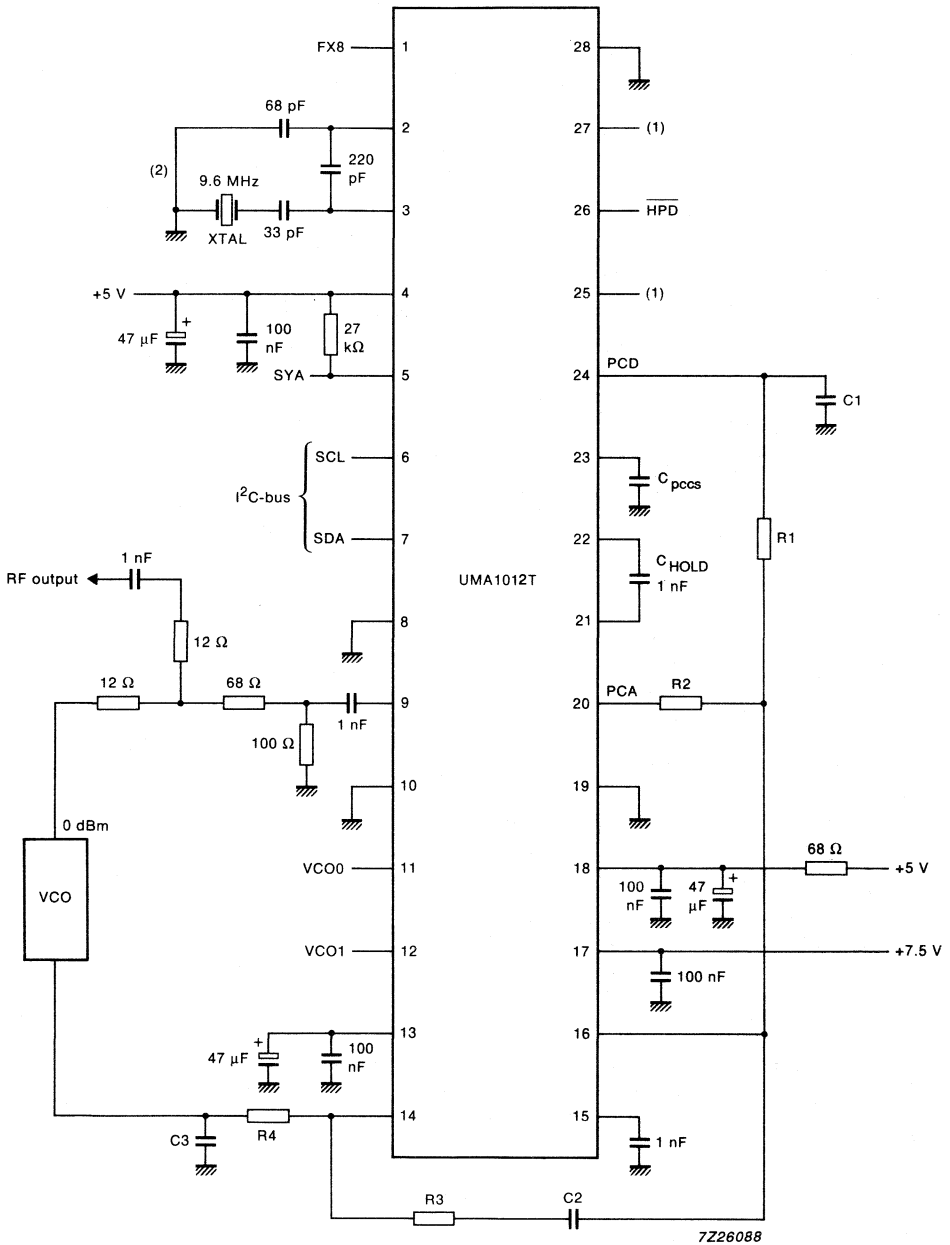
— Typical measurement at V_P = 5 V, T_{amb} = 25 °C.

Fig.3 Input sensitivity.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

DEVELOPMENT DATA

APPLICATION INFORMATION



(1) Not to be connected.

(2) Application using a temperature compensated oscillator (TXCO), pin 3 should be connected only to TXCO and pin 2 left open-circuit.

Fig.4 Synthesizer application.

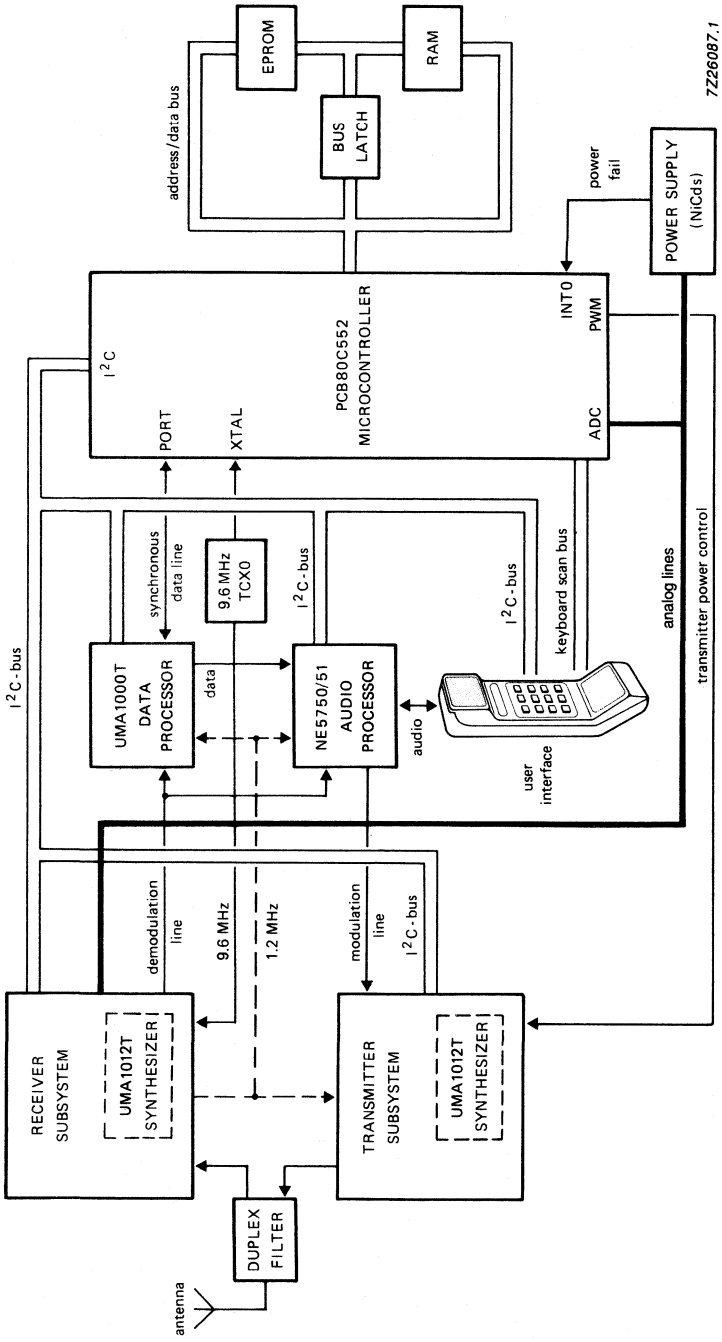


Fig.5 Cellular radio system schematic.

The UM1012T is a member of our Cellular Radio chipset, based on the I²C-bus, which meets the key requirements of a hand-held portable cellular set:

- small physical size
- minimum number of interconnections (serial bus)
- low power consumption
- low cost

DIGITAL PHASE-LOCKED-LOOP FILTER

FEATURES

- **Digital design avoids analog compensation errors**
- **Easily cascadable for higher order loops**
- **Useful frequency range: DC to 55 MHz typical (K-clock) DC to 35 MHz typical (I/D-clock)**
- **Dynamically variable bandwidth**
- **Very narrow bandwidth attainable**
- **Power-on reset**
- **Output capability: standard/bus driver**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT297 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT297 are designed to provide a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. These devices contain all the necessary circuits, with the exception of the divide-by-n counter, to build first order phase-locked-loops.

Both EXCLUSIVE-OR (XORPD) and edge-controlled (ECPD) phase detectors are provided for maximum flexibility. The input signals for the EXCLUSIVE-OR phase detector must have a 50% duty factor to obtain the maximum lock-range.

Proper partioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation (see Fig. 7) or to cascade to higher order phase-locked-loops.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay I/D_{CP} to I/D_{OUT} $\phi A_1, \phi B$ to $XORPD_{OUT}$ $\phi B, \phi A_2$ to $ECPD_{OUT}$	C_L = 15 pF V_{CC} = 5 V	15 13 19	18 13 19	ns
f_{max}	maximum clock frequency K_{CP} I/D_{CP}		63 41	68 40	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	18	19	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38CP).

16-lead mini-pack; plastic (SO16L; SOT162A).

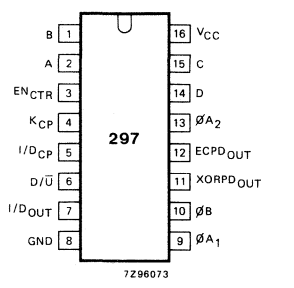


Fig. 1 Pin configuration.

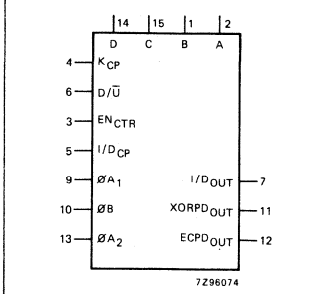


Fig. 2 Logic symbol.

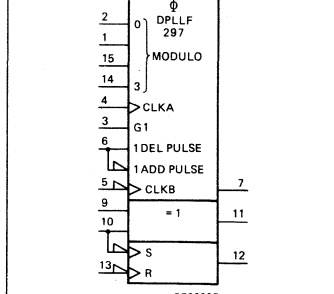


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 1, 15, 14	A, B, C, D	modulo control inputs
3	EN_{CTR}	K-counter enable input
4	K_{CP}	K-counter clock input (LOW-to-HIGH, edge-triggered)
5	I/D_{CP}	increment/decrement clock input (HIGH-to-LOW, edge-triggered)
6	$D/\overline{U}$	down/up control
7	I/D_{OUT}	increment/decrement bus output
8	GND	ground (0 V)
9, 10, 13	ϕA_1, ϕB, ϕA_2	phase inputs
11	$XORPD_{OUT}$	EXCLUSIVE-OR phase detector output
12	$ECPD_{OUT}$	edge-controlled phase detector output
16	V_{CC}	positive supply voltage

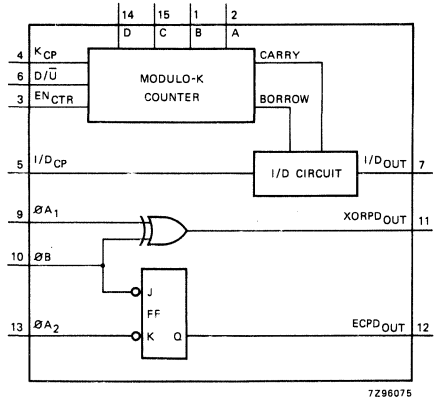


Fig. 4 Functional diagram.

K-COUNTER (DIGITAL CONTROL) FUNCTION TABLE

D	C	B	A	MODULO (K)
L	L	L	L	inhibited
L	L	L	H	2^3
L	L	H	L	2^4
L	L	H	H	2^5
L	H	L	L	2^6
L	H	L	H	2^7
L	H	H	L	2^8
L	H	H	H	2^9
H	L	L	L	2^{10}
H	L	L	H	2^{11}
H	L	H	L	2^{12}
H	L	H	H	2^{13}
H	H	L	L	2^{14}
H	H	L	H	2^{15}
H	H	H	L	2^{16}
H	H	H	H	2^{17}

EXCLUSIVE-OR PHASE DETECTOR FUNCTION TABLE

ϕA_1	ϕB	$XORPD_{OUT}$
L	L	L
L	H	H
H	L	H
H	H	L

EDGE-CONTROLLED PHASE DETECTOR TABLE

ϕA_2	ϕB	$ECPD_{OUT}$
H or L	↓	H
↓	H or L	L
H or L	↑	no change
↑	H or L	no change

H = HIGH voltage level
L = LOW voltage level
↓ = HIGH-to-LOW transition
↑ = LOW-to-HIGH transition

GENERAL DESCRIPTION

The length of the up/down K-counter is digitally programmable according to the K-counter function table. With, A, B, C and D all LOW, the K-counter is disabled. With A HIGH and B, C and D LOW, the K-counter is only three stages long, which widens the bandwidth or capture range and shortens the lock time of the loop. When A, B, C and D are all programmed HIGH, the K-counter becomes seventeen stages long, which narrows the bandwidth or capture range and lengthens the lock time. Real-time control of loop bandwith by manipulating the A to D inputs can maximize the overall performance of the digital phase-locked loop.

The "297" can perform the classic first-order phase-locked-loop function without using analog components. The accuracy of the digital phase-locked-loop (DPLL) is not affected by V_{CC} and temperature variations but depends solely on accuracies of the K-clock, I/D-clock and loop propagation delays.

The phase detector generates an error signal waveform that, at zero phase error, is a 50% duty factor square wave. At the limits of linear operation, the phase detector output will be either HIGH or LOW all of the time depending on the direction of the phase error ($\phi_{IN} - \phi_{OUT}$). Within these limits the phase detector output varies linearly with the input phase

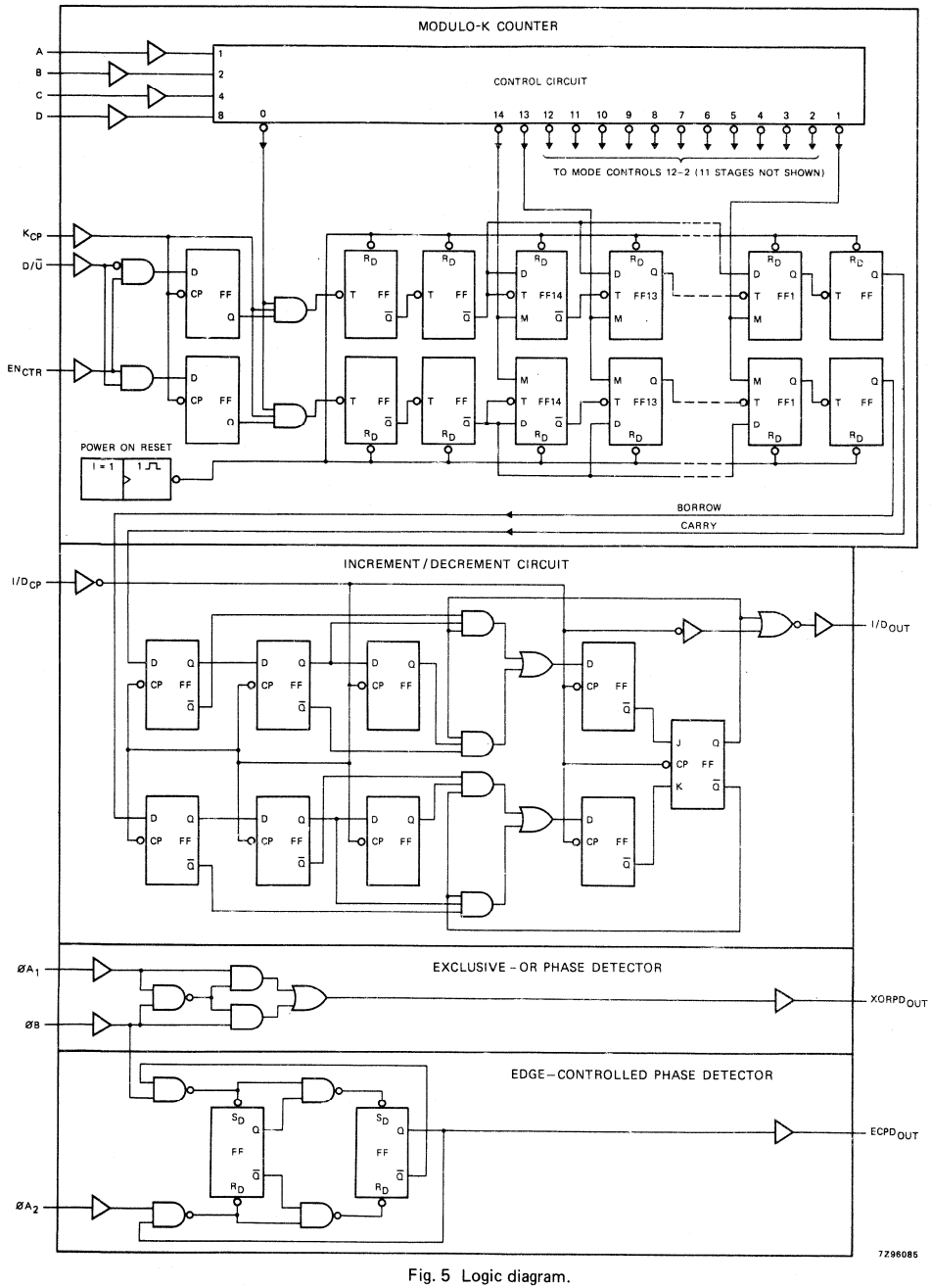


Fig. 5 Logic diagram.

GENERAL DESCRIPTION

error according to the gain k_d, which is expressed in terms of phase detector output per cycle or phase error. The phase detector output can be defined to vary between ± 1 according to the relation:

$$\text{phase detector output} = \frac{\%\,\text{HIGH} - \%\,\text{LOW}}{100}.$$

The output of the phase detector will be $k_d\phi_e$, where the phase error $\phi_e = \phi_{IN} - \phi_{OUT}$.

EXCLUSIVE-OR phase detectors (XORPD) and edge-controlled phase detectors (ECPD) are commonly used digital types. The ECPD is more complex than the XORPD logic function but can be described generally as a circuit that changes states on one of the transitions of its inputs. The gain (k_d) for an XORPD is 4 because its output remains HIGH ($XORPD_{OUT}$ = 1) for a phase error of 1/4 cycle. Similarly, k_d for the ECPD is 2 since its output remains HIGH for a phase error of 1/2 cycle. The type of phase detector will determine the zero-phase-error point, i.e., the phase separation of the phase detector inputs for a ϕ_e defined to be zero. For the basic DPLL system of Fig. 6 ϕ_e = 0 when the phase detector output is a square wave.

The XORPD inputs are 1/4 cycle out-of-phase for zero phase error. For the ECPD, ϕ_e = 0 when the inputs are 1/2 cycle out-of-phase.

The phase detector output controls the up/down input to the K-counter. The counter is clocked by input frequency Mf_c, which is a multiple M of the loop centre frequency f_c. When the K-counter recycles up, it generates a carry pulse. Recycling while counting down generates a borrow pulse. If the carry and the borrow outputs are conceptually combined into one output that is positive for a carry and negative for a borrow, and if the K-counter is considered as a frequency divider with the ratio Mf_c/K, the output of the K-counter will equal the input frequency multiplied by the division ratio. Thus the output from the K-counter is $(k_d\phi_e Mf_c)/K$.

The carry and borrow pulses go to the increment/decrement (I/D) circuit which, in the absence of any carry or borrow pulses has an output that is 1/2 of the input clock (I/D_{CP}). The input clock is just a multiple, 2N, of the loop centre frequency. In response to a carry or borrow pulse, the I/D circuit will either add or delete a pulse at I/D_{OUT}. Thus the output of the I/D circuit will be $Nf_c + (k_d\phi_e Mf_c)/2K$.

The output of the N-counter (or the output of the phase-locked-loop) is thus: $f_o = f_c + (k_d\phi_e Mf_c)/2KN$.

If this result is compared to the equation for a first-order analog phase-locked-loop, the digital equivalent of the gain of the VCO is just $Mf_c/2KN$ or f_c/K for M = 2N.

Thus the simple first-order phase-locked-loop with an adjustable K-counter is the equivalent of an analog phase-locked-loop with a programmable VCO gain.

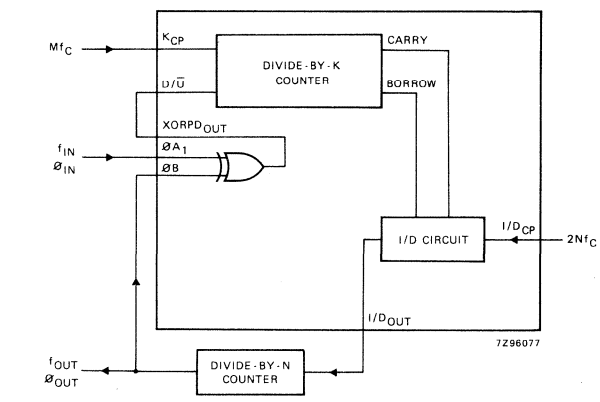


Fig. 6 DPLL using EXCLUSIVE-OR phase detection.

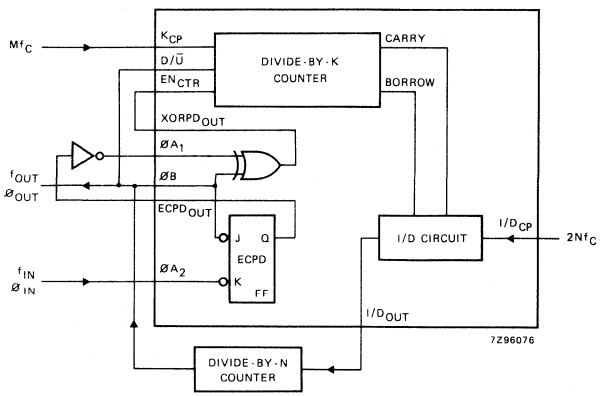


Fig. 7 DPLL using both phase detectors in a ripple-cancelation scheme.

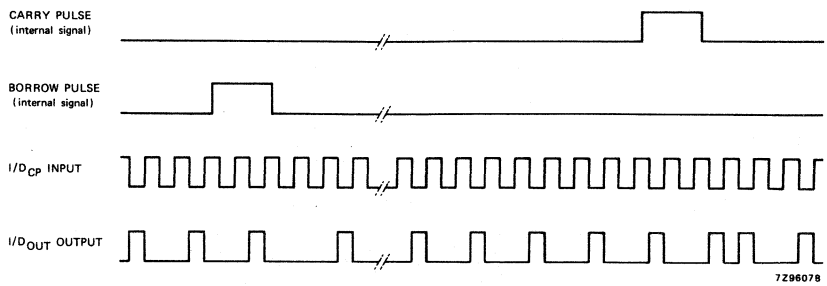


Fig. 8 Timing diagram: I/D$_{OUT}$ in-lock condition.

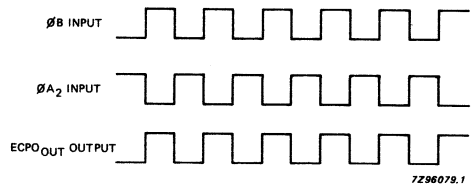


Fig. 9 Timing diagram: edge-controlled phase comparator waveforms.

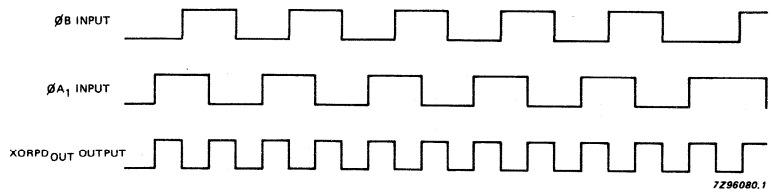


Fig. 10 Timing diagram: EXCLUSIVE-OR phase detector waveforms.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard/bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HC							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay I/D_{CP} to I/D_{OUT}		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 11
t_{PHL}/t_{PLH}	propagation delay ϕA_1, ϕB to $XORPD_{OUT}$		44 16 13	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 12
t_{PHL}/t_{PLH}	propagation delay ϕB, ϕA_2 to $ECPD_{OUT}$		61 22 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 13
t_{THL}/t_{TLH}	output transition time: bus driver output; I/D_{OUT} (pin 7)		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 11
t_{THL}/t_{TLH}	output transition time: standard outputs; $XORPD_{OUT}$, $ECPD_{OUT}$ (pins 11, 12)		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 12 and 13
t_W	clock pulse width K_{CP}	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 14
t_W	clock pulse width I/D_{CP}	100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time $D/\overline{U}$, EN_{CTR} to K_{CP}	120 24 20	33 12 10		150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig. 14
t_h	hold time $D/\overline{U}$, EN_{CTR} to K_{CP}	0 0 0	−19 −7 −6		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 14
f_{max}	maximum clock pulse frequency K_{CP}	6.0 30 35	19 57 68		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 14
f_{max}	maximum clock pulse frequency I/D_{CP}	4.0 20 24	12 37 44		3.2 16 19		2.6 13 15		MHz	2.0 4.5 6.0	Fig. 11

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard/bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
EN_{CTR}, $D/\overline{U}$	0.3
A, B, C, D, K_{CP}, ϕA_2	0.6
I/D_{CP}, ϕA_1, ϕB	1.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V, $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HCT							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay I/D_{CP} to I/D_{OUT}		21	35		44		53	ns	4.5	Fig. 11
t_{PHL}/t_{PLH}	propagation delay ϕA_1, ϕB to $XORPD_{OUT}$		16	32		40		48	ns	4.5	Fig. 12
t_{PHL}/t_{PLH}	propagation delay ϕB, ϕA_2 to $ECPD_{OUT}$		22	44		55		66	ns	4.5	Fig. 13
t_{THL}/t_{TLH}	output transition time bus driver output I/D_{OUT} (pin 7)		5	12		15		18	ns	4.5	Fig. 11
t_{THL}/t_{TLH}	output transition time standard outputs $XORPD_{OUT}$, $ECPD_{OUT}$ (pins 11, 12)		7	15		19		22	ns	4.5	Figs 12 and 13
t_W	clock pulse width K_{CP}	16	8		20		24		ns	4.5	Fig. 14
t_W	clock pulse width I/D_{CP}	25	13		31		38		ns	4.5	Fig. 11
t_{su}	set-up time $D/\overline{U}$, EN_{CTR} to K_{CP}	24	13		30		36		ns	4.5	Fig. 14
t_h	hold time $D/\overline{U}$, EN_{CTR} to K_{CP}	0	−8		0		0		ns	4.5	Fig. 14
f_{max}	maximum clock pulse frequency K_{CP}	30	62		24		20		MHz	4.5	Fig. 14
f_{max}	maximum clock pulse frequency I/D_{CP}	20	36		16		13		MHz	4.5	Fig. 11

AC WAVEFORMS

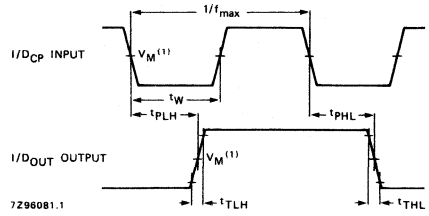


Fig. 11 Waveforms showing the clock (I/D_{CP}) to output (I/D_{OUT}) propagation delays, the clock pulse width, output transition times and maximum clock pulse frequency.

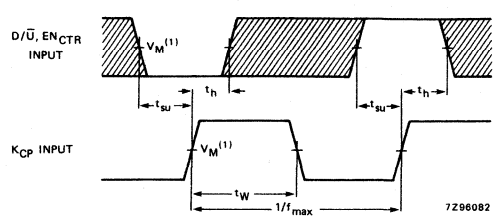


Fig. 14 Waveforms showing the clock (K_{CP}) pulse width and the maximum clock pulse frequency, and the input ($D/\overline{U}$, EN_{CTR}) to clock (K_{CP}) set-up and hold times.

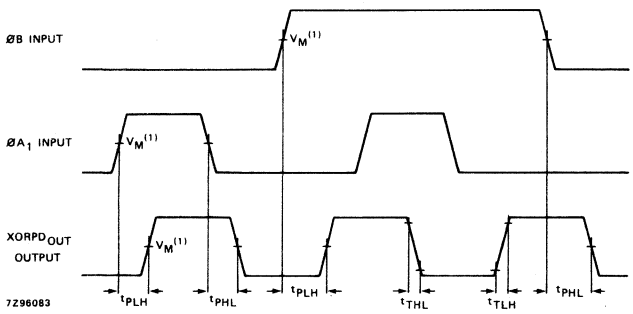


Fig. 12 Waveforms showing the phase input (ϕB, ϕA_1) to output ($XORPD_{OUT}$) propagation delays and output transition times.

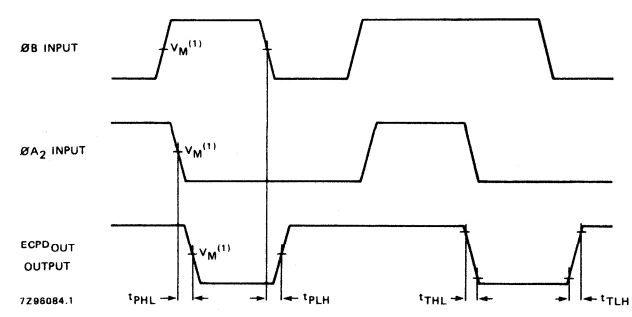


Fig. 13 Waveforms showing the phase input (ϕB, ϕA_2) to output ($ECPD_{OUT}$) propagation delays and output transition times.

Note to Fig. 14

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

PHASE-LOCKED-LOOP WITH VCO

FEATURES

- **Low power consumption**
- **Centre frequency of up to 17 MHz (typ.) at V_{CC} = 4.5 V**
- **Choice of three phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop; edge-triggered RS flip-flop**
- **Excellent VCO frequency linearity**
- **VCO-inhibit control for ON/OFF keying and for low standby power consumption**
- **Minimal frequency drift**
- **Operating power supply voltage range: VCO section 3.0 to 6.0 V digital section 2.0 to 6.0 V**
- **Zero voltage offset due to op-amp buffering**
- **Output capability: standard**
- **I_{CC} category: MSI**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
f_o	VCO centre frequency	C1 = 40 pF R1 = 3 kΩ V_{CC} = 5 V	19	19	MHz
C_I	input capacitance (pin 5)		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	24	24	pF

GND = 0 V; T_{amb} = 25 °C

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. Applies to the phase comparator section only (VCO disabled). For power dissipation of the VCO and demodulator sections see Figs 22, 23 and 24.

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38CP).
16-lead mini-pack; plastic (SO16; SOT109A).

GENERAL DESCRIPTION

The 74HC/HCT4046A are high-speed Si-gate CMOS devices and are pin compatible with the "4046" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4046A are phase-locked-loop circuits that comprise a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2 and PC3) with a common signal input amplifier and a common comparator input.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the "4046A" forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

(continued on next page)

APPLICATIONS

- **FM modulation and demodulation**
- **Frequency synthesis and multiplication**
- **Frequency discrimination**
- **Tone decoding**
- **Data synchronization and conditioning**
- **Voltage-to-frequency conversion**
- **Motor-speed control**

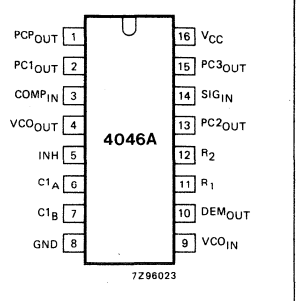


Fig. 1 Pin configuration.

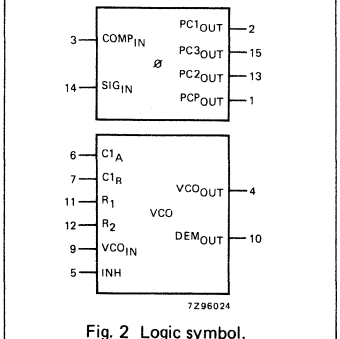


Fig. 2 Logic symbol.

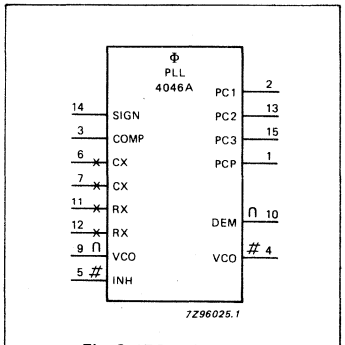


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PCP_{OUT}	phase comparator pulse output
2	$PC1_{OUT}$	phase comparator 1 output
3	$COMP_{IN}$	comparator input
4	VCO_{OUT}	VCO output
5	INH	inhibit input
6	$C1_A$	capacitor C1 connection A
7	$C1_B$	capacitor C1 connection B
8	GND	ground (0 V)
9	VCO_{IN}	VCO input
10	DEM_{OUT}	demodulator output
11	R_1	resistor R1 connection
12	R_2	resistor R2 connection
13	$PC2_{OUT}$	phase comparator 2 output
14	SIG_{IN}	signal input
15	$PC3_{OUT}$	phase comparator 3 output
16	V_{CC}	positive supply voltage

GENERAL DESCRIPTION (Cont'd)

VCO

The VCO requires one external capacitor C1 (between $C1_A$ and $C1_B$) and one external resistor R1 (between R_1 and GND) or two external resistors R1 and R2 (between R_1 and GND, and R_2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required.

The high input impedance of the VCO simplifies the design of low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin 10 (DEM_{OUT}). In contrast to conventional techniques where the DEM_{OUT} voltage is one threshold voltage lower than the VCO input voltage, here the DEM_{OUT} voltage equals that of the VCO input. If DEM_{OUT} is used, a load resistor (R_S) should be connected from DEM_{OUT} to GND; if unused, DEM_{OUT} should be left open. The VCO output (VCO_{OUT}) can be connected directly to the comparator input ($COMP_{IN}$), or connected via a frequency-divider. The VCO output signal has a duty factor of 50% (maximum expected deviation 1%), if the VCO input is held at a constant DC level. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

The only difference between the HC and HCT versions is the input level specification of the INH input. This input disables the VCO section. The sections of the comparator are identical, so that there is no difference in the SIG_{IN} (pin 14) or $COMP_{IN}$ (pin 3) inputs between the HC and HCT versions.

Phase comparators

The signal input (SIG_{IN}) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

Phase comparator 1 (PC1)

This is an EXCLUSIVE-OR network. The signal and comparator input frequencies (f_i) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10;

$V_{DEMOUT} = V_{PC1OUT}$ (via low-pass filter).

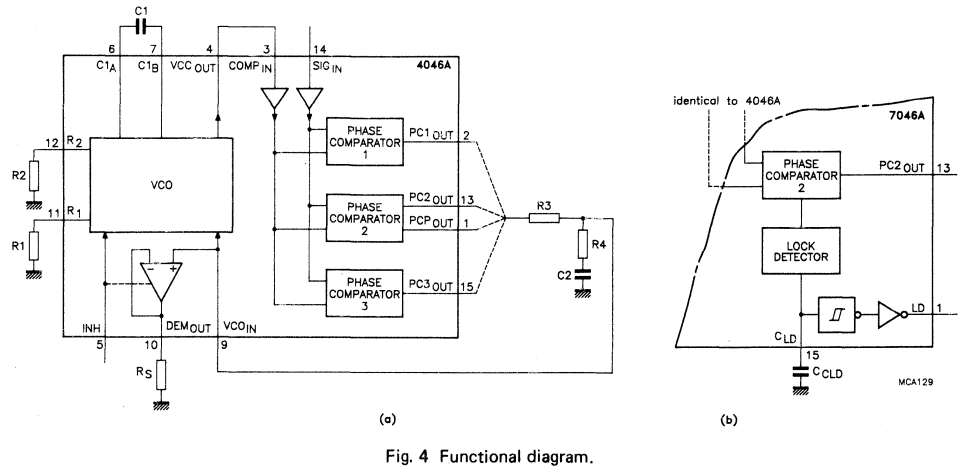


Fig. 4 Functional diagram.

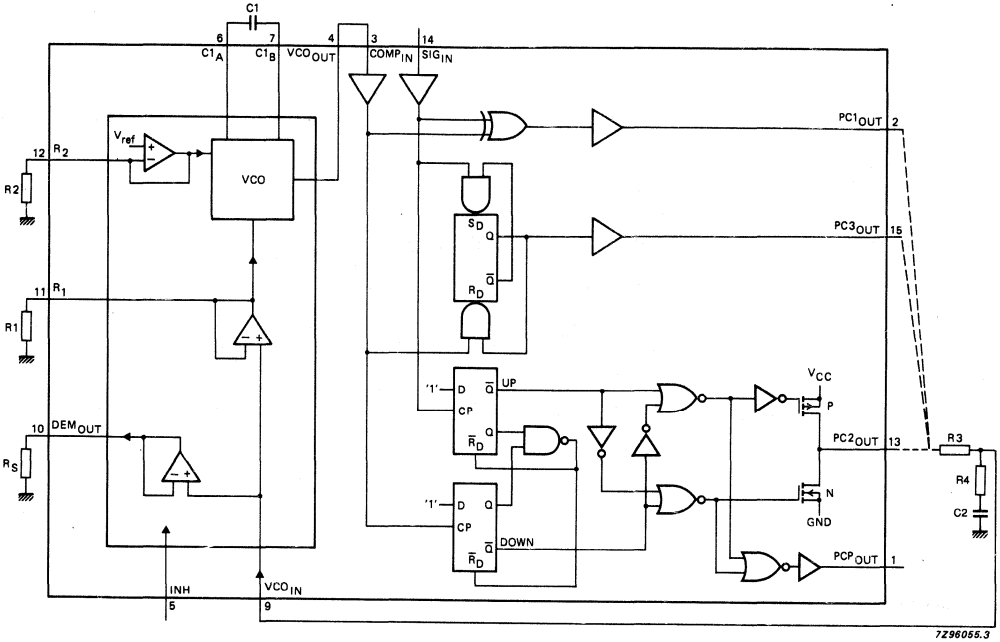


Fig. 5 Logic diagram.

The phase comparator gain is:

$K_p = \frac{V_{CC}}{\pi}$ (V/r).

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of signals (SIG_{IN}) and the comparator input ($COMP_{IN}$) as shown in Fig. 6. The average of V_{DEMOUT} is equal to 1/2 V_{CC} when there is no signal or noise at SIG_{IN} and with this input the VCO oscillates at the centre frequency (f_o). Typical waveforms for the PC1 loop locked at f_o are shown in Fig. 7.

The frequency capture range ($2f_c$) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2f_L$) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

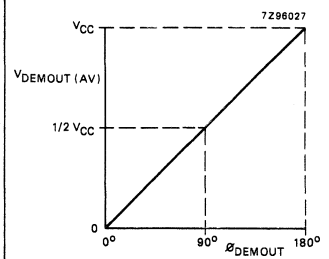


Fig. 6 Phase comparator 1: average output voltage versus input phase difference:

$V_{DEMOUT} = V_{PC1OUT} =$

$\frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

$\phi DEMOUT = (\phi SIGIN - \phi COMPIN)$.

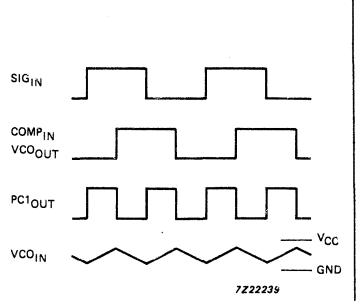


Fig. 7 Typical waveforms for PLL using phase comparator 1, loop locked at f_o.

GENERAL DESCRIPTION (Cont'd)

Phase comparators (Cont'd)

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration retains lock even with very noisy input signals. Typical behaviour of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO centre frequency.

Phase comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. PC2 comprises two D-type flip-flops, control-gating and a 3-state output stage. The circuit functions as an up-down counter (Fig. 5) where SIG_{IN} causes an up-count and $COMP_{IN}$ a down-count. The transfer function of PC2, assuming ripple ($f_r = f_i$) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{4\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10;
$V_{DEMOUT} = V_{PC2OUT}$ (via low-pass filter).

The phase comparator gain is:

$$K_p = \frac{V_{CC}}{4\pi} \text{ (V/r)}.$$

V_{DEMOUT} is the resultant of the initial phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Fig. 8. Typical waveforms for the PC2 loop locked at f_o are shown in Fig. 9.

When the frequencies of SIG_{IN} and $COMP_{IN}$ are equal but the phase of SIG_{IN} leads that of $COMP_{IN}$, the p-type output driver at $PC2_{OUT}$ is held "ON" for a time corresponding to the phase difference (ϕ_{DEMOUT}). When the phase of SIG_{IN} lags that of $COMP_{IN}$, the n-type driver is held "ON".

When the frequency of SIG_{IN} is higher than that of $COMP_{IN}$, the p-type output driver is held "ON" for most of the input signal cycle time, and for the remainder of the cycle both n and p- type drivers are "OFF" (3-state). If the SIG_{IN} frequency is lower than the $COMP_{IN}$ frequency, then it is the n-type driver that is held "ON" for most of the cycle. Subsequently, the voltage at the capacitor (C2) of the low-pass filter connected to $PC2_{OUT}$ varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance. Also in this condition, the signal at the phase comparator pulse output (PCP_{OUT}) is a HIGH level and so can be used for indicating a locked condition.

Thus, for PC2, no phase difference exists between SIG_{IN} and $COMP_{IN}$ over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both p and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG_{IN} the VCO adjusts, via PC2, to its lowest frequency.

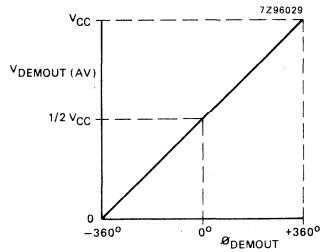


Fig. 8 Phase comparator 2: average output voltage versus input phase difference:
$V_{DEMOUT} = V_{PC2OUT} =$
$\frac{V_{CC}}{4\pi}(\phi_{SIGIN} - \phi_{COMPIN})$
$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$.

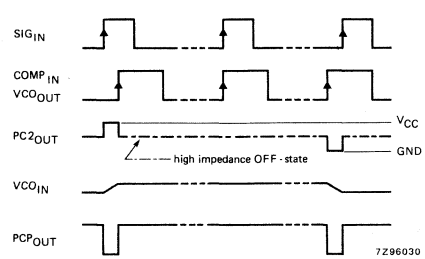


Fig. 9 Typical waveforms for PLL using phase comparator 2, loop locked at f_o.

Phase comparator 3 (PC3)

This is a positive edge-triggered sequential phase detector using an RS-type flip-flop. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. The transfer characteristic of PC3, assuming ripple ($f_r = f_i$) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{2\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10;
$V_{DEMOUT} = V_{PC3OUT}$ (via low-pass filter).

The phase comparator gain is:

$$K_p = \frac{V_{CC}}{2\pi} \text{ (V/r)}.$$

The average output from PC3, fed to the VCO via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Fig. 10. Typical waveforms for the PC3 loop locked at f_o are shown in Fig. 11.

The phase-to-output response characteristic of PC3 (Fig. 10) differs from that of PC2 in that the phase angle between SIG_{IN} and $COMP_{IN}$ varies between 0° and 360° and is 180° at the centre frequency. Also PC3 gives a greater voltage swing than PC2 for input phase differences but as a consequence the ripple content of the VCO input signal is higher. The PLL lock range for this type of phase comparator and the capture range are dependent on the low-pass filter. With no signal present at SIG_{IN} the VCO adjusts, via PC3, to its lowest frequency.

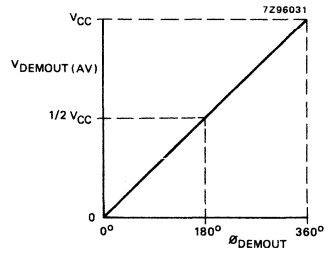


Fig. 10 Phase comparator 3: average output voltage versus input phase difference:
$V_{DEMOUT} = V_{PC3OUT} = \frac{V_{CC}}{2\pi}(\phi_{SIGIN} - \phi_{COMPIN})$
$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$.

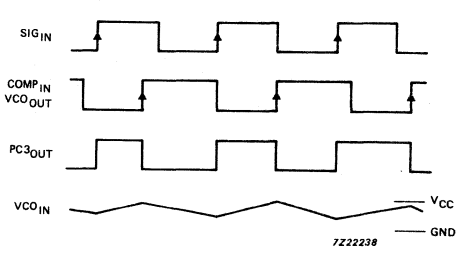


Fig. 11 Typical waveforms for PLL using phase comparator 3, loop locked at f_o.

RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	3.0	5.0	6.0	4.5	5.0	5.5	V	
V_{CC}	DC supply voltage if VCO section is not used	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times (pin 5)		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K

DC CHARACTERISTICS FOR 74HC

Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
I_{CC}	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μA	6.0	pins 3, 5, and 14 at V_{CC}; pin 9 at GND; I_I at pins 3 and 14 to be excluded

Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	DC coupled HIGH level input voltage SIG_{IN}, $COMP_{IN}$	1.5 3.15 4.2	1.2 2.4 3.2		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	DC coupled LOW level input voltage SIG_{IN}, $COMP_{IN}$		0.8 2.1 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage PCP_{OUT}, PC_{nOUT}	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage PCP_{OUT}, PC_{nOUT}	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage PCP_{OUT}, PC_{nOUT}		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage PCP_{OUT}, PC_{nOUT}		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current SIG_{IN}, $COMP_{IN}$			3.0 7.0 18.0 30.0		4.0 9.0 23.0 38.0		5.0 11.0 27.0 45.0	μA	2.0 3.0 4.5 6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current $PC2_{OUT}$			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
R_I	input resistance SIG_{IN}, $COMP_{IN}$		800 250 150						kΩ	3.0 4.5 6.0	V_I at self-bias operating point; $\Delta V_I = 0.5$ V; see Figs 12, 13 and 14	

DC CHARACTERISTICS FOR 74HC (Cont'd)

VCO section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage INH	2.1 3.15 4.2	1.7 2.4 3.2		2.1 3.15 4.2		2.1 3.15 4.2		V	3.0 4.5 6.0		
V_{IL}	LOW level input voltage INH		1.3 2.1 2.8	0.9 1.35 1.8		0.9 1.35 1.8		0.9 1.35 1.8	V	3.0 4.5 6.0		
V_{OH}	HIGH level output voltage VCO_{OUT}	2.9 4.4 5.9	3.0 4.5 6.0		2.9 4.4 5.9		2.9 4.4 5.9		V	3.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage VCO_{OUT}	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage VCO_{OUT}		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	3.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage VCO_{OUT}		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
V_{OL}	LOW level output voltage $C1_A$, $C1_B$ (test purposes only)			0.40 0.40		0.47 0.47		0.54 0.54	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current INH, VCO_{IN}			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
R1	resistor range	3.0 3.0 3.0		300 300 300					kΩ	3.0 4.5 6.0		note 1
R2	resistor range	3.0 3.0 3.0		300 300 300					kΩ	3.0 4.5 6.0		note 1
C1	capacitor range	40 40 40		no limit					pF	3.0 4.5 6.0		
V_{VCOIN}	operating voltage range at VCO_{IN}	1.1 1.1 1.1		1.9 3.4 5.9					V	3.0 4.5 6.0		over the range specified for R1; for linearity see Figs 20 and 21.

Note

1. The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/or R2 are/is > 10 kΩ.

Demodulator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
R_S	resistor range	50 50 50		300 300 300					kΩ	3.0 4.5 6.0	at $R_S > 300$ kΩ the leakage current can influence V_{DEMOUT}
V_{OFF}	offset voltage VCO_{IN} to V_{DEMOUT}		±30 ±20 ±10						mV	3.0 4.5 6.0	$V_I = V_{VCOIN} = 1/2\ V_{CC}$; values taken over R_S range; see Fig. 15
R_D	dynamic output resistance at DEM_{OUT}		25 25 25						Ω	3.0 4.5 6.0	$V_{DEMOUT} = 1/2\ V_{CC}$

AC CHARACTERISTICS FOR 74HC

Phase comparator section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC1_{OUT}$		63 23 18	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 16
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to PCP_{OUT}		96 35 28	340 68 58		425 85 72		510 102 87	ns	2.0 4.5 6.0	Fig. 16
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC3_{OUT}$		77 28 22	270 54 46		340 68 58		405 81 69	ns	2.0 4.5 6.0	Fig. 16
t_{PZH}/t_{PZL}	3-state output enable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		83 30 24	280 56 48		350 70 60		420 84 71	ns	2.0 4.5 6.0	Fig. 17
t_{PHZ}/t_{PLZ}	3-state output disable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		99 36 29	325 65 55		405 81 69		490 98 83	ns	2.0 4.5 6.0	Fig. 17
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 16
$V_{I(p-p)}$	AC coupled input sensitivity (peak-to-peak value) at SIG_{IN} or $COMP_{IN}$		9 11 15 33						mV	2.0 3.0 4.5 6.0	f_i = 1 MHz

VCO section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	typ.	max.	min.	max.			
$\Delta f/T$	frequency stability with temperature change				0.20 0.15 0.14				%/K	3.0 4.5 6.0	$V_I = V_{VCOIN}$ = 1/2 V_{CC}; R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Fig. 18
f_o	VCO centre frequency (duty factor = 50%)	3.0 11.0 13.0	10.0 17.0 21.0						MHz	3.0 4.5 6.0	V_{VCOIN} = 1/2 V_{CC}; R1 = 3 kΩ; R2 = ∞; C1 = 40 pF; see Fig. 19
Δf_{VCO}	VCO frequency linearity		1.0 0.4 0.3						%	3.0 4.5 6.0	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 20 and 21
δ_{VCO}	duty factor at VCO_{OUT}		50 50 50						%	3.0 4.5 6.0	

DC CHARACTERISTICS FOR 74HCT

Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT									
		+25			−40 to +85		−40 to +125			V_{CC} V	OTHER
		min.	typ.	max.	min.	max.	min.	max.			
I_{CC}	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μA	6.0	pins 3, 5 and 14 at V_{CC}; pin 9 at GND; I_I at pins 3 and 14 to be excluded
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1) $V_I = V_{CC} - 2.1$ V		100	360		450		490	μA	4.5 to 5.5	pins 3 and 14 at V_{CC}; pin 9 at GND; I_I at pins 3 and 14 to be excluded

Note

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given above.
   To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
INH	1.00

DC CHARACTERISTICS FOR 74HCT

Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	DC coupled HIGH level input voltage SIG_{IN}, $COMP_{IN}$	3.15	2.4						V	4.5		
V_{IL}	DC coupled LOW level input voltage SIG_{IN}, $COMP_{IN}$		2.1	1.35					V	4.5		
V_{OH}	HIGH level output voltage PCP_{OUT}, PC_{nOUT}	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage PCP_{OUT}, PC_{nOUT}	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage PCP_{OUT}, PC_{nOUT}		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage PCP_{OUT}, PC_{nOUT}		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current SIG_{IN}, $COMP_{IN}$			30		38		45	μA	5.5	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current $PC2_{OUT}$			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
R_I	input resistance SIG_{IN}, $COMP_{IN}$		250						kΩ	4.5	V_I at self-bias operating point; $\Delta V_I = 0.5$ V; see Figs 12, 13 and 14	

DC CHARACTERISTICS FOR 74HCT

VCO section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage INH	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage INH		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage VCO_{OUT}	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage VCO_{OUT}	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage VCO_{OUT}		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage VCO_{OUT}		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
V_{OL}	LOW level output voltage $C1_A$, $C1_B$ (test purposes only)			0.40		0.47		0.54	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current INH, VCO_{IN}			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
R1	resistor range	3.0		300					kΩ	4.5		note 1
R2	resistor range	3.0		300					kΩ	4.5		note 1
C1	capacitor range	40		no limit					pF	4.5		
V_{VCOIN}	operating voltage range at VCO_{IN}	1.1		3.4					V	4.5		over the range specified for R1; for linearity see Figs 20 and 21.

Note

1. The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/or R2 are/is > 10 kΩ.

DC CHARACTERISTICS FOR 74HCT

Demodulator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
R_S	resistor range	50		300					kΩ	4.5	at $R_S > 300$ kΩ the leakage current can influence V_{DEMOUT}
V_{OFF}	offset voltage VCO_{IN} to V_{DEMOUT}		±20						mV	4.5	$V_I = V_{VCOIN} = 1/2\ V_{CC}$; values taken over R_S range; see Fig. 15
R_D	dynamic output resistance at DEM_{OUT}		25						Ω	4.5	$V_{DEMOUT} = 1/2\ V_{CC}$

AC CHARACTERISTICS FOR 74HCT

Phase comparator section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC1_{OUT}$		23	40		50		60	ns	4.5	Fig. 16
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to PCP_{OUT}		35	68		85		102	ns	4.5	Fig. 16
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC3_{OUT}$		28	54		68		81	ns	4.5	Fig. 16
t_{PZH}/t_{PZL}	3-state output enable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		30	56		70		84	ns	4.5	Fig. 17
t_{PHZ}/t_{PLZ}	3-state output disable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		36	65		81		98	ns	4.5	Fig. 17
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 16
$V_{I\ (p-p)}$	AC coupled input sensitivity (peak-to-peak value) at SIG_{IN} or $COMP_{IN}$		15						mV	4.5	f_i = 1 MHz

VCO section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	typ.	max.	min.	max.			
$\Delta f/T$	frequency stability with temperature change				0.15				%/K	4.5	$V_I = V_{VCOIN}$ within recommended range; R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Fig. 18b
f_o	VCO centre frequency (duty factor = 50%)	11.0	17.0						MHz	4.5	V_{VCOIN} = 1/2 V_{CC}; R1 = 3 kΩ; R2 = ∞; C1 = 40 pF; see Fig. 19
Δf_{VCO}	VCO frequency linearity		0.4						%	4.5	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 20 and 21
δ_{VCO}	duty factor at VCO_{OUT}		50						%	4.5	

FIGURE REFERENCES FOR DC CHARACTERISTICS

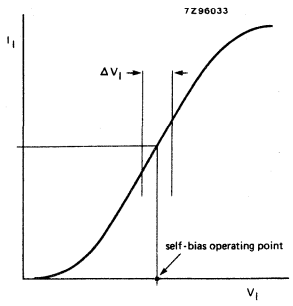


Fig. 12 Typical input resistance curve at SIG_{IN}, $COMP_{IN}$.

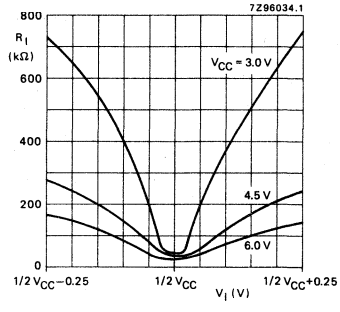


Fig. 13 Input resistance at SIG_{IN}, $COMP_{IN}$ with ΔV_I = 0.5 V at self-bias point.

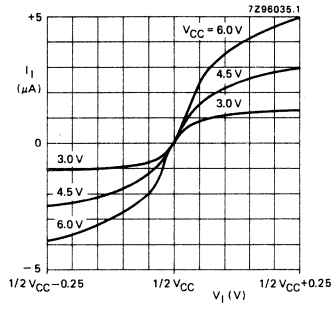
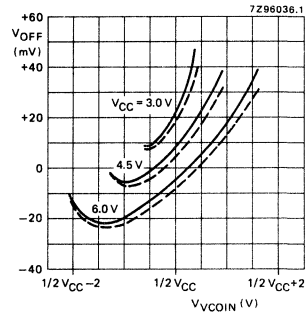


Fig. 14 Input current at SIG_{IN}, $COMP_{IN}$ with ΔV_I = 0.5 V at self-bias point.



— R_S = 50 kΩ
- - - R_S = 300 kΩ

Fig. 15 Offset voltage at demodulator output as a function of VCO_{IN} and R_S.

AC WAVEFORMS

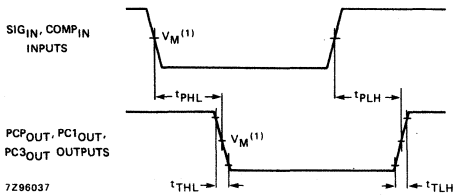


Fig. 16 Waveforms showing input (SIG_{IN}, $COMP_{IN}$) to output (PCP_{OUT}, $PC1_{OUT}$, $PC3_{OUT}$) propagation delays and the output transition times.

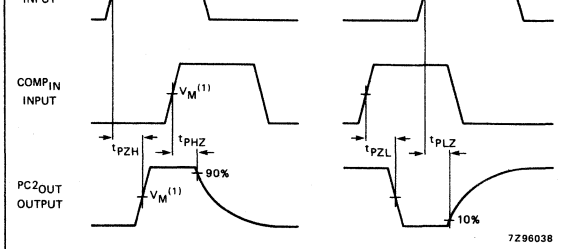


Fig. 17 Waveforms showing the 3-state enable and disable times for $PC2_{OUT}$.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.

AC WAVE FORMS (Continued)

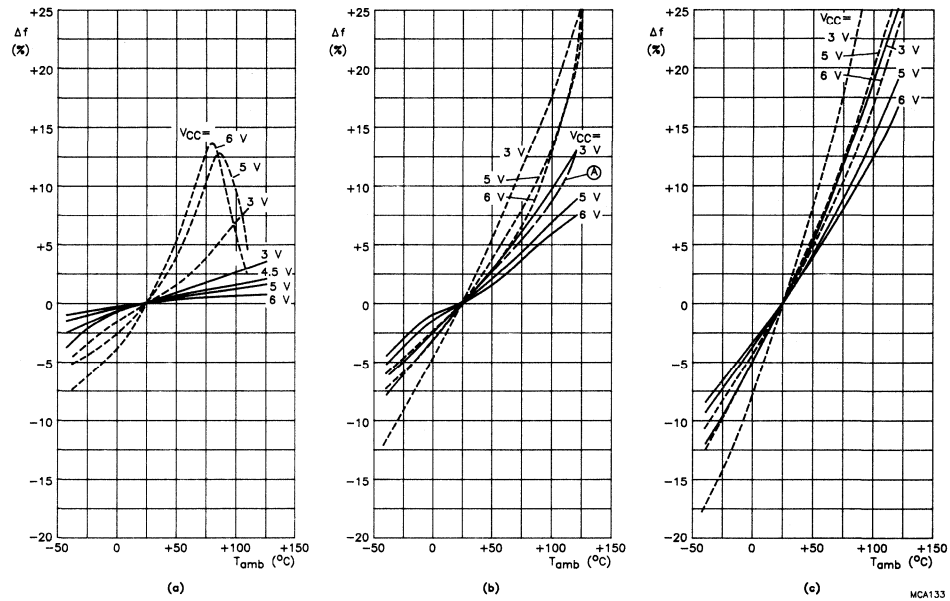
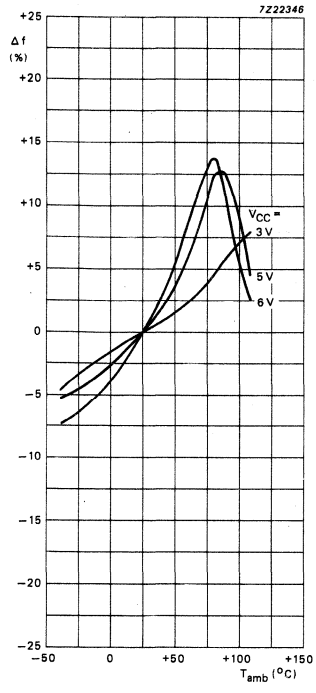
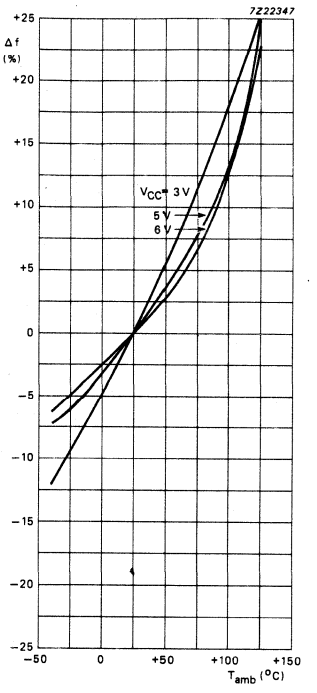


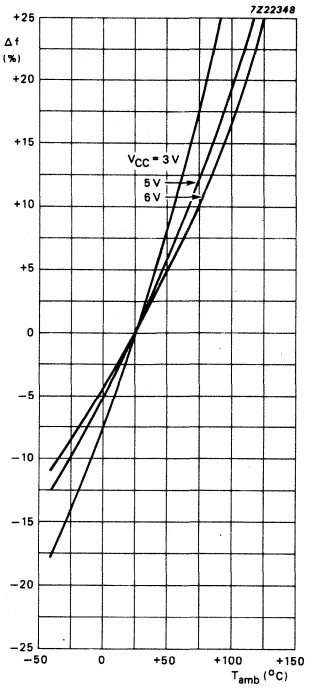
Fig.18 Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.
——— without offset (R2 = ∞): (a) R1 = 3 kΩ; (b) R1 = 10 kΩ; (c) R1 = 300 kΩ.
– – – with offset (R1 = ∞): (a) R2 = 3 kΩ; (b) R2 = 10 kΩ; (c) R2 = 300 kΩ.
In (b), the frequency stability for R1 = R2 = 10 kΩ at 5 V is also given (curve A). This curve is set by the total VCO bias current, and is not simply the addition of the two 10 kΩ stability cuves. C1 = 100 pF; $V_{VCO\ IN} = 0.5\ V_{CC}$.



(d) $R_2 = 3\ k\Omega$
$R_1 = \infty$



(e) $R_2 = 10\ k\Omega$
$R_1 = \infty$



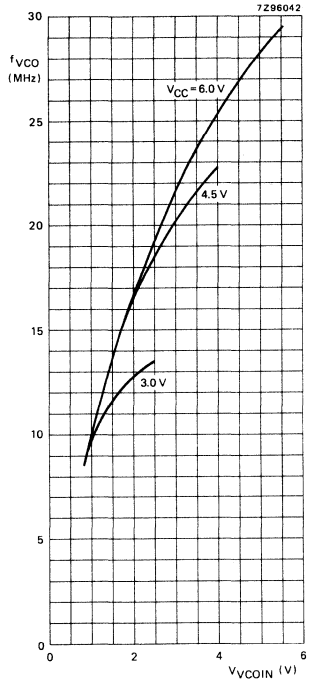
(f) $R_2 = 300\ k\Omega$
$R_1 = \infty$

Fig. 18 Continued.

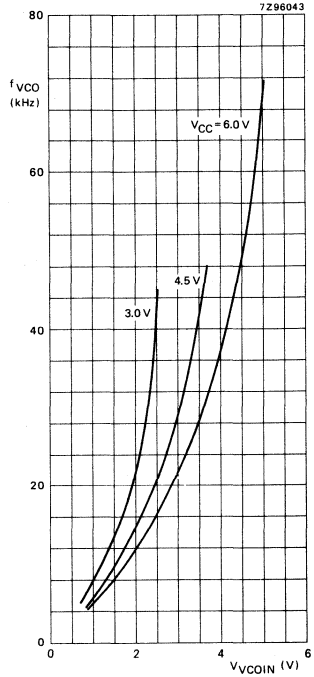
Note to Fig. 18

To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.

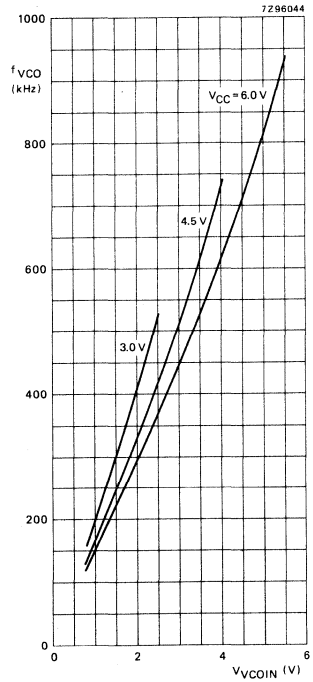
AC WAVEFORMS (Continued)



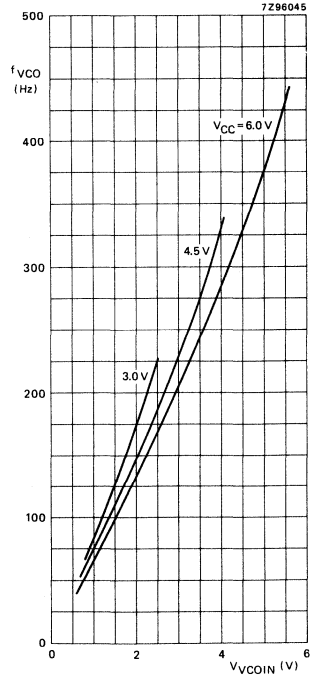
(a) R1 = 3 kΩ; C1 = 40 pF



(b) R1 = 3 kΩ; C1 = 100 nF



(c) R1 = 300 kΩ; C1 = 40 pF



(d) R1 = 300 kΩ; C1 = 100 nF

Fig. 19 Graphs showing VCO frequency (f_{VCO}) as a function of the VCO input voltage (V_{VCOIN}).

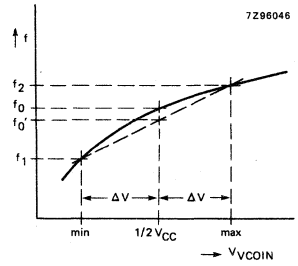


Fig. 20 Definition of VCO frequency linearity: $\Delta V = 0.5$ V over the V_{CC} range: for VCO linearity

$$f'_0 = \frac{f_1 + f_2}{2},$$

$$\text{linearity} = \frac{f'_0 - f_0}{f'_0} \times 100\%$$

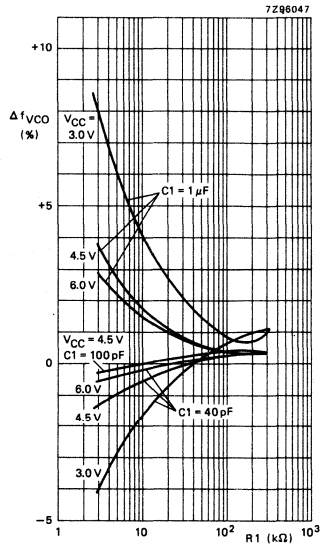
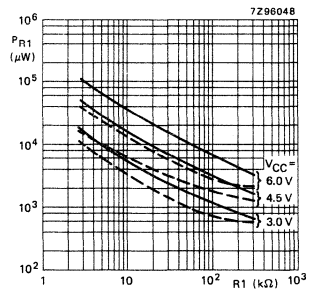
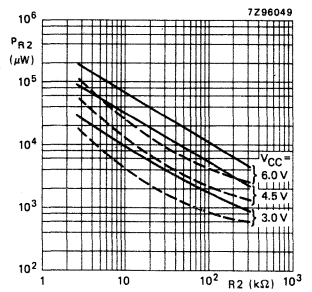


Fig. 21 Frequency linearity as a function of R1, C1 and V_{CC}: R2 = ∞ and $\Delta V = 0.5$ V.



— C1 = 40 pF
- - - C1 = 1 μF

Fig. 22 Power dissipation versus the value of R1: $C_L = 50$ pF; R2 = ∞; $V_{VCOIN} = 1/2\ V_{CC}$; $T_{amb} = 25$ °C.



— C1 = 40 pF
- - - C1 = 1 μF

Fig. 23 Power dissipation versus the value of R2: $C_L = 50$ pF; R1 = ∞; $V_{VCOIN} = GND = 0$ V; $T_{amb} = 25$ °C.

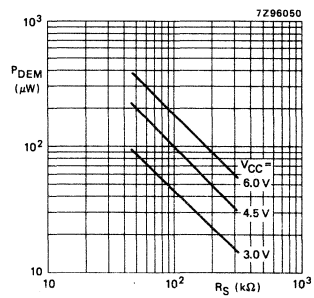


Fig. 24 Typical dc power dissipation of demodulator sections as a function of R_S: R1 = R2 = ∞; $T_{amb} = 25$ °C; $V_{VCOIN} = 1/2\ V_{CC}$.

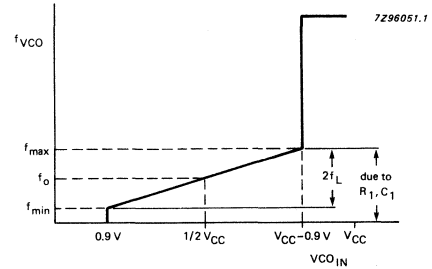
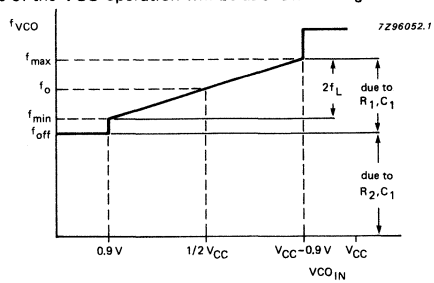
APPLICATION INFORMATION

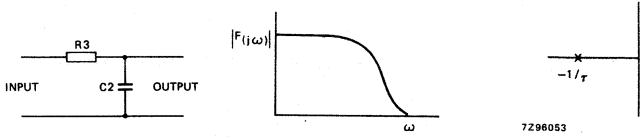
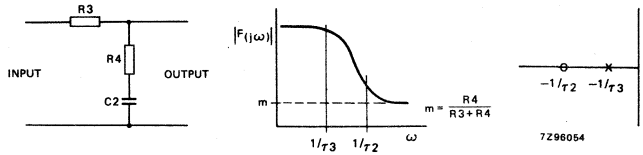
This information is a guide for the approximation of values of external components to be used with the 74HC/HCT4046A in a phase-lock-loop system.

References should be made to Figs 29, 30 and 31 as indicated in the table.

Values of the selected components should be within the following ranges:

R1 between 3 kΩ and 300 kΩ;
R2 between 3 kΩ and 300 kΩ;
R1 + R2 parallel value > 2.7 kΩ;
C1 greater than 40 pF.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
VCO frequency **without extra offset**	PC1, PC2 or PC3	**VCO frequency characteristic** With R2 = ∞ and R1 within the range 3 kΩ < R1 < 300 kΩ, the characteristics of the VCO operation will be as shown in Fig. 25. (Due to R1, C1 time constant a small offset remains when R2 = ∞.)  Fig. 25 Frequency characteristic of VCO operating without offset: f_o = centre frequency; $2f_L$ = frequency lock range.
	PC1	**Selection of R1 and C1** Given f_o, determine the values of R1 and C1 using Fig. 29.
	PC2 or PC3	Given f_{max} and f_o, determine the values of R1 and C1 using Fig. 29, use Fig. 31 to obtain $2f_L$ and then use this to calculate f_{min}.
VCO frequency **with extra offset**	PC1, PC2 or PC3	**VCO frequency characteristic** With R1 and R2 within the ranges 3 kΩ < R1 < 300 kΩ, 3 kΩ < R2 < 300 kΩ, the characteristics of the VCO operation will be as shown in Fig. 26.  Fig. 26 Frequency characteristic of VCO operating with offset: f_o = centre frequency; $2f_L$ = frequency lock range.
	PC1, PC2 or PC3	**Selection of R1, R2 and C1** Given f_o and f_L, determine the value of product R1C1 by using Fig. 31. Calculate f_{off} from the equation $f_{off} = f_o - 1.6f_L$. Obtain the values of C1 and R2 by using Fig. 30. Calculate the value of R1 from the value of C1 and the product R1C1.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
PLL conditions with no signal at the SIG_{IN} input	PC1	VCO adjusts to f_o with ϕ_{DEMOUT} = 90° and V_{VCOIN} = 1/2 V_{CC} (see Fig. 6).
	PC2	VCO adjusts to f_o with ϕ_{DEMOUT} = −360° and V_{VCOIN} = min. (see Fig. 8).
	PC3	VCO adjusts to f_o with ϕ_{DEMOUT} = −360° and V_{VCOIN} = min. (see Fig. 10).
PLL frequency capture range	PC1, PC2 or PC3	**Loop filter component selection**  (a) τ = R3 x C2 (b) amplitude characteristic (c) pole-zero diagram A small capture range ($2f_c$) is obtained if $2f_c \approx 1/\pi\ (\sqrt{2\pi f_L/\tau})$ Fig. 27 Simple loop filter for PLL **without** offset; R3 ⩾ 500 Ω.  (a) τ_1 = R3 x C2; τ_2 = R4 x C2; τ_3 = (R3 + R4) x C2 (b) amplitude characteristic (c) pole-zero diagram Fig. 28 Simple loop filter for PLL **with** offset; R3 + R4 ⩾ 500 Ω.
PLL locks on harmonics at centre frequency	PC1 or PC3	yes
	PC2	no
noise rejection at signal input	PC1	high
	PC2 or PC3	low
AC ripple content when PLL is locked	PC1	$f_r = 2f_i$, large ripple content at ϕ_{DEMOUT} = 90°
	PC2	$f_r = f_i$, small ripple content at ϕ_{DEMOUT} = 0°
	PC3	$f_r = f_i$, large ripple content at ϕ_{DEMOUT} = 180°

APPLICATION INFORMATION (Continued)

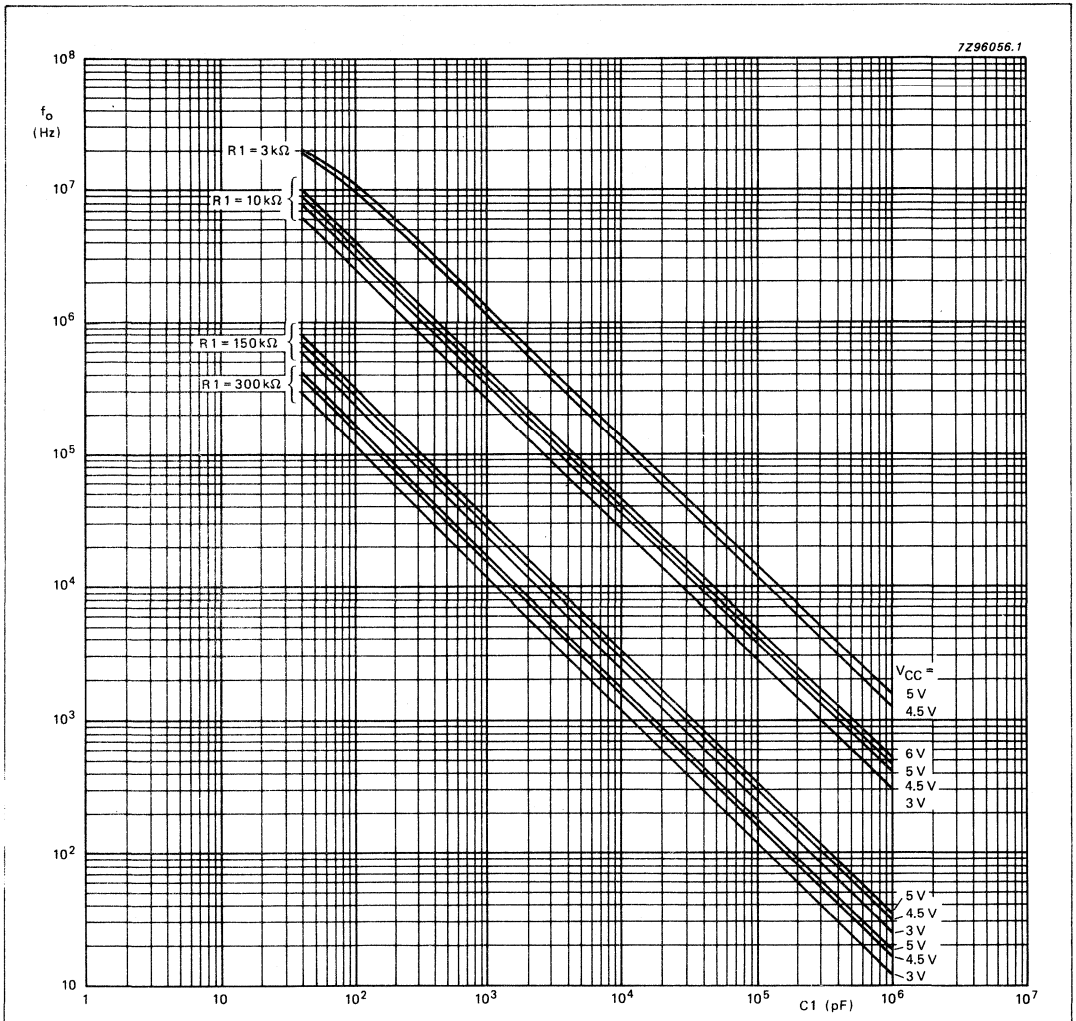


Fig. 29 Typical value of VCO centre frequency (f_o) as a function of C1: R2 = ∞; V_{VCOIN} = 1/2 V_{CC}; INH = GND; T_{amb} = 25 °C.

Notes to Fig. 29

1. To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.
2. Interpolation for various values of R1 can be easily calculated because, a constant R1C1 product will produce almost the same VCO output frequency.

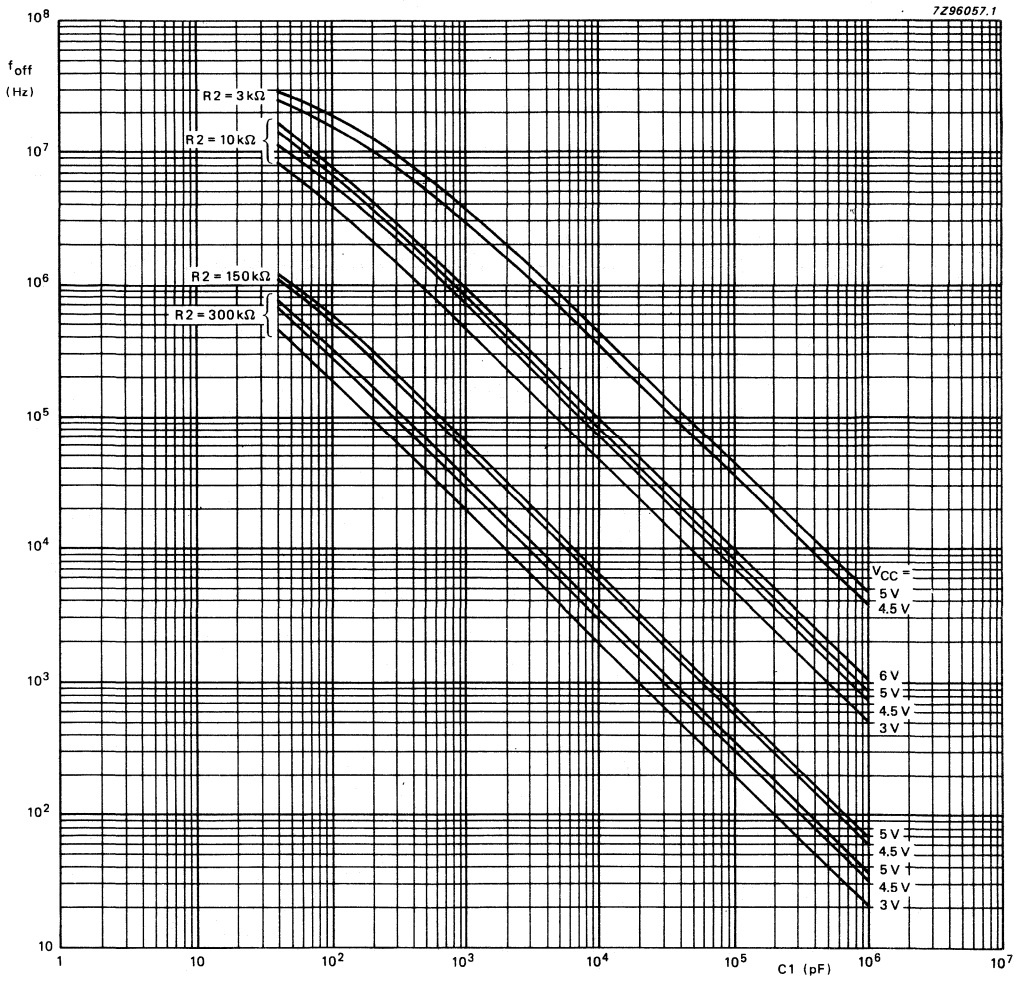


Fig. 30 Typical value of frequency offset as a function of C1: R1 = ∞; V_{VCOIN} = 1/2 V_{CC}; INH = GND; T_{amb} = 25 °C.

Notes to Fig. 30

1. To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.
2. Interpolation for various values of R2 can be easily calculated because, a constant R2C1 product will produce almost the same VCO output frequency.

APPLICATION INFORMATION (Continued)

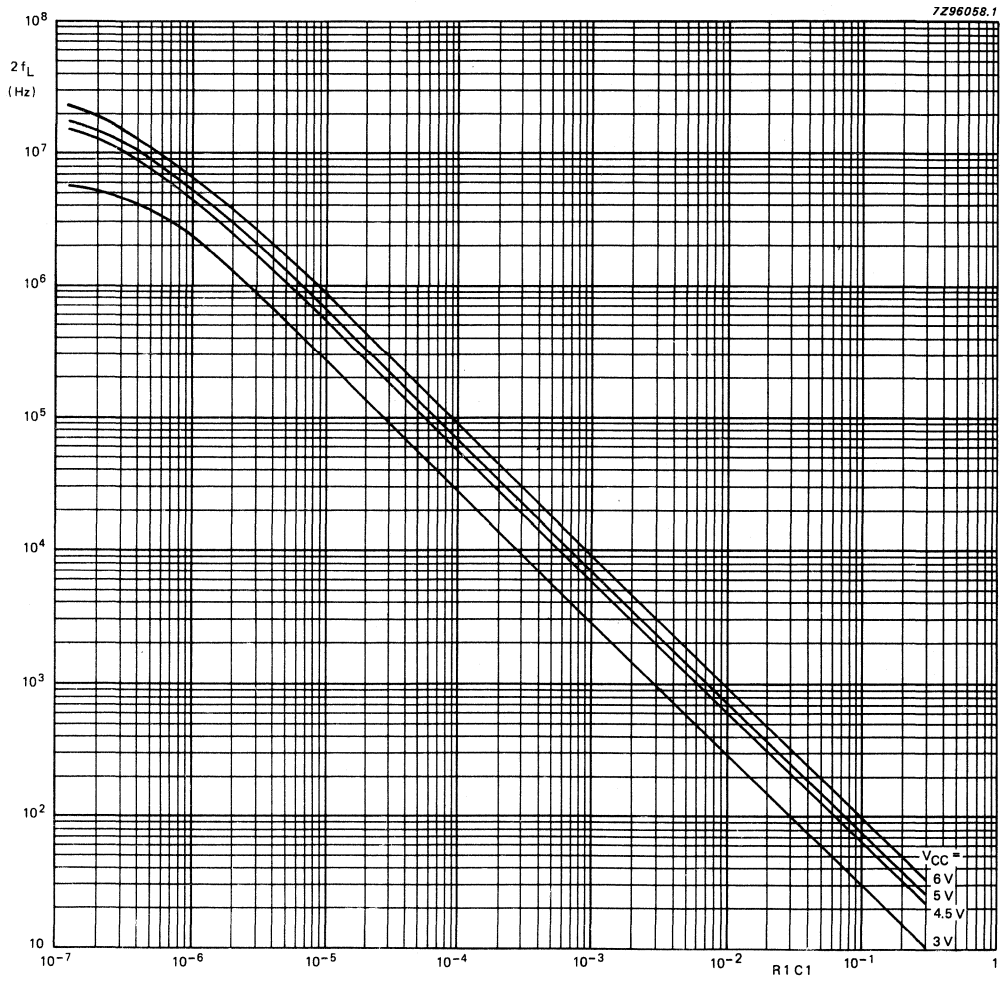


Fig. 31 Typical frequency lock range ($2f_L$) versus the product R1C1: V_{VCOIN} range = 0.9 to ($V_{CC} - 0.9$) V; R2 = ∞; VCO gain:

$$K_V = \frac{2f_L}{V_{VCOIN\ range}} 2\pi \text{ (r/s/V)}.$$

PLL design example

The frequency synthesizer, used in the design example shown in Fig. 32, has the following parameters:

Output frequency: 2 MHz to 3 MHz
frequency steps : 100 kHz
settling time : 1 ms
overshoot : $< 20\%$

The open-loop gain is H (s) x G (s) = $K_p \times K_f \times K_o \times K_n$.

Where:

K_p = phase comparator gain
K_f = low-pass filter transfer gain
K_o = K_v/s VCO gain
K_n = 1/n divider ratio

The programmable counter ratio K_n can be found as follows:

$$N_{min.} = \frac{f_{out}}{f_{step}} = \frac{2\ MHz}{100\ kHz} = 20$$

$$N_{max.} = \frac{f_{out}}{f_{step}} = \frac{3\ MHz}{100\ kHz} = 30$$

The VCO is set by the values of R1, R2 and C1, R2 = 10 kΩ (adjustable).
The values can be determined using the information in the section "DESIGN CONSIDERATIONS".
With f_o = 2.5 MHz and f_L = 500 kHz this gives the following values (V_{CC} = 5.0 V):
R1 = 10 kΩ
R2 = 10 kΩ
C1 = 500 pF

The VCO gain is:

$$K_v = \frac{2f_L \times 2 \times \pi}{0.9 - (V_{CC} - 0.9)} = \frac{1\ MHz}{3.2} \times 2\pi \approx 2 \times 10^6\ r/s/V$$

The gain of the phase comparator is:

$$K_p = \frac{V_{CC}}{4 \times \pi} = 0.4\ V/r.$$

The transfer gain of the filter is given by:

$$K_f = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2)s}.$$

Where:

τ_1 = R3C2 and τ_2 = R4C2.

The characteristics equation is:

1 + H (s) x G (s) = 0.

This results in:

$$s^2 + \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)} s + \frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)} = 0.$$

The natural frequency ω_n is defined as follows:

$$\omega_n = \sqrt{\frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)}}.$$

and the damping value ξ is defined as follows:

$$\zeta = \frac{1}{2\omega_n} \times \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)}.$$

In Fig. 33 the output frequency response to a step of input frequency is shown.

The overshoot and settling time percentages are now used to determine ω_n. From Fig. 33 it can be seen that the damping ratio ζ = 0.45 will produce an overshoot of less than 20% and settle to within 5% at $\omega_n t$ = 5. The required settling time is 1 ms. This results in:

$$\omega_n = \frac{5}{t} = \frac{5}{0.001} = 5 \times 10^3\ r/s.$$

Rewriting the equation for natural frequency results in:

$$(\tau_1 + \tau_2) = \frac{K_p \times K_v \times K_n}{\omega_n^2}.$$

The maximum overshoot occurs at $N_{max.}$:

$$(\tau_1 + \tau_2) = \frac{0.4 \times 2 \times 10^6}{5000^2 \times 30} = 0.0011\ s.$$

When C2 = 470 nF, then

$$R4 = \frac{(\tau_1 + \tau_2) \times 2 \times \omega_n \times \zeta - 1}{K_p \times K_v \times K_n \times C2} = 315\ \Omega$$

now R3 can be calculated:

$$R3 = \frac{\tau_1}{C2} - R4 = 2\ k\Omega.$$

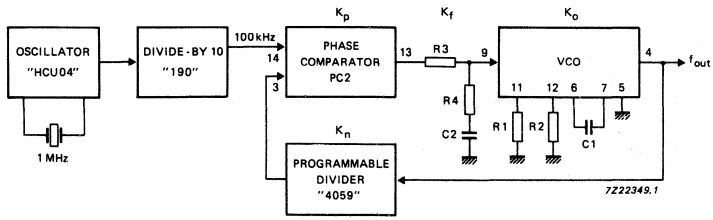


Fig. 32 Frequency synthesizer.

Note

For an extensive description and application example please refer to application note ordering number 9398 649 90011.
Also available a computer design program for PLL's ordering number 9398 961 10061.

APPLICATION INFORMATION (Continued)

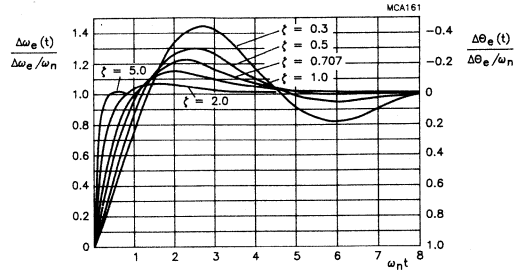


Fig. 33 Type 2, second order frequency step response.

Since the output frequency is proportional to the VCO control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 9 of the VCO. The average frequency response, as calculated by the Laplace method, is found experimentally by smoothing this voltage at pin 9 with a simple RC filter, whose time constant is long compared to the phase detector sampling rate but short compared to the PLL response time.

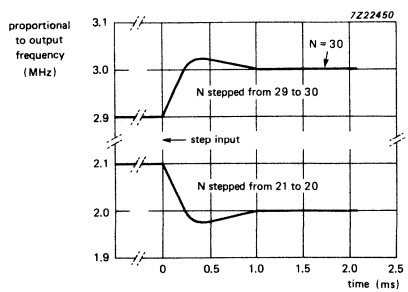


Fig. 34 Frequency compared to the time response.

PHASE-LOCKED-LOOP WITH LOCK DETECTOR

FEATURES

- Low power consumption
- Centre frequency up to 17 MHz (typ.) at V_{CC} = 4.5 V
- Choice of two phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop;
- Excellent VCO frequency linearity
- VCO-inhibit control for ON/OFF keying and for low standby power consumption
- Minimal frequency drift
- Operation power supply voltage range:
  VCO section 3.0 to 6.0 V
  digital section 2.0 to 6.0 V
- Zero voltage offset due to op-amp buffering
- Output capability: standard
- I_{CC} category: MSI

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
f_o	VCO centre frequency	C1 = 40 pF R1 = 3 kΩ V_{CC} = 5 V	19	19	MHz
C_I	input capacitance (pin 5)		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	24	24	pF

GND = 0 V; T_{amb} = 25 °C

Notes

1. Applies to the phase comparator section only (VCO disabled).
   For power dissipation of VCO and demodulator sections see Figs 20, 21 and 22.
2. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38CP).
16-lead mini-pack; plastic (SO16; SOT109A).

GENERAL DESCRIPTION

The 74HC/HCT7046 are high-speed Si-gate CMOS devices and are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT7046 are phase-locked-loop circuits that comprise a linear voltage-controlled oscillator (VCO) and two different phase comparators (PC1 and PC2) with a common signal input amplifier and a common comparator input.

A lock detector is provided and this gives a HIGH level at pin 1 (LD) when the PLL is locked. The lock detector capacitor must be connected between pin 15 (C_{LD}) and pin 8 (GND). The value of the C_{LD} capacitor can be determined, using information supplied in Fig. 32

The input signal can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the "7046" forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

(continued on next page)

APPLICATIONS

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control

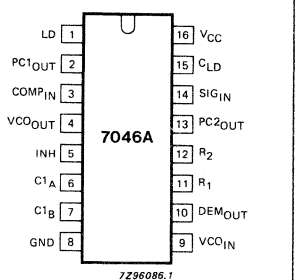


Fig. 1 Pin configuration.

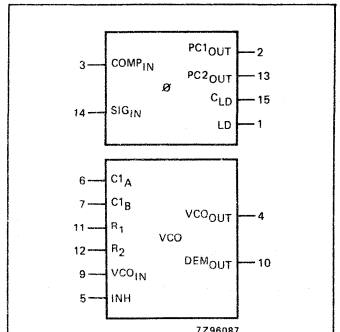


Fig. 2 Logic symbol.

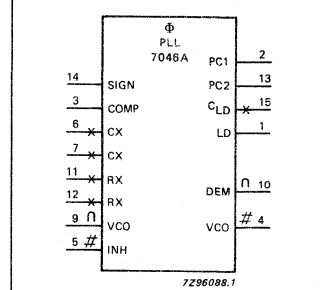


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LD	lock detector output (active HIGH)
2	$PC1_{OUT}$	phase comparator 1 output
3	$COMP_{IN}$	comparator input
4	VCO_{OUT}	VCO output
5	INH	inhibit input
6	$C1_A$	capacitor C1 connection A
7	$C1_B$	capacitor C1 connection B
8	GND	ground (0 V)
9	VCO_{IN}	VCO input
10	DEM_{OUT}	demodulator output
11	R_1	resistor R1 connection
12	R_2	resistor R2 connection
13	$PC2_{OUT}$	phase comparator 2 output
14	SIG_{IN}	signal input
15	C_{LD}	lock detector capacitor input
16	V_{CC}	positive supply voltage

GENERAL DESCRIPTION

VCO

The VCO requires one external capacitor C1 (between $C1_A$ and $C1_B$) and one external resistor R1 (between R_1 and GND) or two external resistors R1 and R2 (between R_1 and GND, and R_2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required.

The high input impedance of the VCO simplifies the design of low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin 10 (DEM_{OUT}). In contrast to conventional techniques where the DEM_{OUT} voltage is one threshold voltage lower than the VCO input voltage, here the DEM_{OUT} voltage equals that of the VCO input. If DEM_{OUT} is used, a load resistor (R_S) should be connected from DEM_{OUT} to GND; if unused, DEM_{OUT} should be left open. The VCO output (VCO_{OUT}) can be connected directly to the comparator input ($COMP_{IN}$), or connected via a frequency-divider. The VCO output signal has a duty factor of 50% (maximum expected deviation 1%), if the VCO input is held at a constant DC level. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

The only difference between the HC and HCT versions is the input level specification of the INH input. This input disables the VCO section. The comparators' sections are identical, so that there is no difference in the SIG_{IN} (pin 14) or $COMP_{IN}$ (pin 3) inputs between the HC and HCT versions.

Phase comparators

The signal input (SIG_{IN}) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

Phase comparator 1 (PC1)

This is an EXCLUSIVE-OR network. The signal and comparator input frequencies (f_i) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10;
$V_{DEMOUT} = V_{PC1OUT}$ (via low-pass filter).

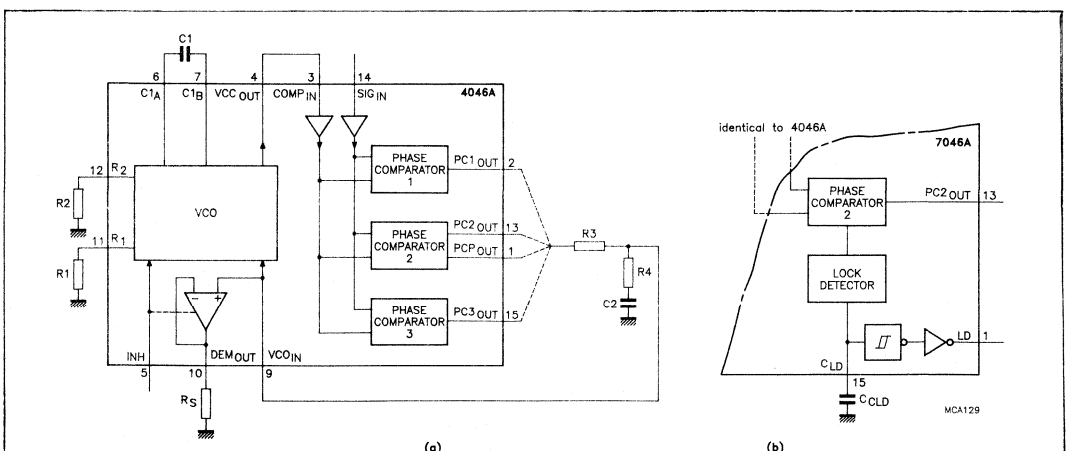


Fig. 4 Functional diagram.

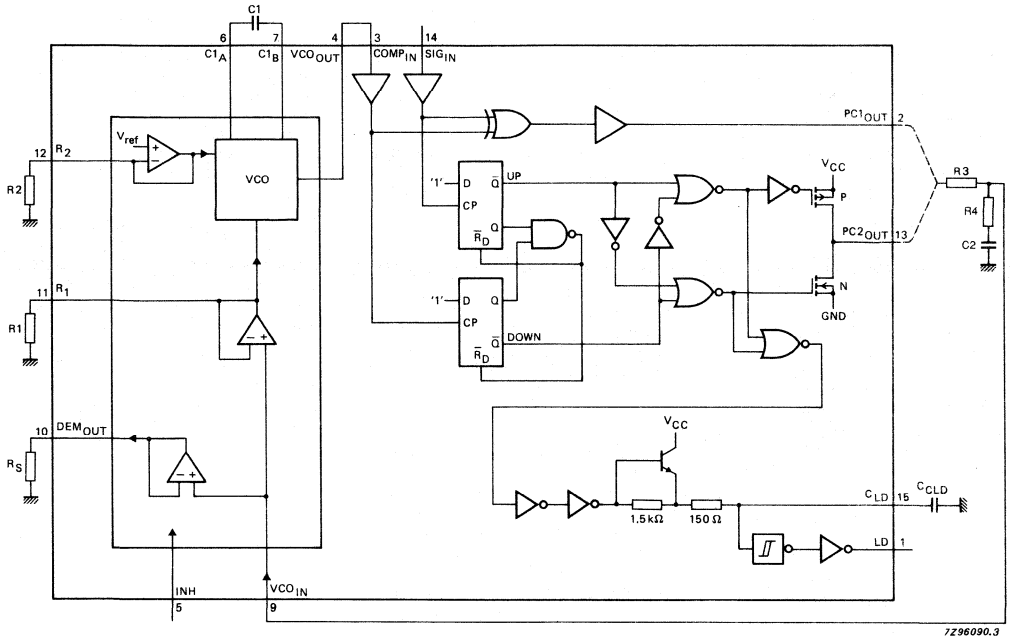


Fig. 5 Logic diagram.

The phase comparator gain is:

$$K_p = \frac{V_{CC}}{\pi} \text{ (V/r)}.$$

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of signals (SIG_{IN}) and the comparator input ($COMP_{IN}$) as shown in Fig. 6. The average of V_{DEMOUT} is equal to 1/2 V_{CC} when there is no signal or noise at SIG_{IN} and with this input the VCO oscillates at the centre frequency (f_o). Typical waveforms for the PC1 loop locked at f_o are shown in Fig. 7.

The frequency capture range ($2f_c$) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2f_L$) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

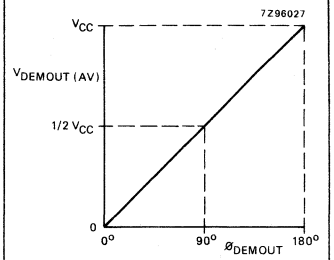


Fig. 6 Phase comparator 1: average output voltage versus input phase difference:

$V_{DEMOUT} = V_{PC1OUT} = \frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$.

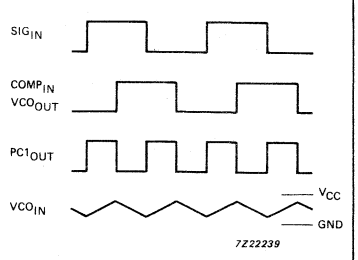


Fig. 7 Typical waveforms for PLL using phase comparator 1, loop locked at f_o.

GENERAL DESCRIPTION

Phase comparators

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration retains lock even with very noisy input signals. Typical behaviour of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO centre frequency.

Phase comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. PC2 comprises two D-type flip-flops, control-gating and a 3-state output stage. The circuit functions as an up-down counter (Fig. 5) where SIG_{IN} causes an up-count and $COMP_{IN}$ a down-count. The transfer function of PC2, assuming ripple ($f_r = f_i$) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{4\pi}(\phi SIGIN - \phi COMPIN)$$

where V_{DEMOUT} is the demodulator output at pin 10;
$V_{DEMOUT} = V_{PC2OUT}$ (via low-pass filter).

The phase comparator gain is:

$$K_p = \frac{V_{CC}}{4\pi} \text{ (V/r)}.$$

V_{DEMOUT} is the resultant of the initial phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Fig. 8. Typical waveforms for the PC2 loop locked at f_o are shown in Fig. 9.

When the frequencies of SIG_{IN} and $COMP_{IN}$ are equal but the phase of SIG_{IN} leads that of $COMP_{IN}$, the p-type output driver at $PC2_{OUT}$ is held "ON" for a time corresponding to the phase difference ($\phi DEMOUT$). When the phase of SIG_{IN} lags that of $COMP_{IN}$, the n-type driver is held "ON".

When the frequency of SIG_{IN} is higher than that of $COMP_{IN}$, the p-type output driver is held "ON" for most of the input signal cycle time, and for the remainder of the cycle both n and p- type drivers are "OFF" (3-state). If the SIG_{IN} frequency is lower than the $COMP_{IN}$ frequency, then it is the n-type driver that is held "ON" for most of the cycle. Subsequently, the voltage at the capacitor (C2) of the low-pass filter connected to $PC2_{OUT}$ varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance.

Thus, for PC2, no phase difference exists between SIG_{IN} and $COMP_{IN}$ over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both p and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG_{IN} the VCO adjusts, via PC2, to its lowest frequency.

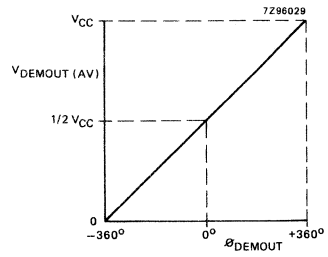


Fig. 8 Phase comparator 2: average output voltage versus input phase difference:
$V_{DEMOUT} - V_{PC2OUT} =$
$\frac{V_{CC}}{4\pi}(\phi SIGIN - \phi COMPIN)$
$\phi DEMOUT = (\phi SIGIN - \phi COMPIN)$.

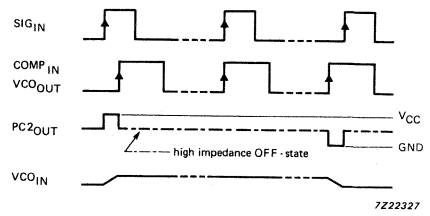


Fig. 9 Typical waveforms for PLL using phase comparator 2, loop locked at f_o.

RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	3.0	5.0	6.0	4.5	5.0	5.5	V	
V_{CC}	DC supply voltage if VCO section is not used	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times (pin 5)		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package plastic DIL		750	mW	for temperature range: −40 to +125 °C 74HC/HCT above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K

DC CHARACTERISTICS FOR 74HC

Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
I_{CC}	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μA	6.0	pins 3, 5, and 14 at V_{CC}; pin 9 at GND; I_I at pins 3 and 14 to be excluded

Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	DC coupled HIGH level input voltage SIG_{IN}, $COMP_{IN}$	1.5 3.15 4.2	1.2 2.4 3.2		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	DC coupled LOW level input voltage SIG_{IN}, $COMP_{IN}$		0.8 2.1 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage LD, PC_{nOUT}	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage LD, PC_{nOUT}	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage LD, PC_{nOUT}		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage LD, PC_{nOUT}		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current SIG_{IN}, $COMP_{IN}$			3.0 7.0 18.0 30.0		4.0 9.0 23.0 38.0		5.0 11.0 27.0 45.0	μA	2.0 3.0 4.5 6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current $PC2_{OUT}$			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
R_I	input resistance SIG_{IN}, $COMP_{IN}$		800 250 150						kΩ	3.0 4.5 6.0	V_I at self-bias operating point; $\Delta V_I = 0.5$ V; see Figs 10, 11 and 12	

VCO section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage INH	2.1 3.15 4.2	1.7 2.4 3.2		2.1 3.15 4.2		2.1 3.15 4.2		V	3.0 4.5 6.0		
V_{IL}	LOW level input voltage INH		1.3 2.1 2.8	0.9 1.35 1.8		0.9 1.35 1.8		0.9 1.35 1.8	V	3.0 4.5 6.0		
V_{OH}	HIGH level output voltage VCO_{OUT}	2.9 4.4 5.9	3.0 4.5 6.0		2.9 4.4 5.9		2.9 4.4 5.9		V	3.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage VCO_{OUT}	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage VCO_{OUT}		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	3.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage VCO_{OUT}		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
V_{OL}	LOW level output voltage $C1_A$, $C1_B$ (test purposes only)			0.40 0.40		0.47 0.47		0.54 0.54	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current INH, VCO_{IN}			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
R1	resistor range	3.0 3.0 3.0		300 300 300					kΩ	3.0 4.5 6.0		note 1
R2	resistor range	3.0 3.0 3.0		300 300 300					kΩ	3.0 4.5 6.0		note 1
C1	capacitor range	40 40 40		no limit					pF	3.0 4.5 6.0		
V_{VCOIN}	operating voltage range at VCO_{IN}	1.1 1.1 1.1		1.9 3.4 4.9					V	3.0 4.5 6.0		over the range specified for R1; for linearity see Figs 18 and 19.

Note

1. The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/or R2 are/is $>$ 10 kΩ.

DC CHARACTERISTICS FOR 74HC

Demodulator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
R_S	resistor range	50 50 50		300 300 300					kΩ	3.0 4.5 6.0	at $R_S > 300$ kΩ the leakage current can influence V_{DEMOUT}
V_{OFF}	offset voltage VCO_{IN} to V_{DEMOUT}		±30 ±20 ±10						mV	3.0 4.5 6.0	$V_I = V_{VCOIN} = 1/2\ V_{CC}$; values taken over R_S range; see Fig. 13
R_D	dynamic output resistance at DEM_{OUT}		25 25 25						Ω	3.0 4.5 6.0	$V_{DEMOUT} = 1/2\ V_{CC}$

AC CHARACTERISTICS FOR 74HC

Phase comparator section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC1_{OUT}$		58 21 17	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 14
t_{PZH}/t_{PZL}	3-state output enable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		74 27 22	280 56 48		350 70 60		420 84 71	ns	2.0 4.5 6.0	Fig. 15
t_{PHZ}/t_{PLZ}	3-state output disable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		96 35 28	325 65 55		405 81 69		490 98 83	ns	2.0 4.5 6.0	Fig. 15
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 14
$V_{I(p-p)}$	AC coupled input sensitivity (peak-to-peak value) at SIG_{IN} or $COMP_{IN}$		9 11 15 33						mV	2.0 3.0 4.5 6.0	f_i = 1 MHz

VCO section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	typ.	max.	min.	max.			
$\Delta f/T$	frequency stability with temperature change				0.20 0.15 0.14				%/K	3.0 4.5 6.0	$V_I = V_{VCOIN}$ = 1/2 V_{CC}; R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Fig. 16
f_o	VCO centre frequency (duty factor = 50%)	3.0 11.0 13.0	10.0 17.0 21.0						MHz	3.0 4.5 6.0	V_{VCOIN} = 1/2 V_{CC}; R1 = 3 kΩ; R2 = ∞; C1 = 40 pF; see Fig. 17
Δf_{VCO}	VCO frequency linearity		1.0 0.4 0.3						%	3.0 4.5 6.0	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 18 and 19
δ_{VCO}	duty factor at VCO_{OUT}		50 50 50						%	3.0 4.5 6.0	

DC CHARACTERISTICS FOR 74HCT

Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
I_{CC}	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μA	6.0	pins 3, 5 and 14 at V_{CC}; pin 9 at GND; I_I at pins 3 and 14 to be excluded
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1) $V_I = V_{CC} - 2.1$ V		100	360		450		490	μA	4.5 to 5.5	pins 3 and 14 at V_{CC}; pin 9 at GND; I_I at pins 3 and 14 to be excluded

Note

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given above. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
INH	1.00

Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	DC coupled HIGH level input voltage SIG_{IN}, $COMP_{IN}$	3.15	2.4						V	4.5		
V_{IL}	DC coupled LOW level input voltage SIG_{IN}, $COMP_{IN}$		2.1	1.35					V	4.5		
V_{OH}	HIGH level output voltage LD, PC_{nOUT}	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage LD, PC_{nOUT}	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage LD, PC_{nOUT}		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage LD, PC_{nOUT}		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current SIG_{IN}, $COMP_{IN}$			30		38		45	μA	5.5	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current $PC2_{OUT}$			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
R_I	input resistance SIG_{IN}, $COMP_{IN}$		250						kΩ	4.5	V_I at self-bias operating point; $\Delta V_I = 0.5$ V; see Figs 10, 11 and 12	

DC CHARACTERISTICS FOR 74HCT

VCO section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage INH	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage INH		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage VCO_{OUT}	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage VCO_{OUT}	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage VCO_{OUT}		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage VCO_{OUT}		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
V_{OL}	LOW level output voltage $C1_A$, $C1_B$ (test purposes only)			0.40		0.47		0.54	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current INH, VCO_{IN}			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
R1	resistor range	3.0		300					kΩ	4.5		note 1
R2	resistor range	3.0		300					kΩ	4.5		note 1
C1	capacitor range	40		no limit					pF	4.5		
V_{VCOIN}	operating voltage range at VCO_{IN}	1.1		3.4					V	4.5		over the range specified for R1; for linearity see Figs 18 and 19.

Note

1. The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/or R2 are/is > 10 kΩ.

Demodulator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
R_S	resistor range	50		300					kΩ	4.5	at $R_S > 300$ kΩ the leakage current can influence V_{DEMOUT}
V_{OFF}	offset voltage VCO_{IN} to V_{DEMOUT}		±20						mV	4.5	$V_I = V_{VCOIN} = 1/2\ V_{CC}$; values taken over R_S range; see Fig. 13
R_D	dynamic output resistance at DEM_{OUT}		25						Ω	4.5	$V_{DEMOUT} = 1/2\ V_{CC}$

AC CHARACTERISTICS FOR 74HCT

Phase comparator section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC1_{OUT}$		21	40		50		60	ns	4.5	Fig. 14
t_{PZH}/t_{PZL}	3-state output enable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		27	56		70		84	ns	4.5	Fig. 15
t_{PHZ}/t_{PLZ}	3-state output disable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		35	65		81		98	ns	4.5	Fig. 15
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 14
$V_{I\ (p-p)}$	AC coupled input sensitivity (peak-to-peak value) at SIG_{IN} or $COMP_{IN}$		15						mV	4.5	f_i = 1 MHz

VCO section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	typ.	max.	min.	max.			
$\Delta f/T$	frequency stability with temperature change				0.15				%/K	4.5	$V_I = V_{VCOIN}$ within recommended range; R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Fig. 16b
f_o	VCO centre frequency (duty factor = 50%)	11.0	17.0						MHz	4.5	V_{VCOIN} = 1/2 V_{CC}; R1 = 3 kΩ; R2 = ∞; C1 = 40 pF; see Fig. 17
Δf_{VCO}	VCO frequency linearity		0.4						%	4.5	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 18 and 19
δ_{VCO}	duty factor at VCO_{OUT}		50						%	4.5	

FIGURE REFERENCES FOR DC CHARACTERISTICS

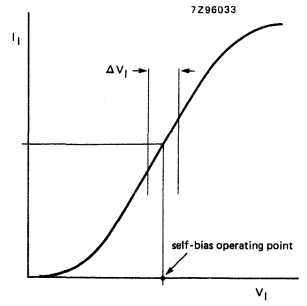


Fig. 10 Typical input resistance curve at SIG_{IN}, $COMP_{IN}$.

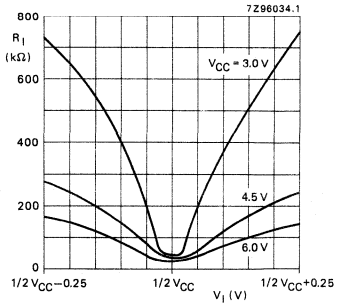


Fig. 11 Input resistance at SIG_{IN}, $COMP_{IN}$ with ΔV_I = 0.5 V at self-bias point.

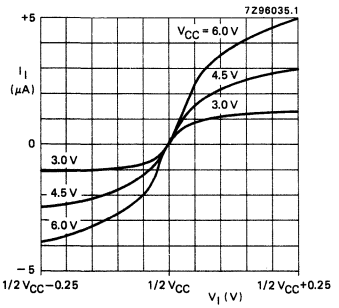
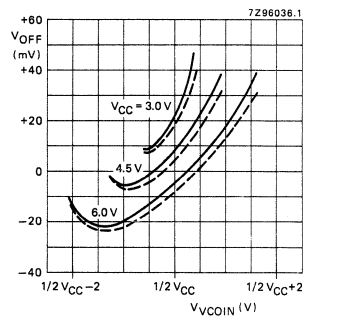


Fig. 12 Input current at SIG_{IN}, $COMP_{IN}$ with ΔV_I = 0.5 V at self-bias point.



— R_S = 50 kΩ
- - - R_S = 300 kΩ

Fig. 13 Offset voltage at demodulator output as a function of VCO_{IN} and R_S.

AC WAVEFORMS

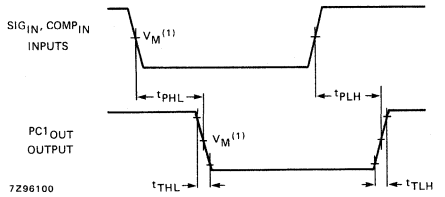


Fig. 14 Waveforms showing input (SIG$_{IN}$, COMP$_{IN}$) to output (PC1$_{OUT}$) propagation delays and the output transition times.

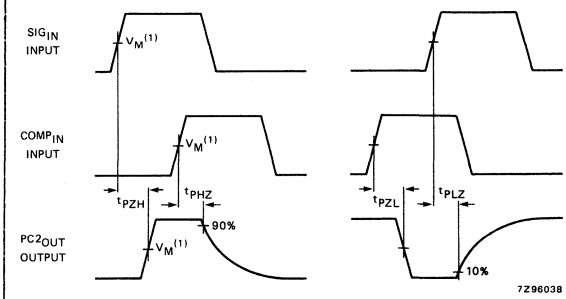


Fig. 15 Waveforms showing the 3-state enable and disable times for PC2$_{OUT}$.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.

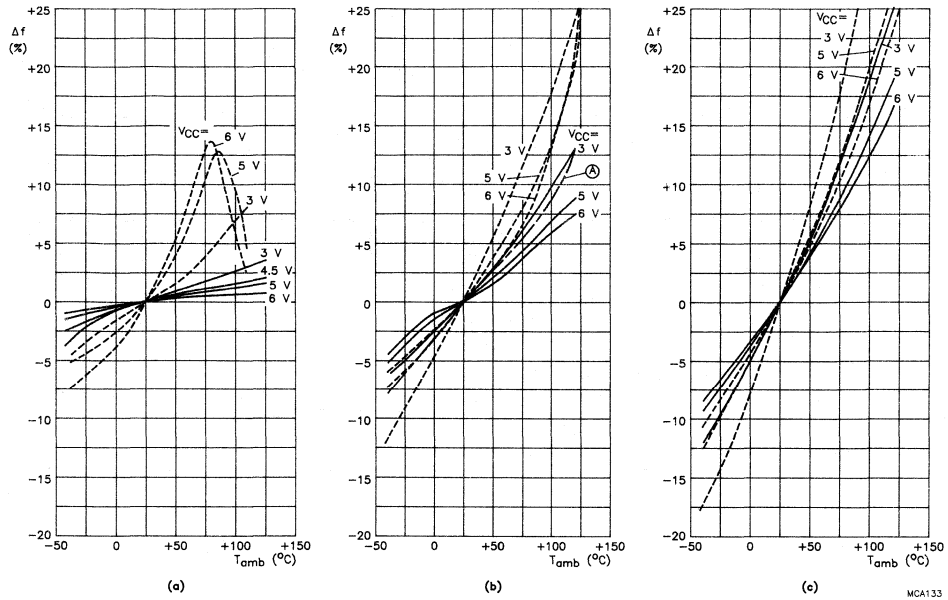
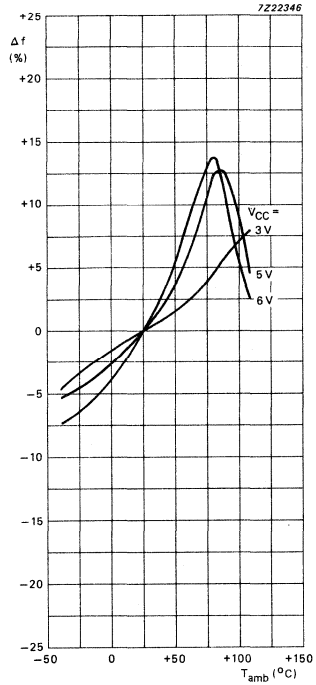
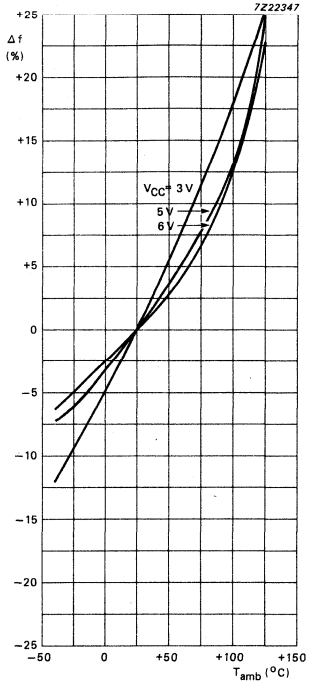


Fig.16 Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.
——— without offset (R2 = ∞): (a) R1 = 3 kΩ; (b) R1 = 10 kΩ; (c) R1 = 300 kΩ.
– – – with offset (R1 = ∞): (a) R2 = 3 kΩ; (b) R2 = 10 kΩ; (c) R2 = 300 kΩ.
In (b), the frequency stability for R1 = R2 = 10 kΩ at 5 V is also given (curve A). This curve is set by the total VCO bias current, and is not simply the addition of the two 10 kΩ stability curves. C1 = 100 pF; $V_{VCO\ IN} = 0.5\ V_{CC}$.

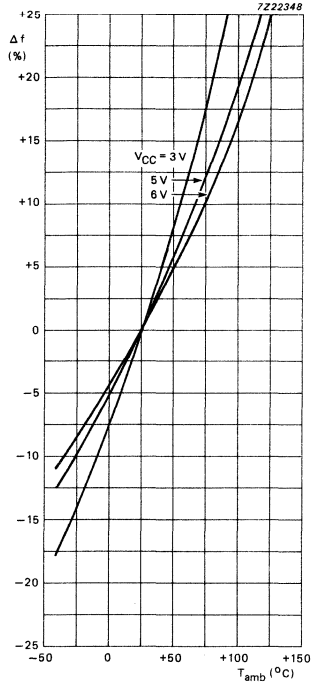
AC WAVEFORMS



(d) R2 = 3 kΩ
R1 = ∞



(e) R2 = 10 kΩ
R1 = ∞

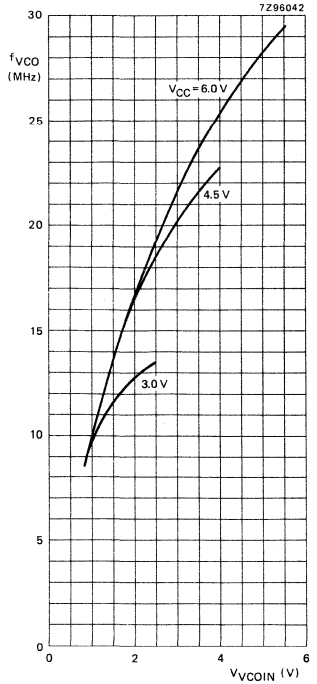


(f) R2 = 300 kΩ
R1 = ∞

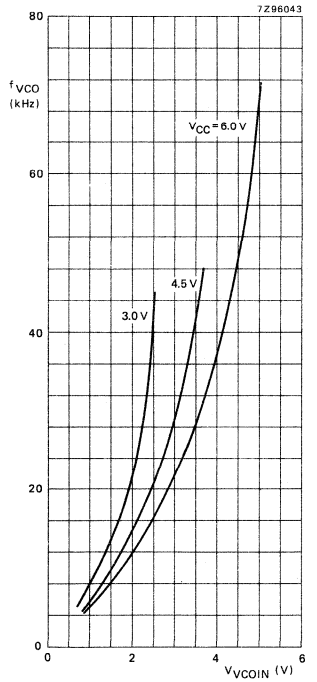
Fig. 16 Continued.

Note to Fig. 16

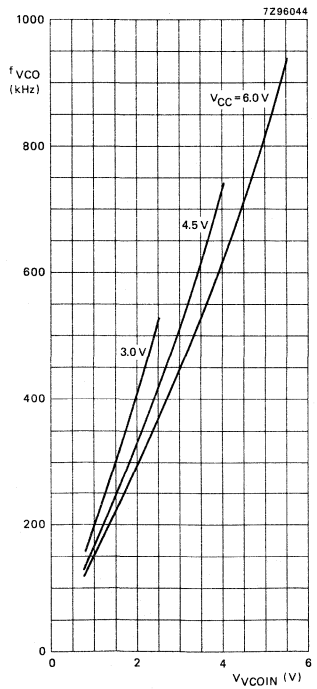
To obtain optimum temperature stability, C_1 must be as small as possible, but larger than 100 pF.



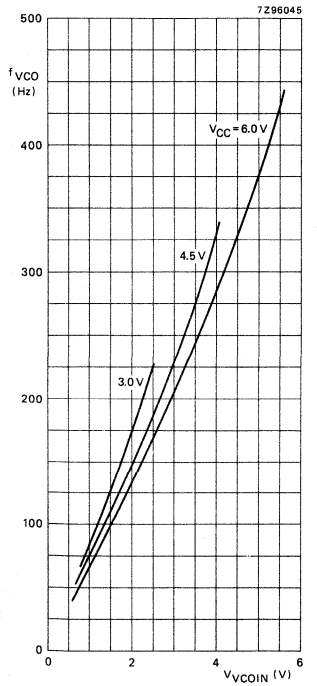
(a) R1 = 3 kΩ; C1 = 40 pF



(b) R1 = 3 kΩ; C1 = 100 nF



(c) R1 = 300 kΩ; C1 = 40 pF



(d) R1 = 300 kΩ; C1 = 100 nF

Fig. 17 Graphs showing VCO frequency (f_{VCO}) as a function of the VCO input voltage (V_{VCOIN}).

AC WAVEFORMS

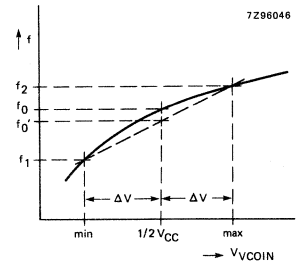


Fig. 18 Definition of VCO frequency linearity: $\Delta V = 0.5$ V over the V_{CC} range: for VCO linearity

$$f'_0 = \frac{f_1 + f_2}{2},$$

$$\text{linearity} = \frac{f'_0 - f_0}{f'_0} \times 100\%$$

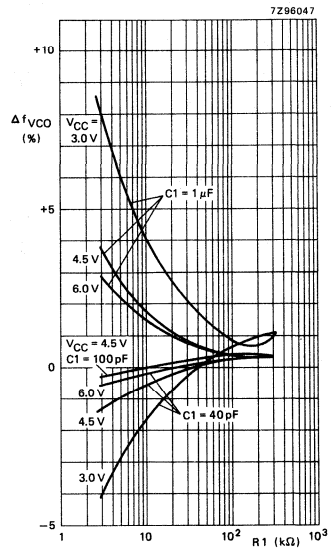
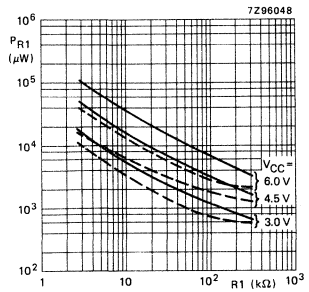
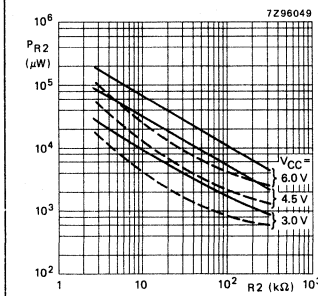


Fig. 19 Frequency linearity as a function of R1, C1 and V_{CC}: R2 = ∞ and ΔV = 0.5 V.



—— C1 = 40 pF
- - - C1 = 1 μF

Fig. 20 Power dissipation versus the value of R1: C_L = 50 pF; R2 = ∞; V_{VCOIN} = 1/2 V_{CC}; T_{amb} = 25 °C.



—— C1 = 40 pF
- - - C1 = 1 μF

Fig. 21 Power dissipation versus the value of R2: C_L = 50 pF; R1 = ∞; V_{VCOIN} = GND = 0 V; T_{amb} = 25 °C.

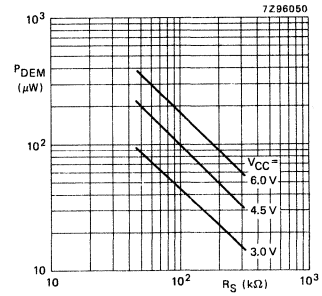


Fig. 22 Typical dc power dissipation of demodulator section as a function of R_S: R1 = R2 = ∞; T_{amb} = 25 °C; V_{VCOIN} = 1/2 V_{CC}.

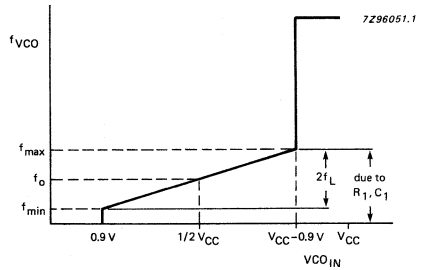
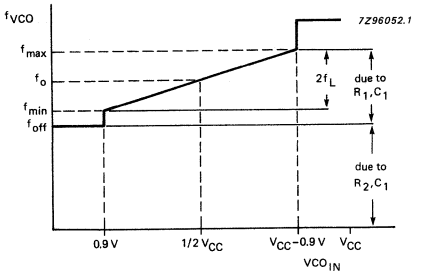
APPLICATION INFORMATION

This information is a guide for the approximation of values of external components to be used with the 74HC/HCT7046 in a phase-lock-loop system.

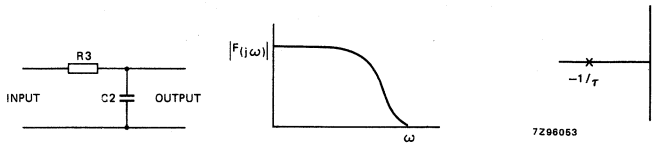
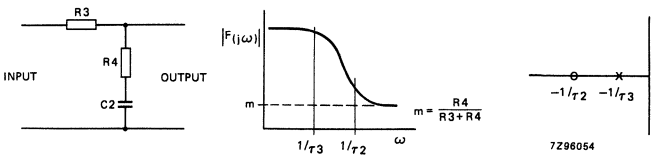
References should be made to Figs 27, 28 and 29 as indicated in the table.

Values of the selected components should be within the following ranges:

R1	between 3 kΩ and 300 kΩ;
R2	between 3 kΩ and 300 kΩ;
R1 + R2	parallel value > 2.7 kΩ;
C1	greater than 40 pF.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
VCO frequency **without extra offset**	PC1, PC2	**VCO frequency characteristic** With R2 = ∞ and R1 within the range 3 kΩ < R1 < 300 kΩ, the characteristics of the VCO operation will be as shown in Fig. 23. (Due to R1, C1 time constant a small offset remains when R2 = ∞.)  Fig. 23 Frequency characteristic of VCO operating without offset: f_o = centre frequency; $2f_L$ = frequency lock range.
	PC1	**Selection of R1 and C1** Given f_o, determine the values of R1 and C1 using Fig. 27.
	PC2	Given f_{max} and f_o, determine the values of R1 and C1 using Fig. 27, use Fig. 29 to obtain $2f_L$ and then use this to calculate f_{min}.
VCO frequency **with extra offset**	PC1, PC2	**VCO frequency characteristic** With R1 and R2 within the ranges 3 kΩ < R1 < 300 kΩ, 3 kΩ < R2 < 300 kΩ, the characteristics of the VCO operation will be as shown in Fig. 24.  Fig. 24 Frequency characteristic of VCO operating with offset: f_o = centre frequency; $2f_L$ = frequency lock range.
	PC1, PC2	**Selection of R1, R2 and C1** Given f_o and f_L, determine the value of product R1C1 by using Fig. 29. Calculate f_{off} from the equation $f_{off} = f_o - 1.6f_L$. Obtain the values of C1 and R2 by using Fig. 28. Calculate the value of R1 from the value of C1 and the product R1C1.

APPLICATION INFORMATION

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
PLL conditions with no signal at the SIG_{IN} input	PC1	VCO adjusts to f_o with ϕ_{DEMOUT} = 90° and V_{VCOIN} = 1/2 V_{CC} (see Fig. 6).
	PC2	VCO adjusts to f_o with ϕ_{DEMOUT} = −360° and V_{VCOIN} = min. (see Fig. 8).
PLL frequency capture range	PC1, PC2	**Loop filter component selection**  (a) τ = R3 x C2 (b) amplitude characteristic (c) pole-zero diagram A small capture range ($2f_c$) is obtained if $2f_c \approx 1/\pi\ (\sqrt{2\pi f_L/\tau})$ Fig. 25 Simple loop filter for PLL **without** offset; R3 ⩾ 500 Ω.  (a) τ_1 = R3 x C2; τ_2 = R4 x C2; τ_3 = (R3 + R4) x C2 (b) amplitude characteristic (c) pole-zero diagram Fig. 26 Simple loop filter for PLL **with** offset; R3 + R4 ⩾ 500 Ω.
PLL locks on harmonics at centre frequency	PC1	yes
	PC2	no
noise rejection at signal input	PC1	high
	PC2	low
AC ripple content when PLL is locked	PC1	$f_r = 2f_i$, large ripple content at ϕ_{DEMOUT} = 90°
	PC2	$f_r = f_i$, small ripple content at ϕ_{DEMOUT} = 0°

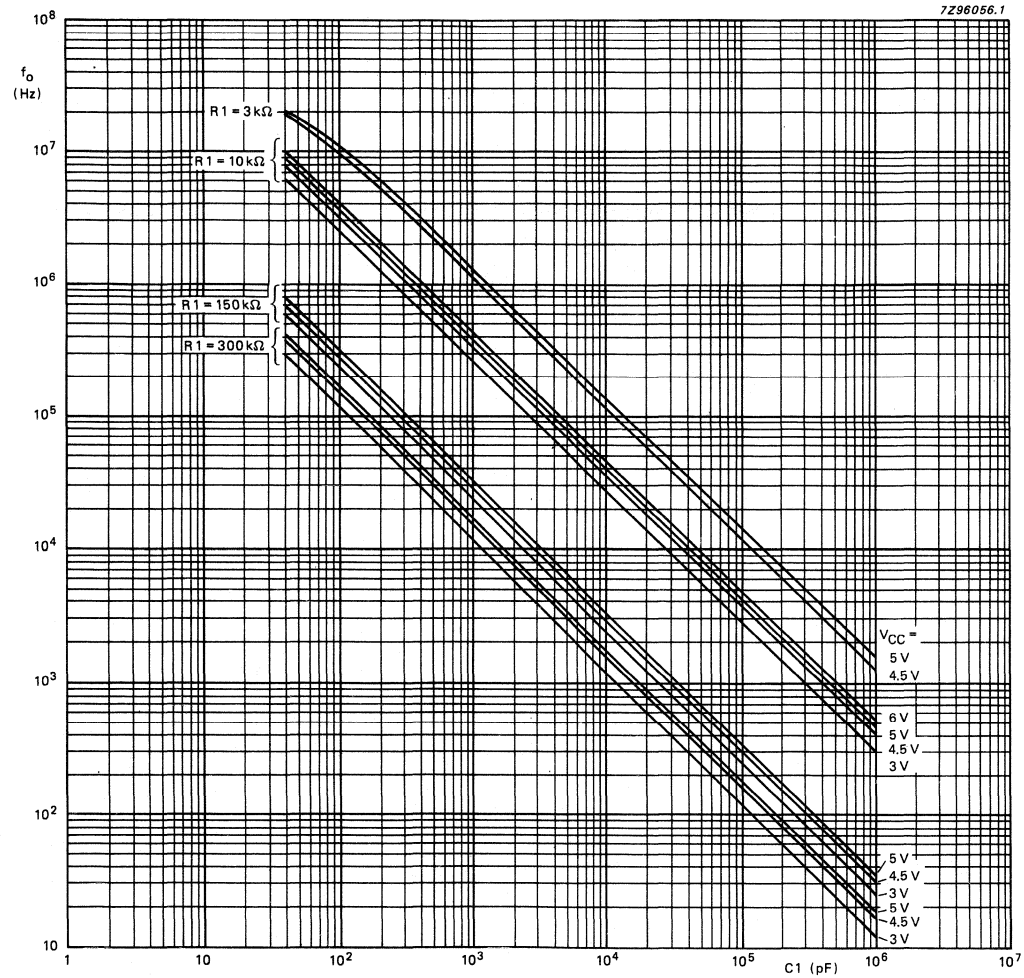


Fig. 27 Typical value of VCO centre frequency (f_o) as a function of C1: R2 = ∞; V_{VCOIN} = 1/2 V_{CC}; INH = GND; T_{amb} = 25 °C.

Notes to Fig. 27

1. To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.
2. Interpolation for various values of R1 can be easily calculated because, a constant R1C1 product will produce almost the same VCO output frequency.

APPLICATION INFORMATION

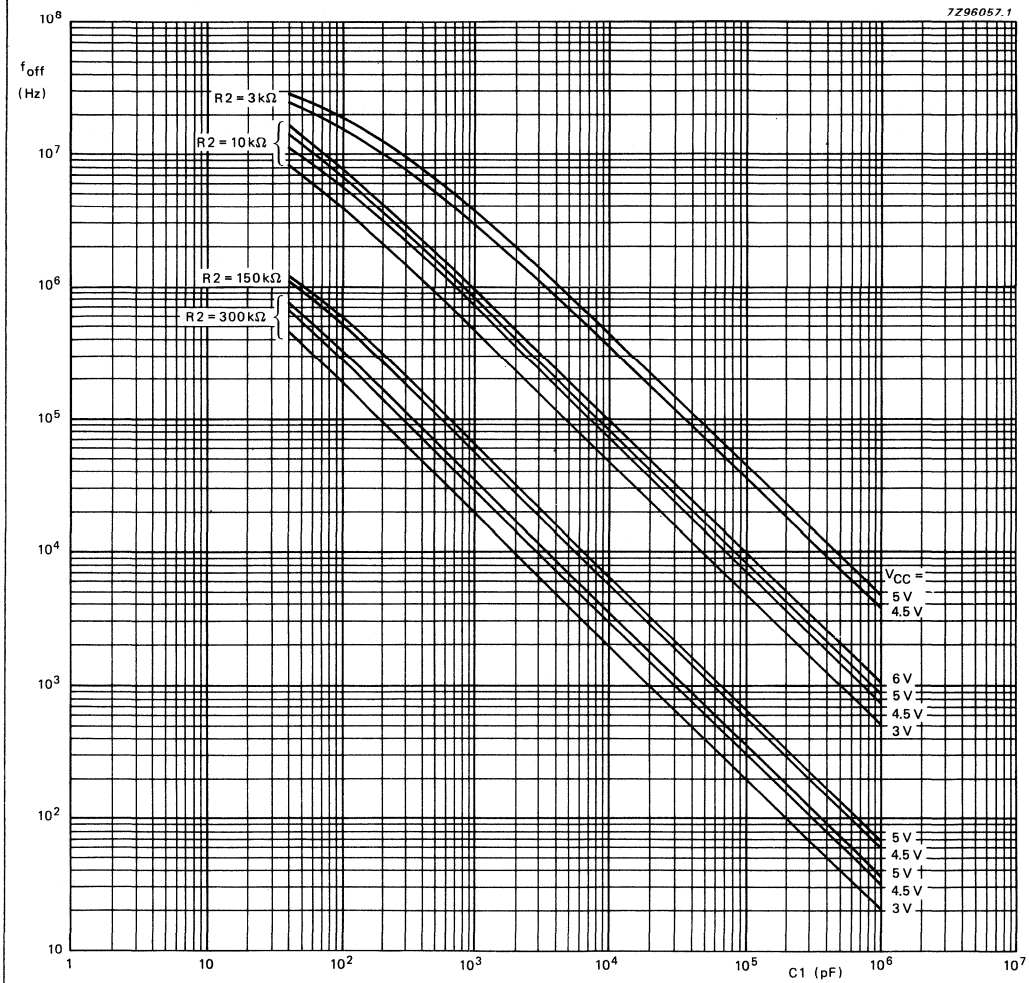


Fig. 28 Typical value of frequency offset as a function of C1: R1 = ∞; V_{VCOIN} = 1/2 V_{CC}; INH = GND; T_{amb} = 25 °C.

Notes to Fig. 28

1. To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.
2. Interpolation for various values of R2 can be easily calculated because, a constant R2C2 product will produce almost the same VCO output frequency.

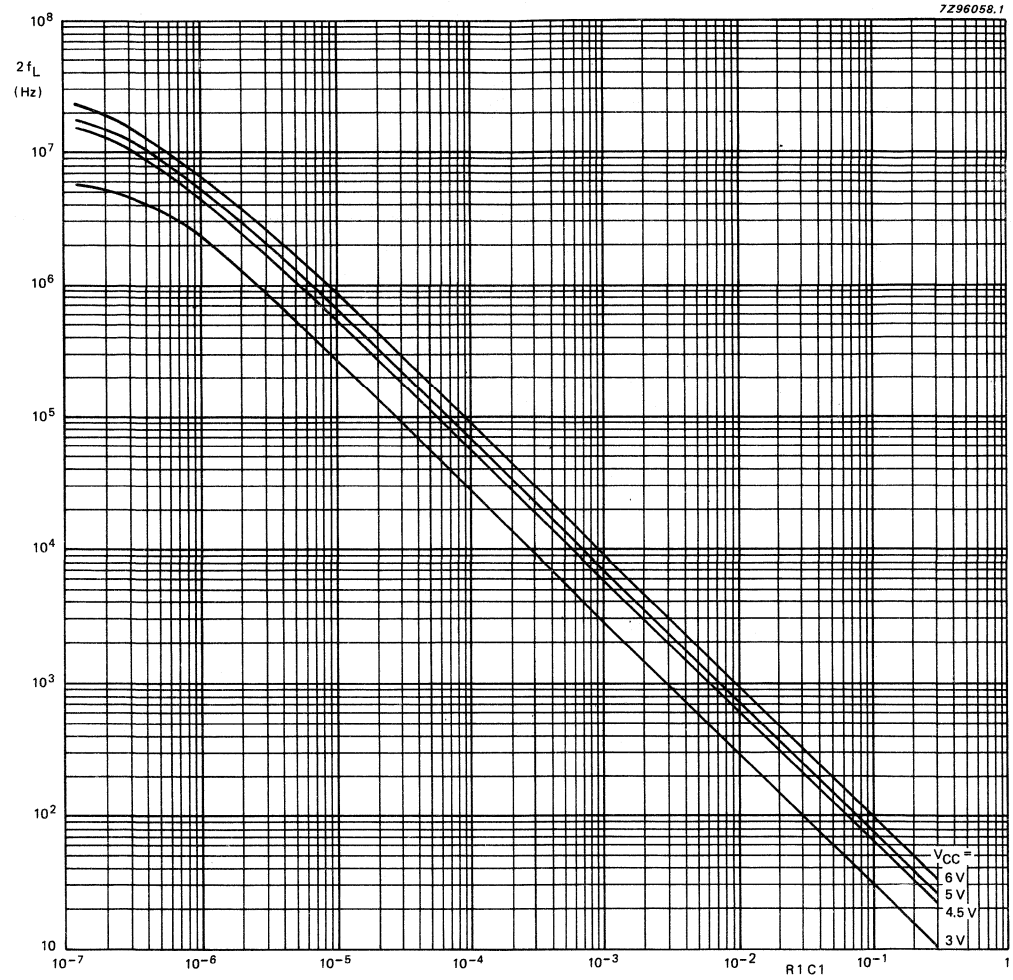


Fig. 29 Typical frequency lock range ($2f_L$) versus the product R1C1: V_{VCOIN} range = 0.9 to ($V_{CC} - 0.9$) V; R2 = ∞; VCO gain:

$$K_V = \frac{2f_L}{V_{VCOIN\ range}} 2\pi \text{ (r/s/V)}.$$

APPLICATION INFORMATION

Lock-detection circuit

The built-in lock-detection circuit will only work when used in conjunction with the phase comparator PC2. The lock-indication is derived from the phase error between SIG_{IN} and $COMP_{IN}$. The PC2 has a typical phase error of zero degrees over the entire VCO operating range. However, to remain in-lock the circuit requires some small adjustments. The variation is dependent on the loop parameters and back-lash time (typically 5 ns). Depending on the application, the phase error can be defined as the limit, a phase error of greater magnitude would be considered out-of-lock. An example of an in-lock detection circuit using the "7046A" is shown in Fig. 30.

If the PLL is in-lock, only very small pulses will come from the "up" or "down" connections of PC2. These pulses are filtered out by a RC network. A Schmitt trigger produces a steady state level, a HIGH level indicates an in-lock condition and a pulsed output indicates an out-of-lock condition as shown in Fig. 31.

Note to Fig. 30

(1) See Fig. 31 for input waveform.

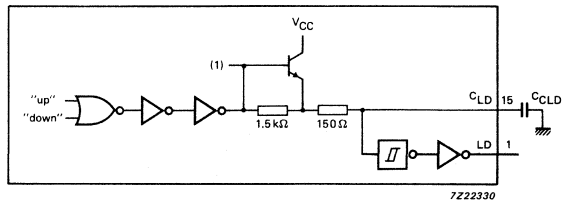


Fig. 30 An example of an in-lock detection circuit using the "7046A".

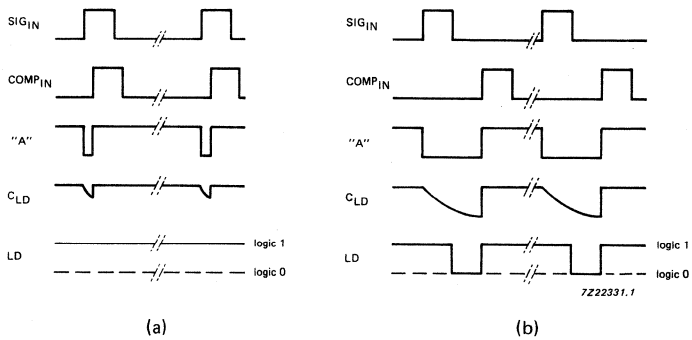


Fig. 31 Waveforms showing the lock detection process; (a) in-lock; (b) out-of-lock.

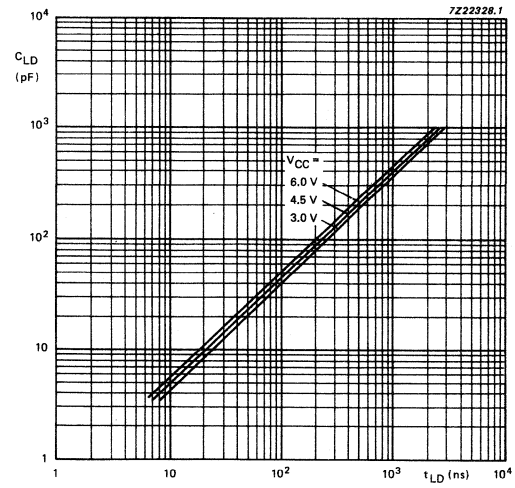


Fig. 32 C_{LD} capacitor value versus typical t_{LD}.

Where:

C_{LD} = capacitor connected to pin 15
(includes the parasitic input capacitance of the IC, approximately 3.5 pF).

t_{LD} = phase difference between SIG_{IN} and $COMP_{IN}$ (positive-going edges).

APPLICATION INFORMATION

The maximum permitted phase error must be defined, before t_{LD} can be defined using the following formula:

$$t_{LD} = \frac{\phi max}{360} \times \frac{1}{f_{IN}}.$$

Using this calculated value in Fig. 32, it is possible to define the value of C_{LD}, e.g. assuming the phase error is 36° and f_{IN} = 2 MHz:

$$t_{LD} = \frac{36°}{360} \times \frac{1}{2\ MHz} = 50\ ns,$$

and using Fig. 32, it can be seen that C_{LD} is 26 pF.

With the addition of one retriggerable monostable (e.g. "123", "423" or "4538") a steady state LOW and HIGH indication can be obtained, as shown in Fig. 33.

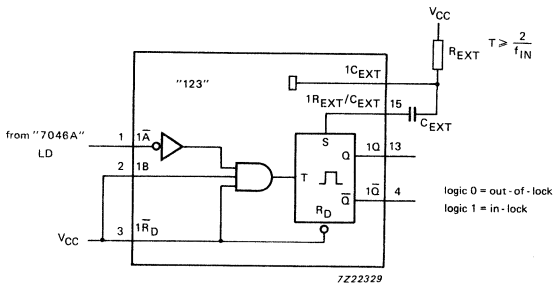


Fig. 33 Steady state signal for lock indication.

PLL design example

The frequency synthesizer, used in the design example shown in Fig. 34, has the following parameters:

Output frequency: 2 MHz to 3 MHz
frequency steps : 100 kHz
settling time : 1 ms
overshoot : $< 20\%$

The open-loop gain is H (s) x G (s) = $K_p \times K_f \times K_o \times K_n$.

Where:

K_p = phase comparator gain
K_f = low-pass filter transfer gain
$K_o = K_v/s$ VCO gain
K_n = 1/n divider ratio

The programmable counter ratio K_n can be found as follows:

$$N_{min.} = \frac{f_{out}}{f_{step}} = \frac{2\ MHz}{100\ kHz} = 20$$

$$N_{max.} = \frac{f_{out}}{f_{step}} = \frac{3\ MHz}{100\ kHz} = 30$$

The VCO is set by the values of R1, R2 and C1, R2 = 10 kΩ (adjustable).
The values can be determined using the information in the section "DESIGN CONSIDERATIONS".
With f_o = 2.5 MHz and f_L = 500 kHz this gives the following values (V_{CC} = 5.0 V):
R1 = 10 kΩ
R2 = 10 kΩ
C1 = 500 pF

The VCO gain is:

$$K_v = \frac{2f_L \times 2 \times \pi}{0.9 - (V_{CC} - 0.9)} = \frac{1\ MHz}{3.2} \times 2\pi \approx 2 \times 10^6\ r/s/v$$

The gain of the phase comparator is:

$$K_p = \frac{V_{CC}}{4 \times \pi} = 0.4\ V/r.$$

The transfer gain of the filter is given by:

$$K_f = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2)s}$$

Where:

τ_1 = R3C2 and τ_2 = R4C2.

The characteristics equation is:

1 + H (s) x G (s) = 0.

This results in:

$$s^2 + \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)} s + \frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)} = 0.$$

The natural frequency ω_n is defined as follows:

$$\omega_n = \sqrt{\frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)}}.$$

and the damping value ξ is defined as follows:

$$\xi = \frac{1}{2\omega_n} \times \frac{1 + K_p \times K_v \times K_n \times \tau_2}{\tau_1 + \tau_2}.$$

The overshoot and settling time percentages are now used to determine ω_n. From Fig. 35 it can be seen that the damping ratio ξ = 0.8 will produce an overshoot of less than 20% and settle to within 5% at $\omega_n t$ = 4.5. The required settling time is 1 ms. This results in:

$$\omega_n = \frac{5}{t} = \frac{5}{0.001} = 5 \times 10^3\ r/s.$$

Rewriting the equation for natural frequency results in:

$$(\tau_1 + \tau_2) = \frac{K_p \times K_v \times K_n}{\omega_n^2}.$$

The maximum overshoot occurs at $N_{max.}$:

$$(\tau_1 + \tau_2) = \frac{0.4 \times 2 \times 10^6}{5000^2 \times 30} = 0.0011\ s.$$

When C2 = 470 nF, then

$$R4 = \frac{(\tau_1 + \tau_2) \times 2 \times \omega_n \times \xi - 1}{K_p \times K_v \times K_n} = 790\ \Omega.$$

R3 is calculated using the damping ratio equation:

$$R3 = \frac{\tau_1}{C2} - R4 = 2\ k\Omega.$$

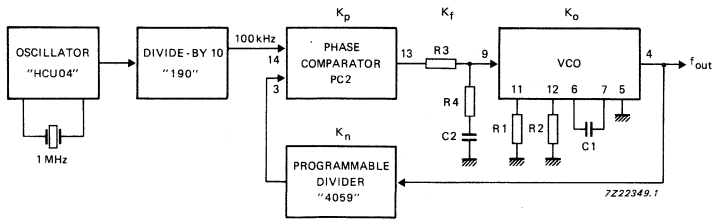


Fig. 34 Frequency synthesizer.

Note

For an extensive description and application example please refer to application note ordering number 9398 649 90011.
Also available a computer design program for PLL's ordering number 9398 961 10061.

APPLICATION INFORMATION

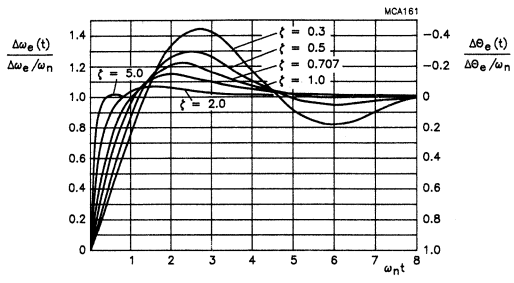


Fig. 35 Type 1, second order frequency step response.

Since the output frequency is proportional to the VCO control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 9 of the VCO. The average frequency response, as calculated by the Laplace method, is found experimentally by smoothing this voltage at pin 9 with a simple RC filter, whose time constant is long compared to the phase detector sampling rate but short compared to the PLL response time.

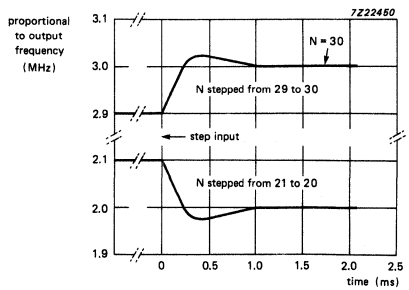
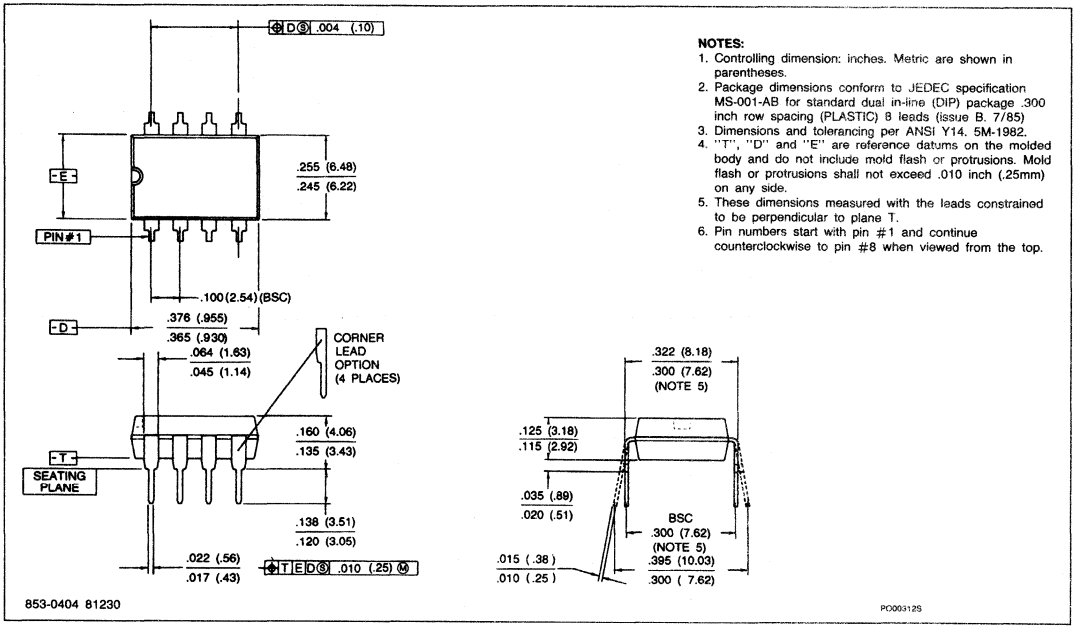


Fig. 36 Frequency compared to the time response.

PACKAGE INFORMATION

Package outlines
Soldering

NE1 8-PIN PLASTIC PDIP



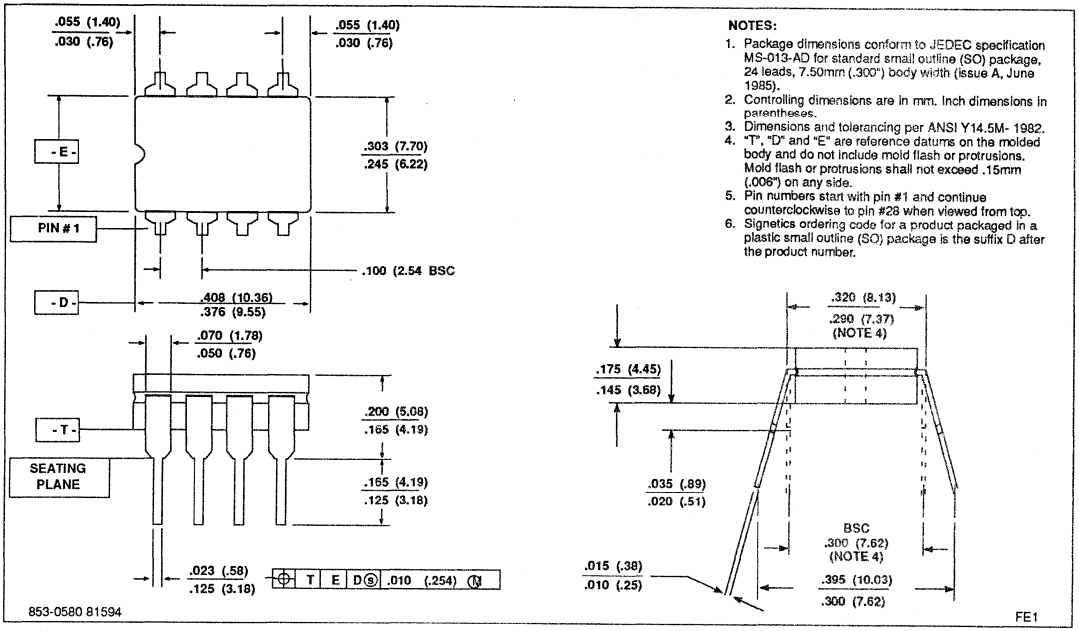
NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B, 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.

853-0404 81230

PO00312S

8-PIN CERAMIC DIP (FE PACKAGE)



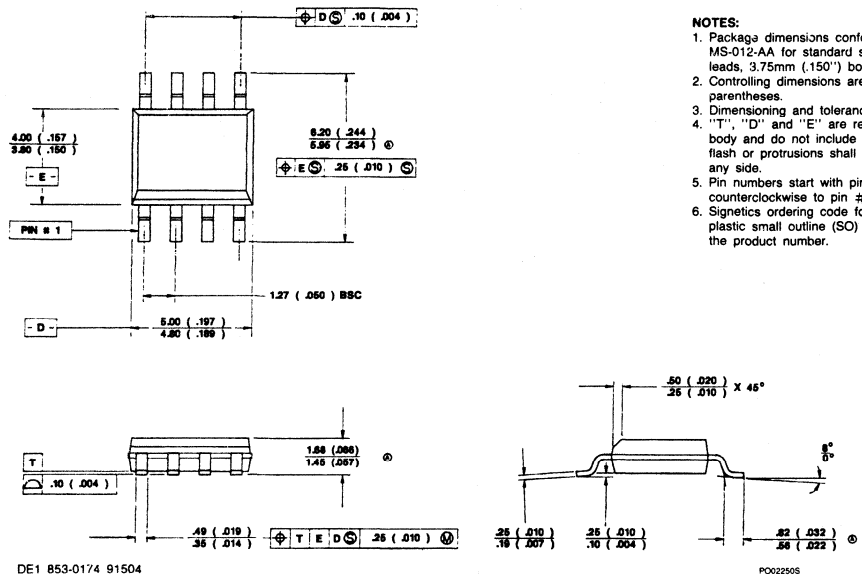
NOTES:

1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

853-0580 81594

FE1

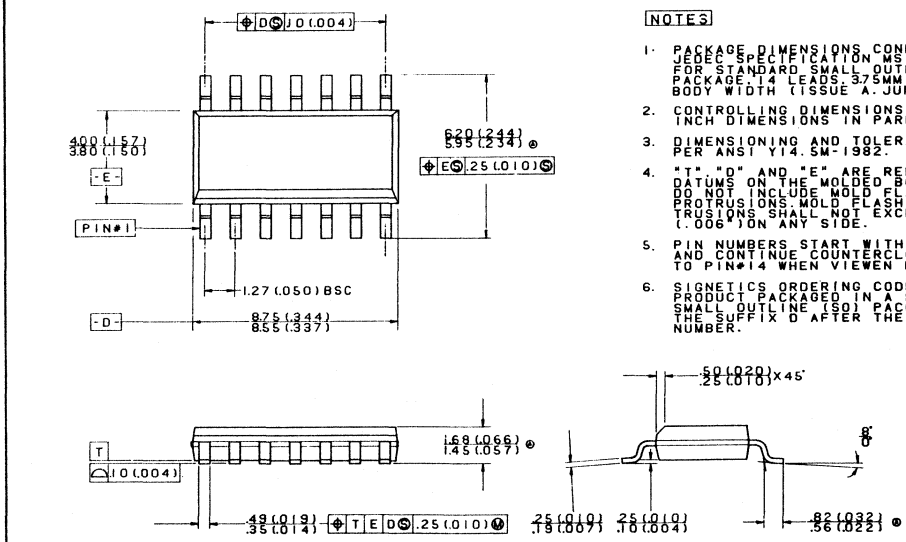
8-PIN PLASTIC SMALL OUTLINE (SO)



NOTES:

1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

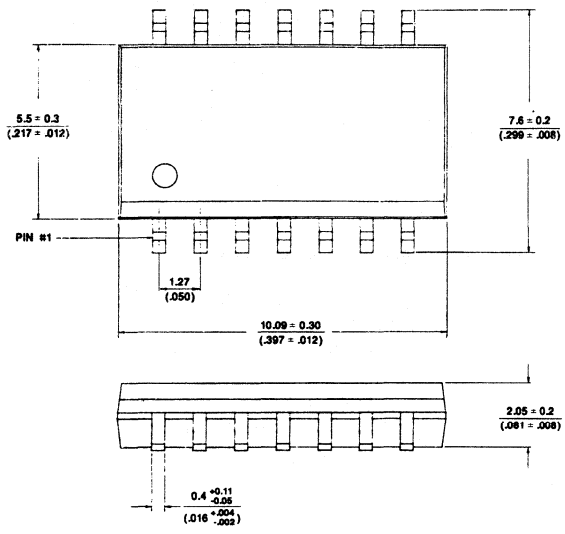
14-PIN PLASTIC SMALL OUTLINE (SO)

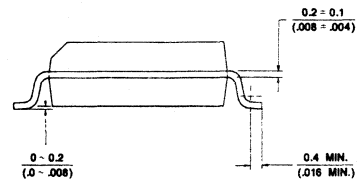


NOTES

1. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MS-012-AB FOR STANDARD SMALL OUTLINE (SO) PACKAGE. 14 LEADS. 3.75MM (.150") BODY WIDTH (ISSUE A. JUNE 1985).
2. CONTROLLING DIMENSIONS ARE MM. INCH DIMENSIONS IN PARENTHESES.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
4. "T", "D" AND "E" ARE REFERENCE DATUMS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .15MM (.006") ON ANY SIDE.
5. PIN NUMBERS START WITH PIN#1 AND CONTINUE COUNTERCLOCKWISE TO PIN#14 WHEN VIEWEN FROM TOP.
6. SIGNETICS ORDERING CODE FOR A PRODUCT PACKAGED IN A PLASTIC SMALL OUTLINE (SO) PACKAGE IS THE SUFFIX D AFTER THE PRODUCT NUMBER.

14-PIN PLASTIC SMALL OUTLINE



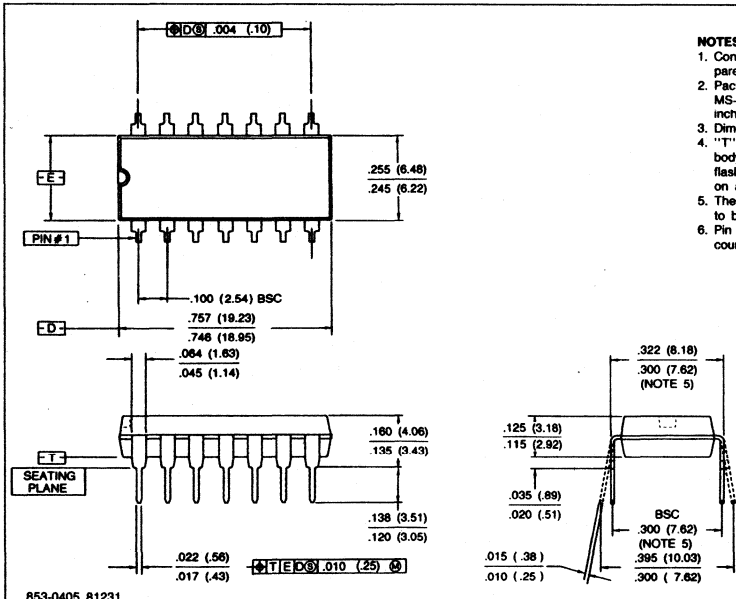


NOTES:
1. Controlling dimensions are in mm. Dimensions in parentheses are in inches.
2. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.

DHA 853-0634 95138

PO01950S

NH1 14-PIN PLASTIC PDIP

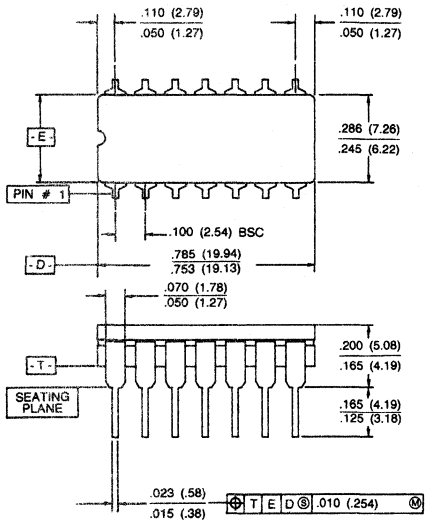


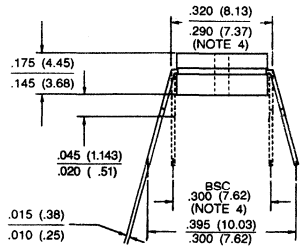
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AC for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 14 leads (issue B, 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

853-0405 81231

PO00330S

FH1 14-PIN HERMETIC CERDIP



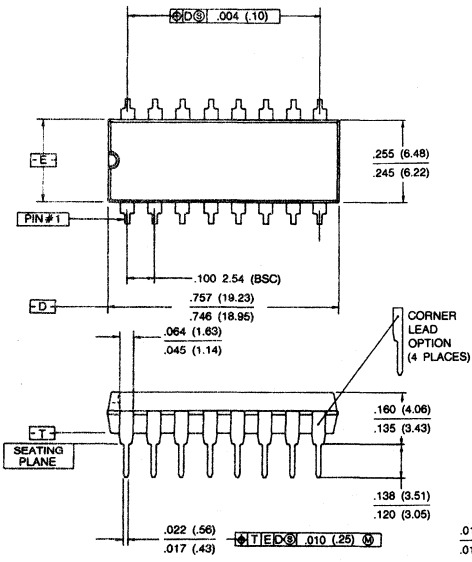


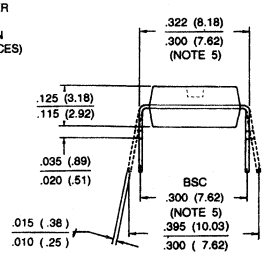
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

853-0581 88375

PO00441S

NJ1 16-PIN PLASTIC PDIP



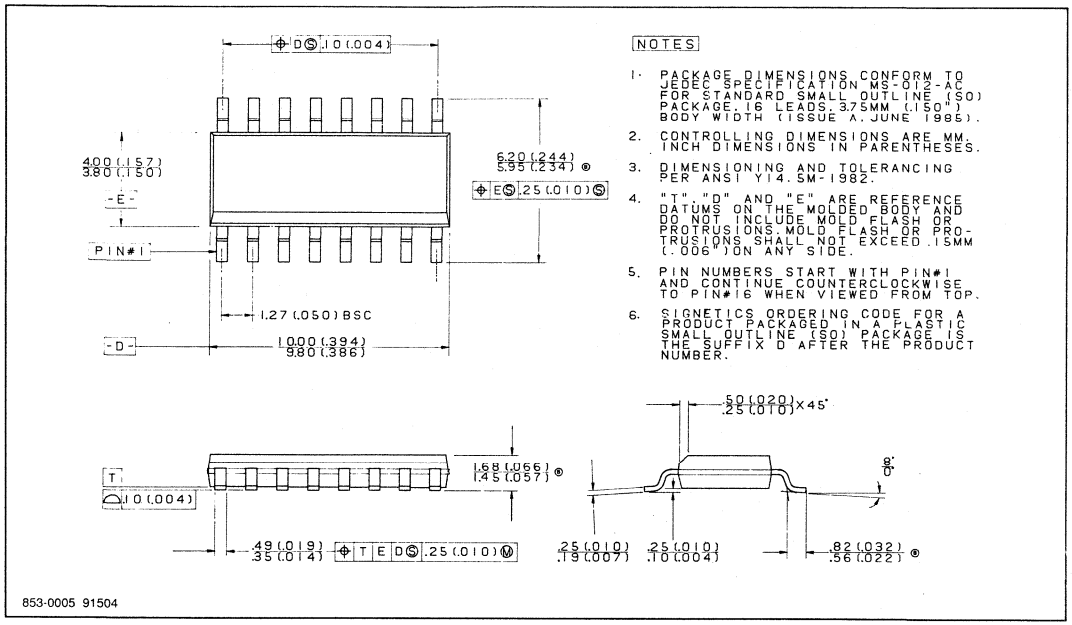


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

853-0406 81232

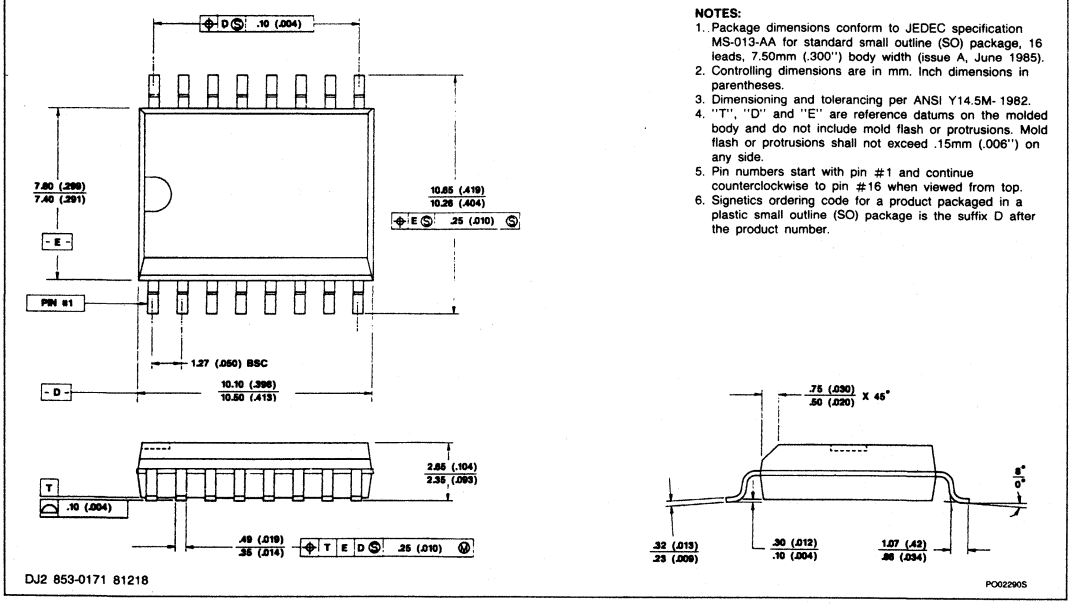
PO00280S

16-PIN PLASTIC DIP (SO)



853-0005 91504

16-PIN PLASTIC SMALL OUTLINE (SOL)



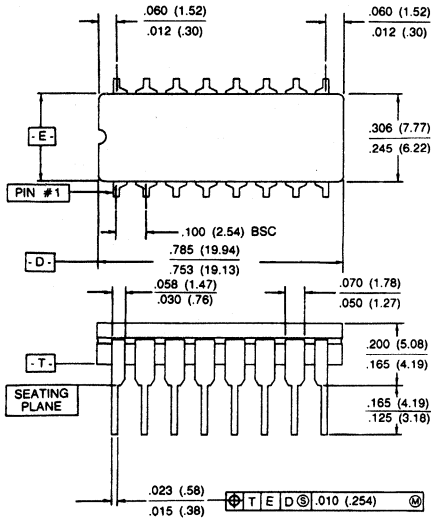
NOTES:

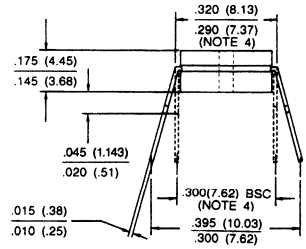
1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

DJ2 853-0171 81218

PO02290S

16-PIN HERMETIC CERDIP



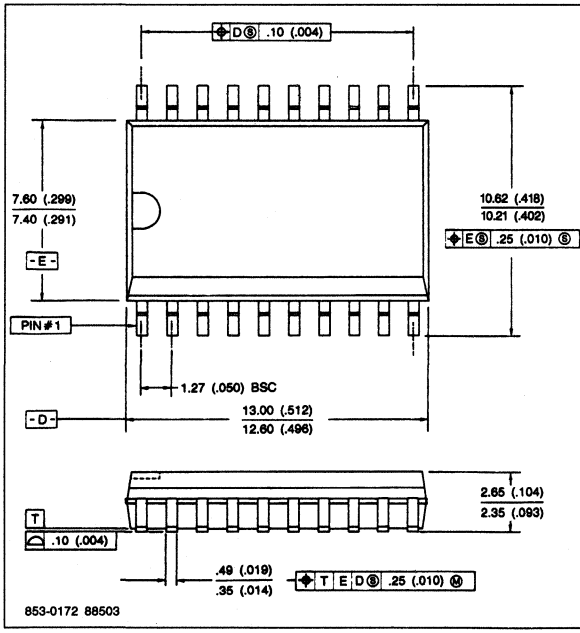


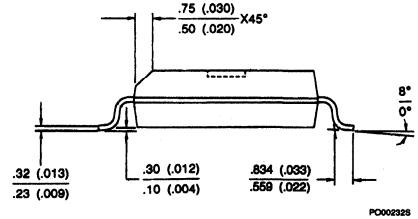
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

FJ1 853-0582 88375

PO00491S

DL2 20-PIN PLASTIC SOL



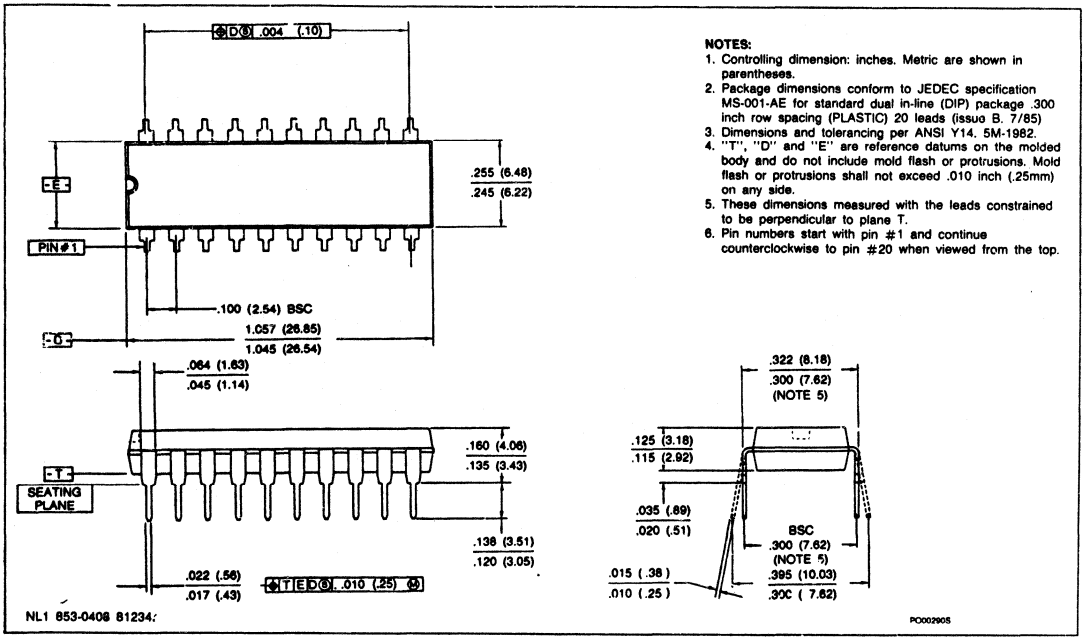


NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

853-0172 88503

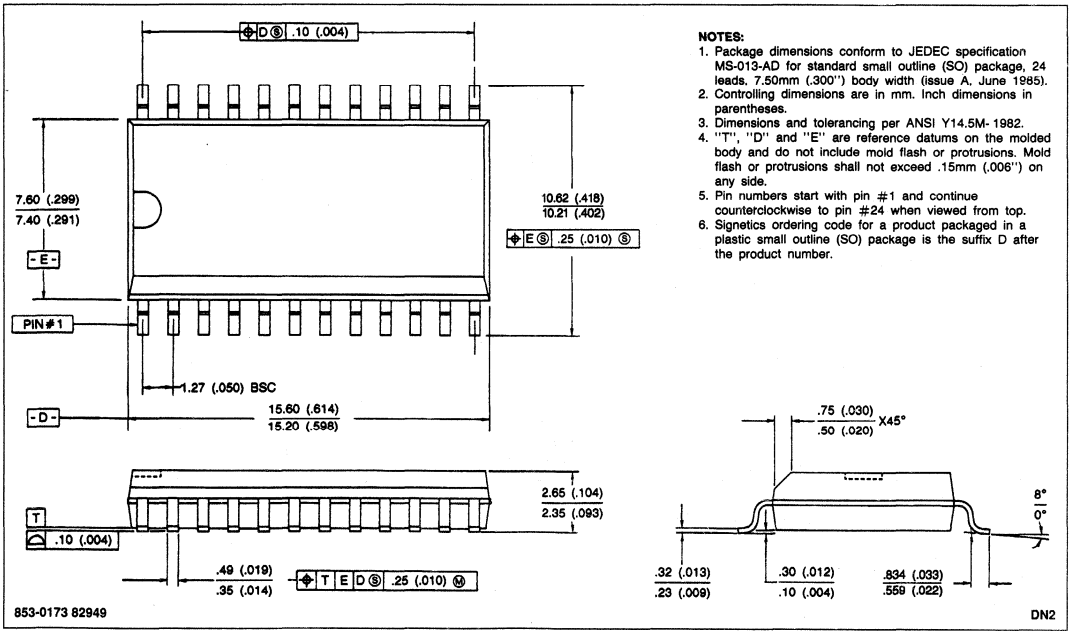
PO00232S

20-PIN PLASTIC DUAL IN-LINE (PDIP)



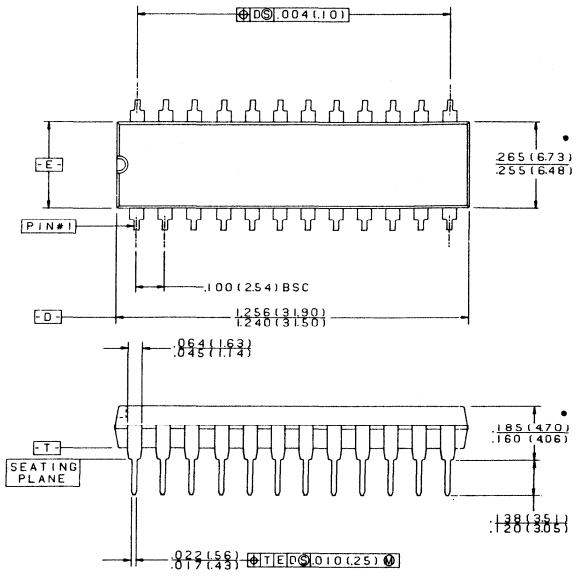
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AE for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 20 leads (issue B, 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

24-PIN PLASTIC (SOL)



NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

24-PIN PLASTIC (DIP)



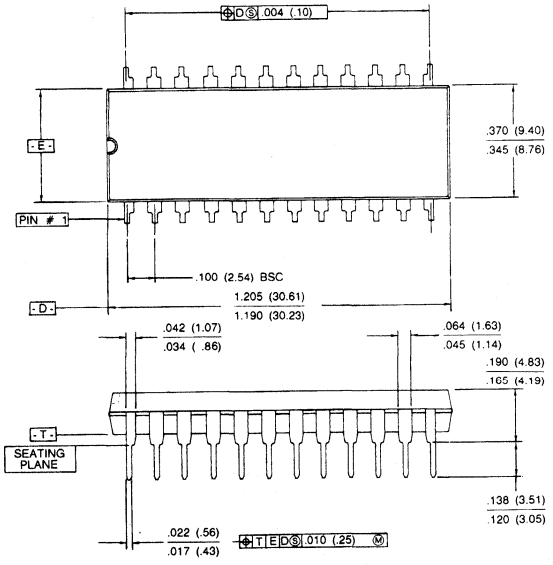
NOTES

1. CONTROLLING DIMENSION: INCHES METRIC ARE SHOWN IN PARENTHESES.
2. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MS-001-AF FOR STANDARD DUAL IN-LINE (DIP) PACKAGE .300 INCH ROW SPACING (PLASTIC) 24 LEADS (ISSUE B, 7/85)
3. DIMENSION AND TOLERANCING PER ANSI Y14.5M-1982.
4. "T", "D" AND "E" ARE REFERENCE DATUMS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (.25MM) ON ANY SIDE.
5. THESE DIMENSIONS MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE T.
6. PIN NUMBERS START WITH PIN#1 AND CONTINUE COUNTERCLOCKWISE TO PIN#24 WHEN VIEWED FROM THE TOP.

853-0410 98727

NN1

24-PIN PLASTIC DUAL IN-LINE (PDIP) (400mil-wide)

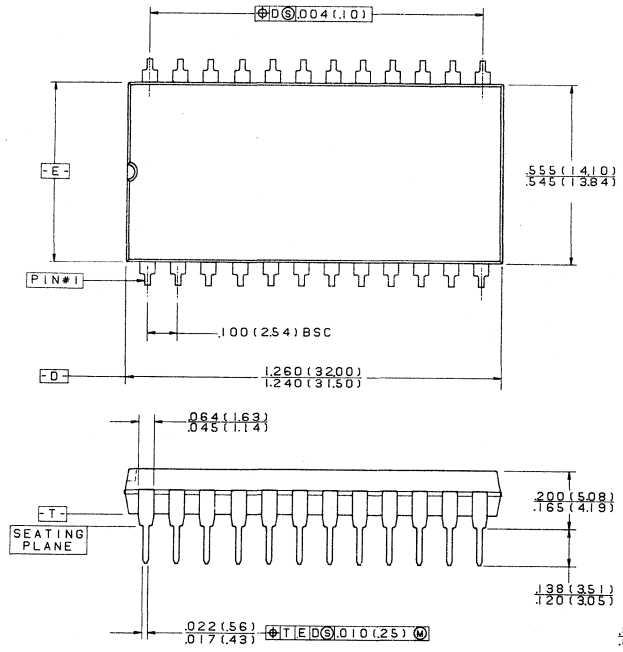


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14. 5M-1982.
3. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

NN2 853-0411 81237

PO00351S

24-PIN PLASTIC (DIP) (600 mil-wide)

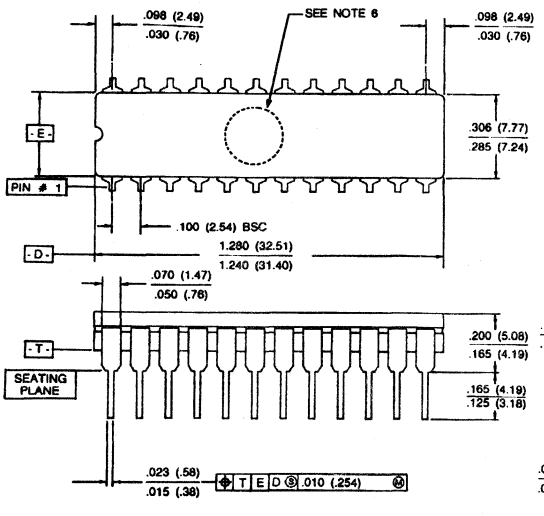


NOTES

1. CONTROLLING DIMENSION: INCHES. METRIC ARE SHOWN IN PARENTHESES.
2. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MS-011-AA FOR STANDARD DUAL IN-LINE(DIP) PACKAGE .600 INCH ROW SPACING (PLASTIC) 24 LEADS (ISSUE B, 7/85)
3. DIMENSION AND TOLERANCING PER ANSI Y14.5M-1982.
4. "T", "D" AND "E" ARE REFERENCE DATUMS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (.25MM) ON ANY SIDE.
5. THESE DIMENSIONS MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE T.
6. PIN NUMBERS START WITH PIN#1 AND CONTINUE COUNTERCLOCKWISE TO PIN#24 WHEN VIEWED FROM THE TOP.

853-0412 81238

24-PIN CERAMIC DIP (300 mil-wide)



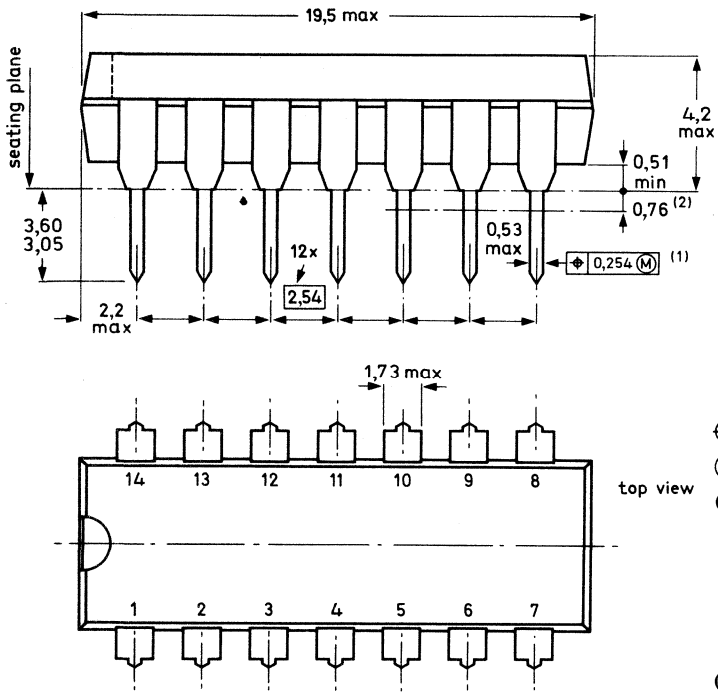
NOTES:

1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M - 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.
6. Denotes window location for EPROM products (see FA package).

853-0586 84000

P000402S

14-LEAD DUAL IN-LINE; PLASTIC (SOT27)



Dimensions in mm

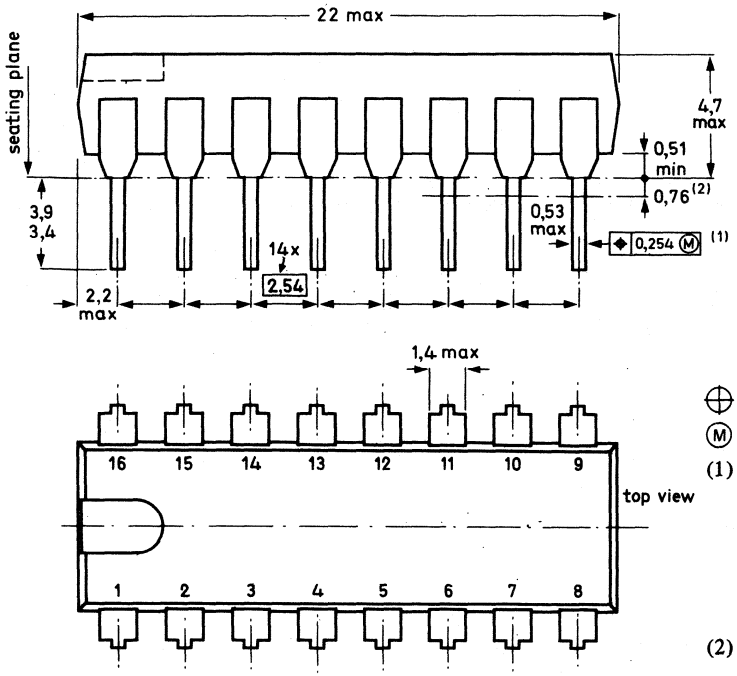
⊕ Positional accuracy.

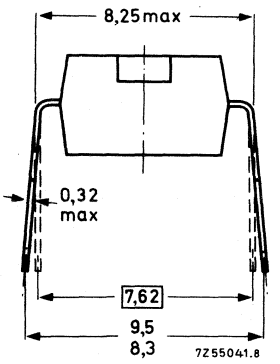
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

16-LEAD DUAL IN-LINE; PLASTIC (SOT38)





⊕ Positional accuracy.

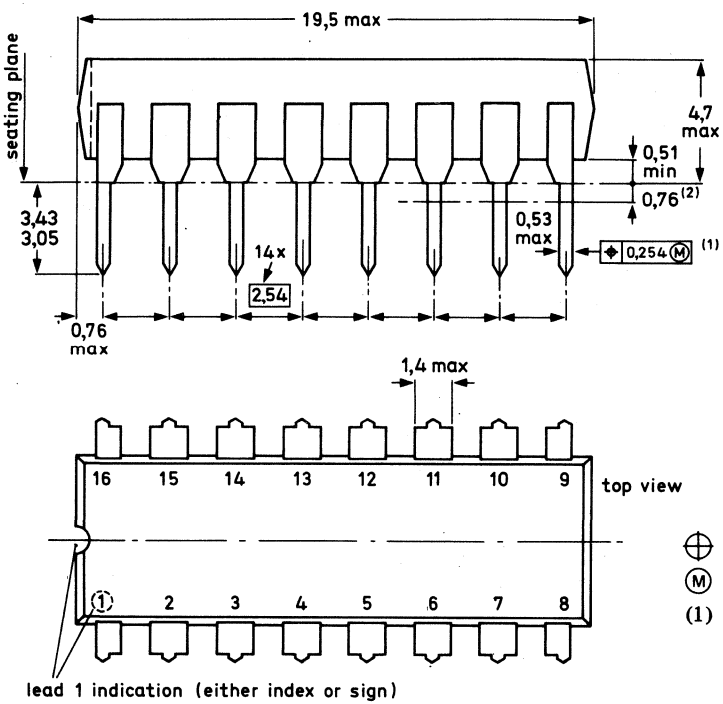
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC (SOT38C, P)



⊕ Positional accuracy.

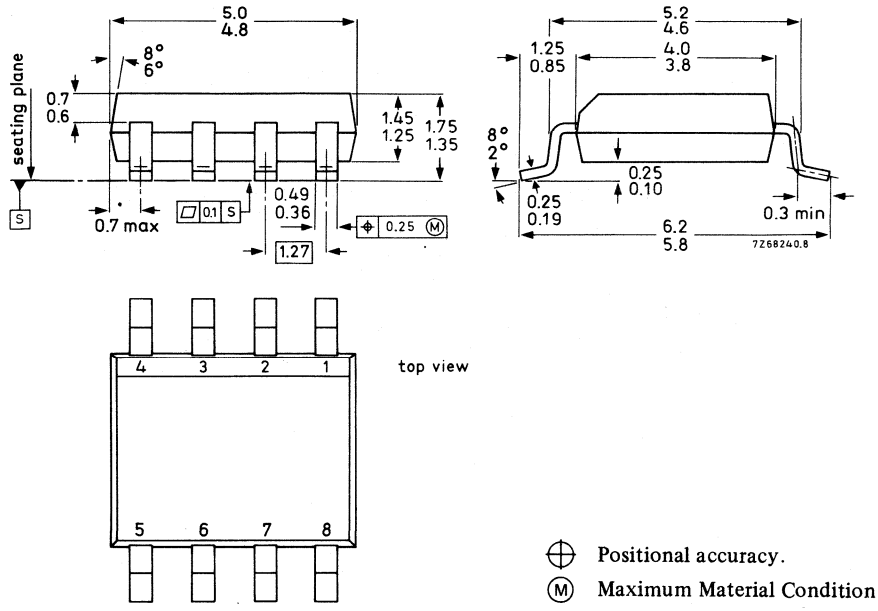
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO8; SOT96A)

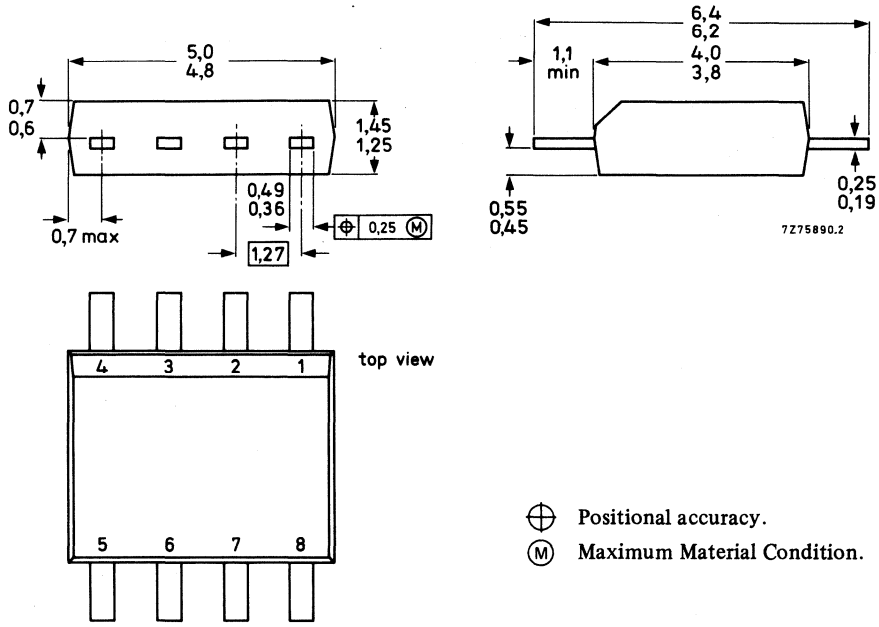


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO8; SOT96C)

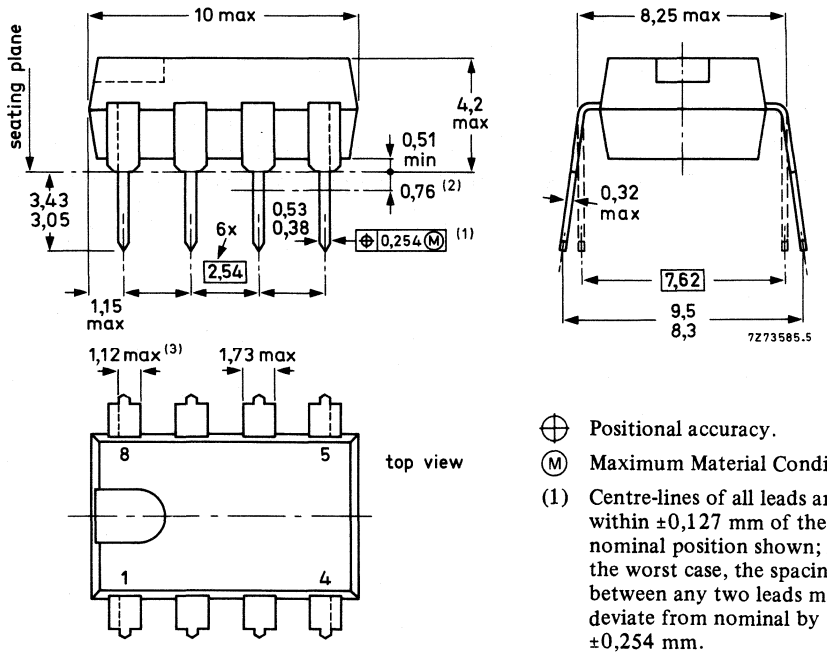


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

8-LEAD DUAL IN-LINE; PLASTIC (SOT97)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

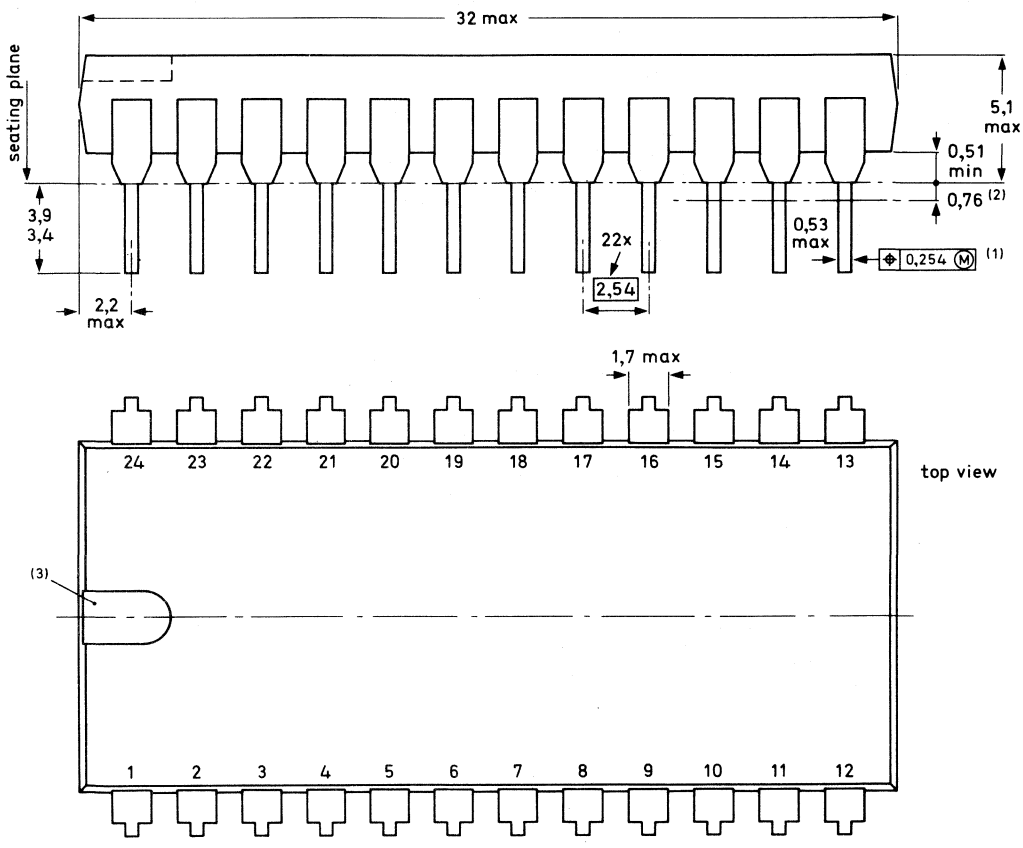
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

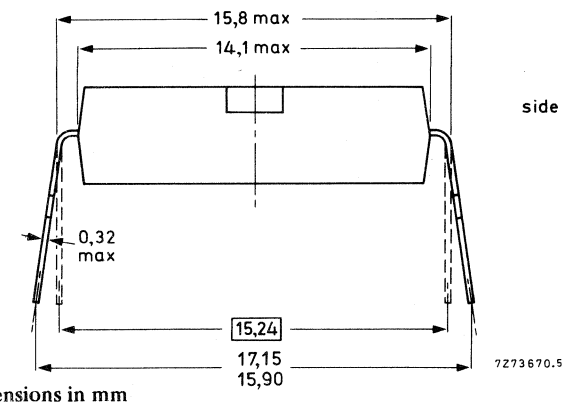
(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

24-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT101A, B, F, G, L)





Dimensions in mm

⊕ Positional accuracy.

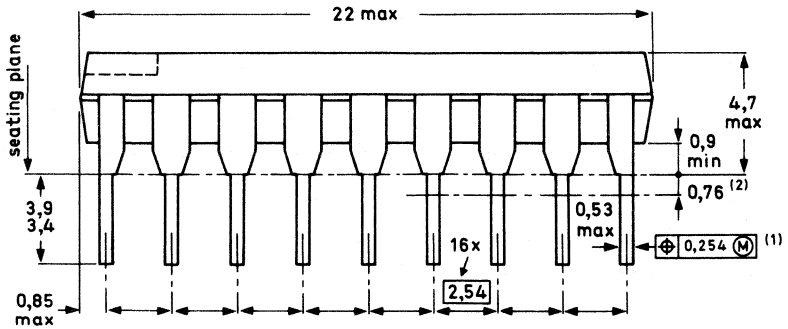
Ⓜ Maximum Material Condition.

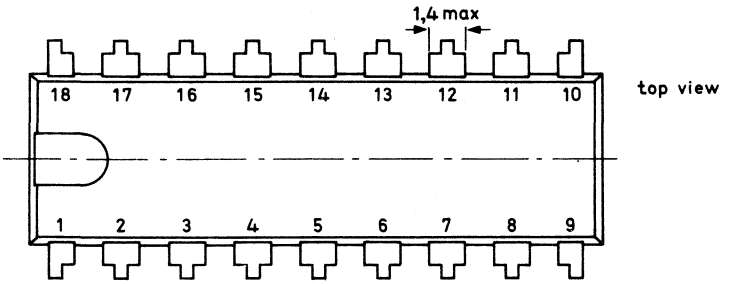
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

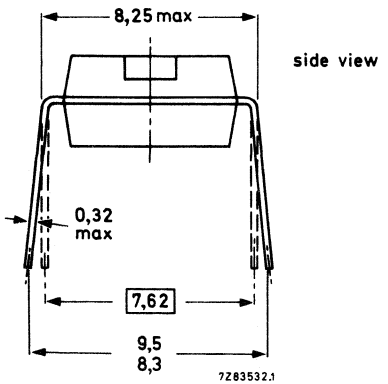
(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

18-LEAD DUAL IN-LINE; PLASTIC (SOT102)







⊕ Positional accuracy.

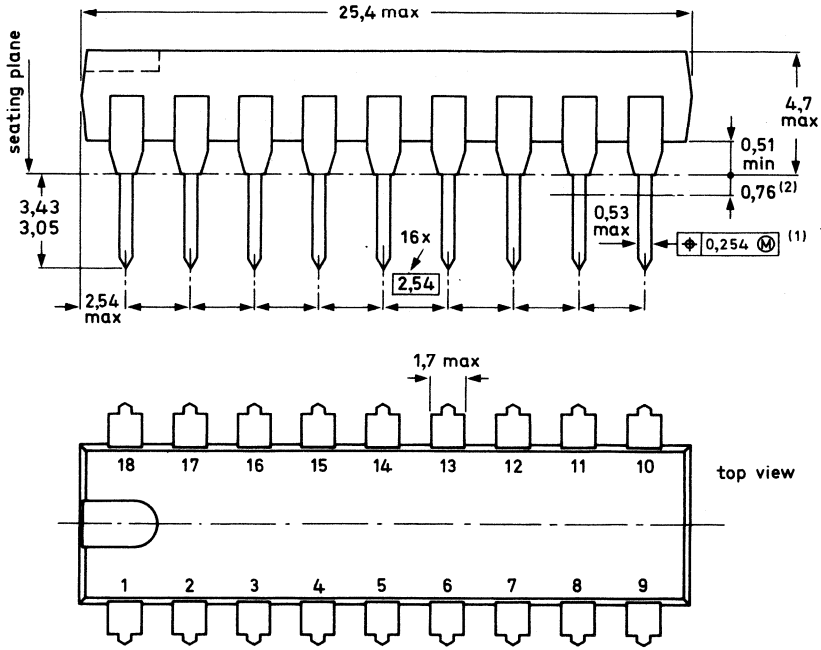
Ⓜ Maximum Material Condition.

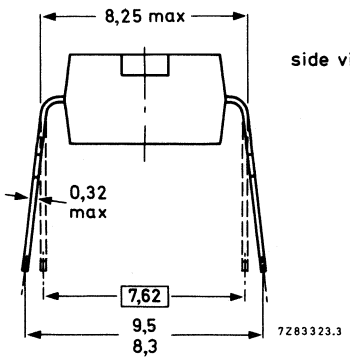
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

18-LEAD DUAL IN-LINE; PLASTIC (SOT102G, N, PE)





⊕ Positional accuracy.

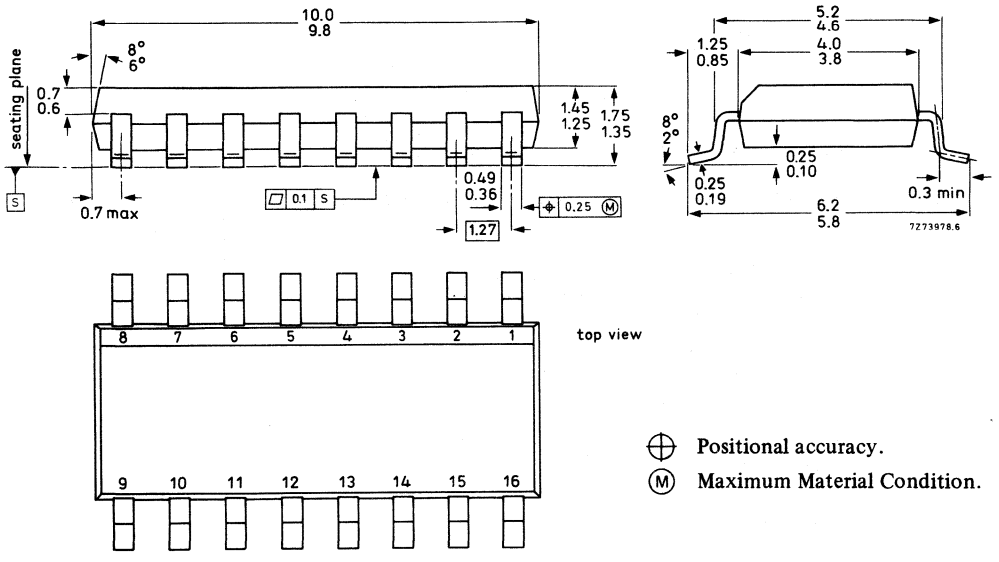
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD MINI-PACK; PLASTIC (SO16; SOT109A)

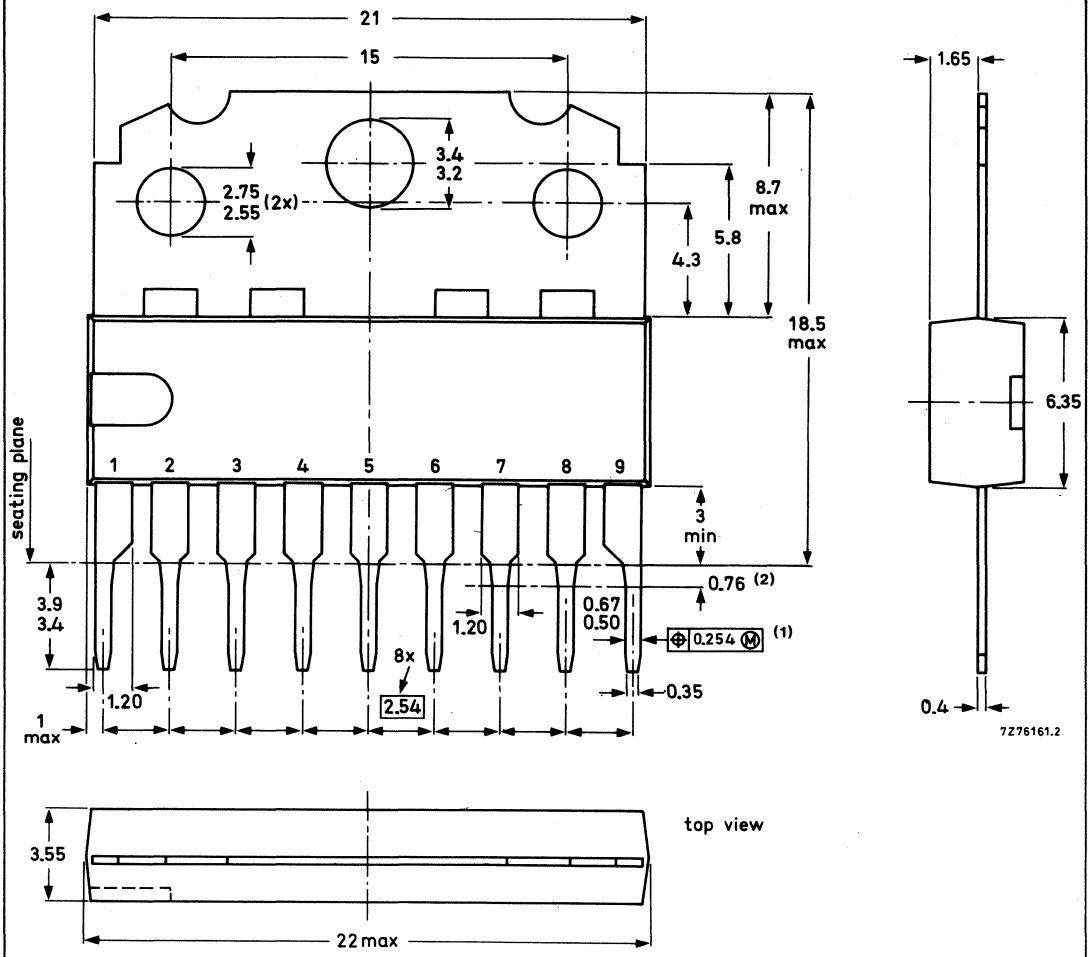


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

9-LEAD SINGLE IN-LINE; PLASTIC (SOT110B)



⊕ Positional accuracy.

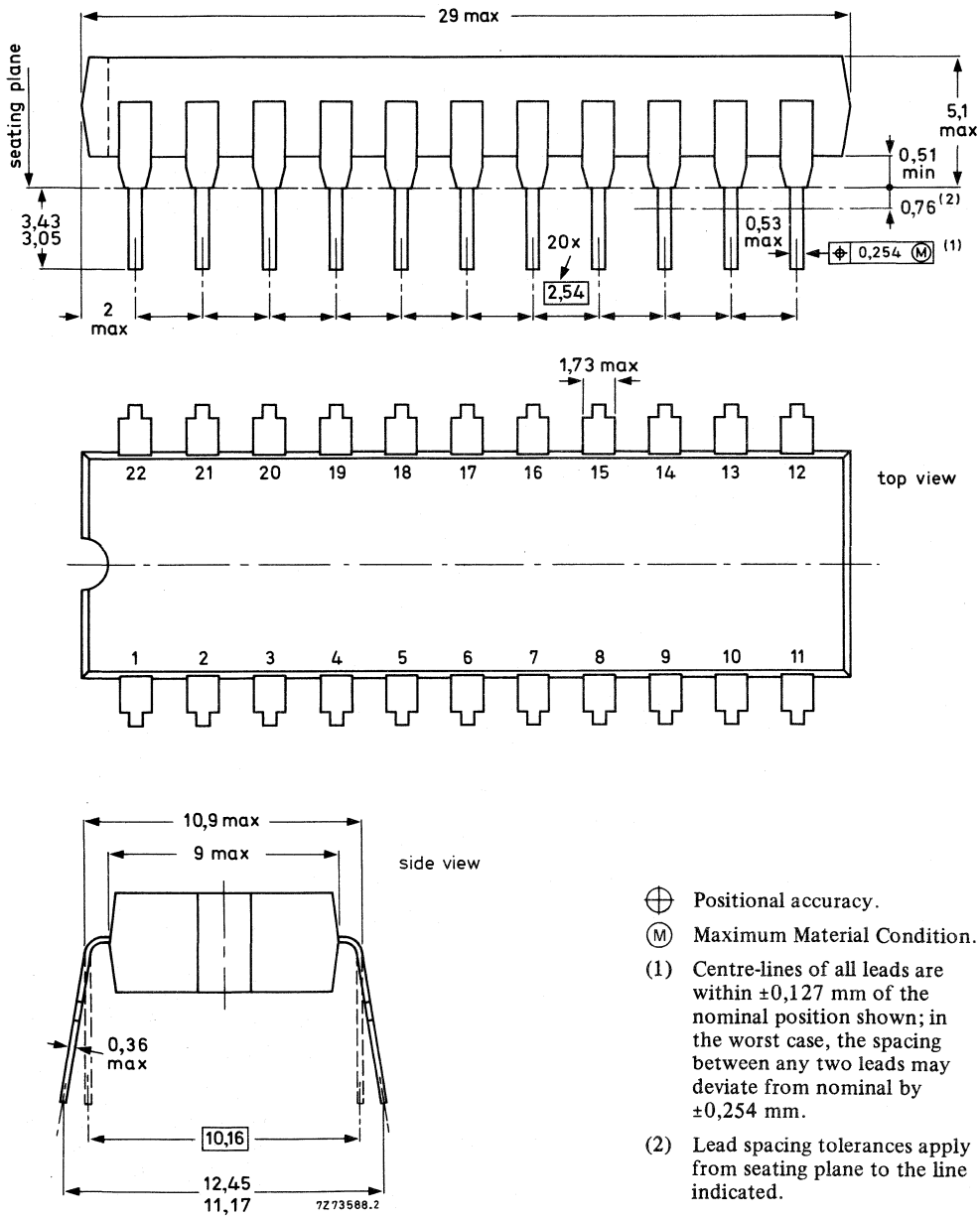
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

22-LEAD DUAL IN-LINE; PLASTIC (SOT116)



⊕ Positional accuracy.

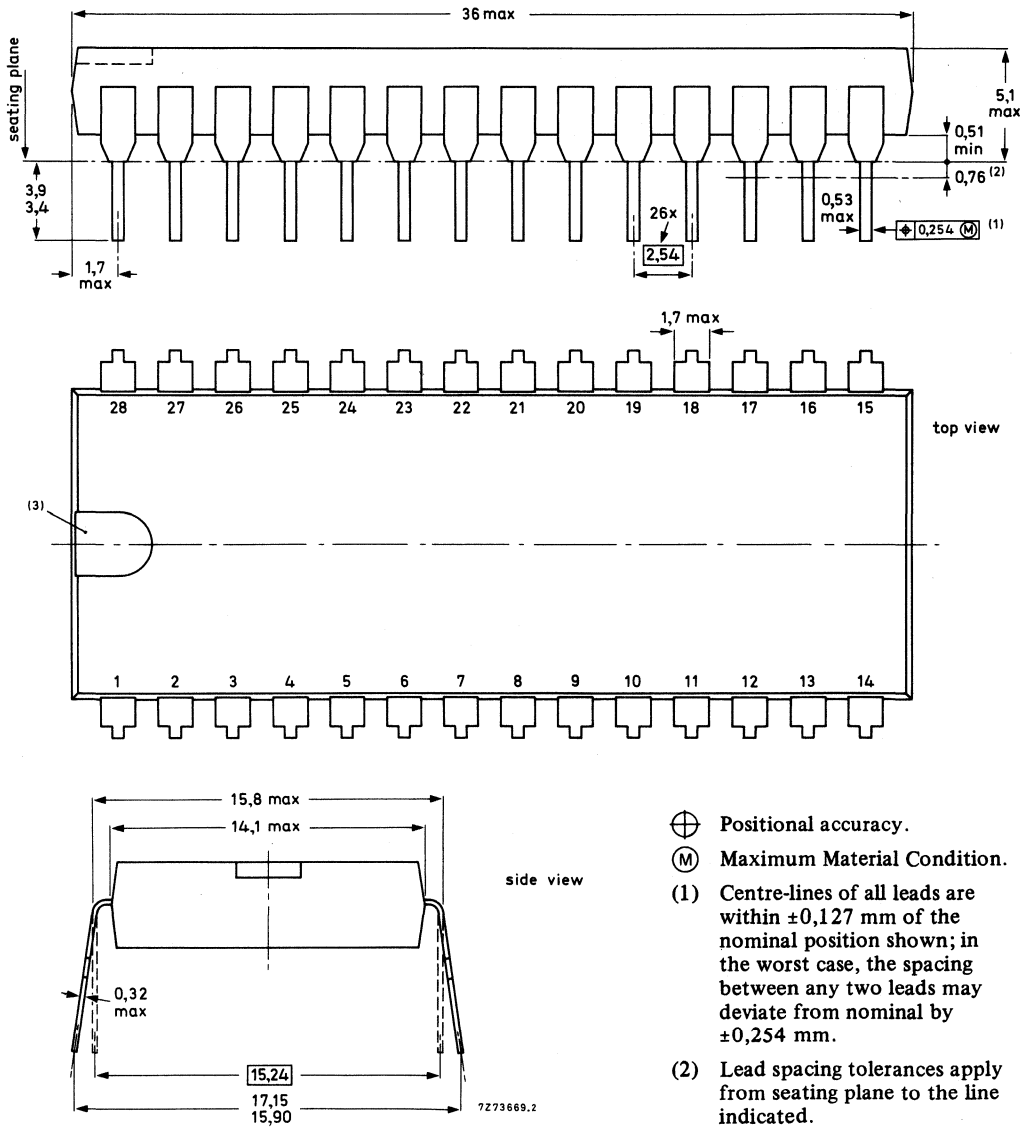
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

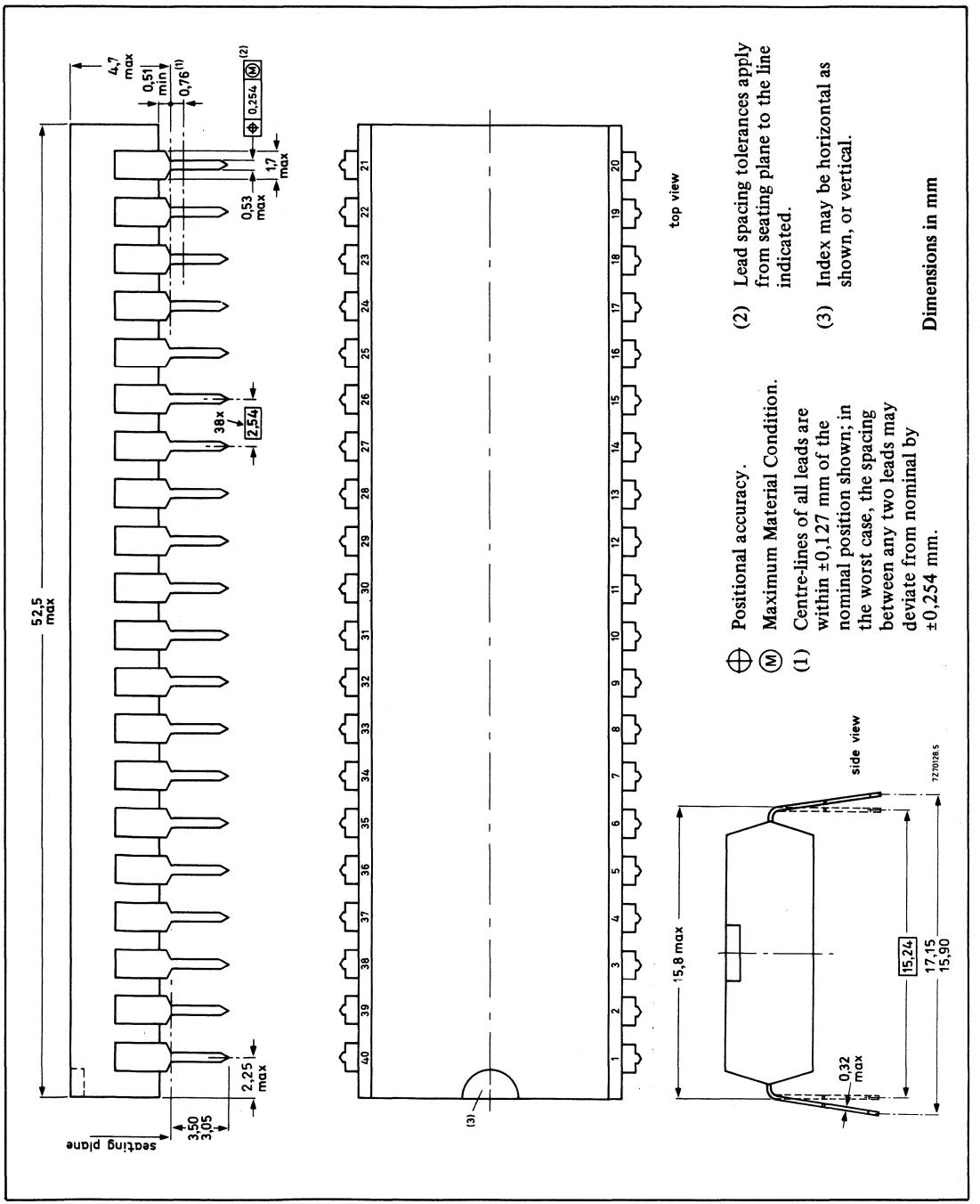
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

40-LEAD DUAL IN-LINE; PLASTIC (SOT129)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

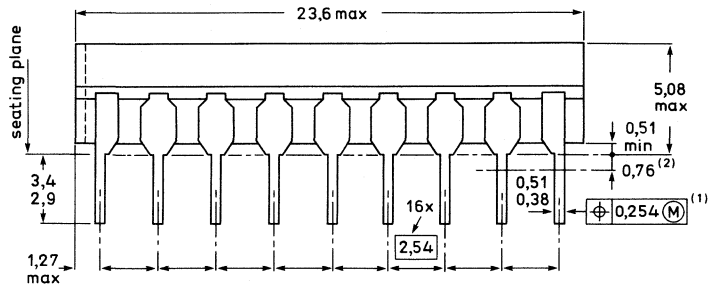
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

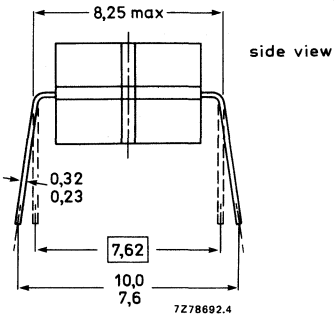
(2) Lead spacing tolerances apply from seating plane to the line indicated.

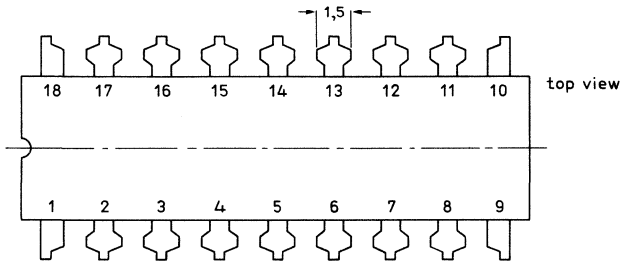
(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

18-LEAD DUAL IN-LINE; CERAMIC (CERDIP) (SOT133B)







⊕ Positional accuracy.

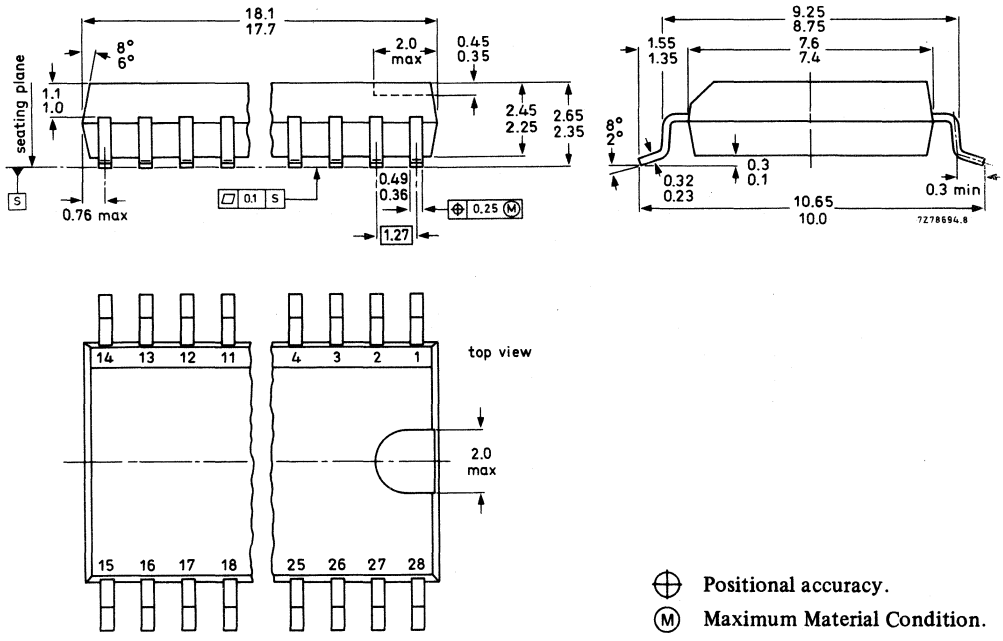
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

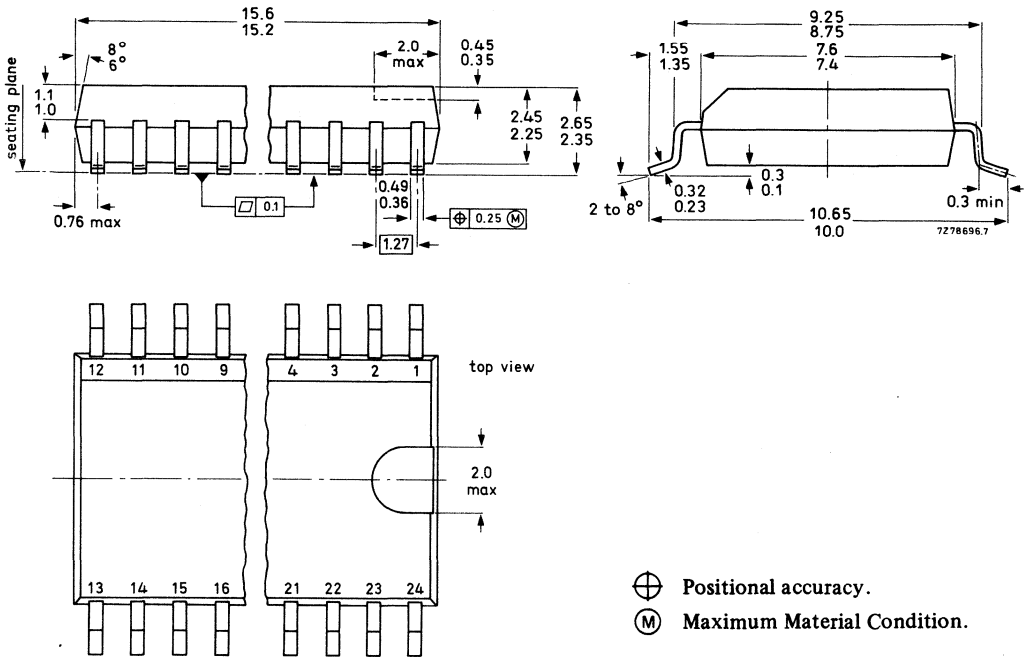
Dimensions in mm

28-LEAD MINI-PACK; PLASTIC (SO28; SOT136A)



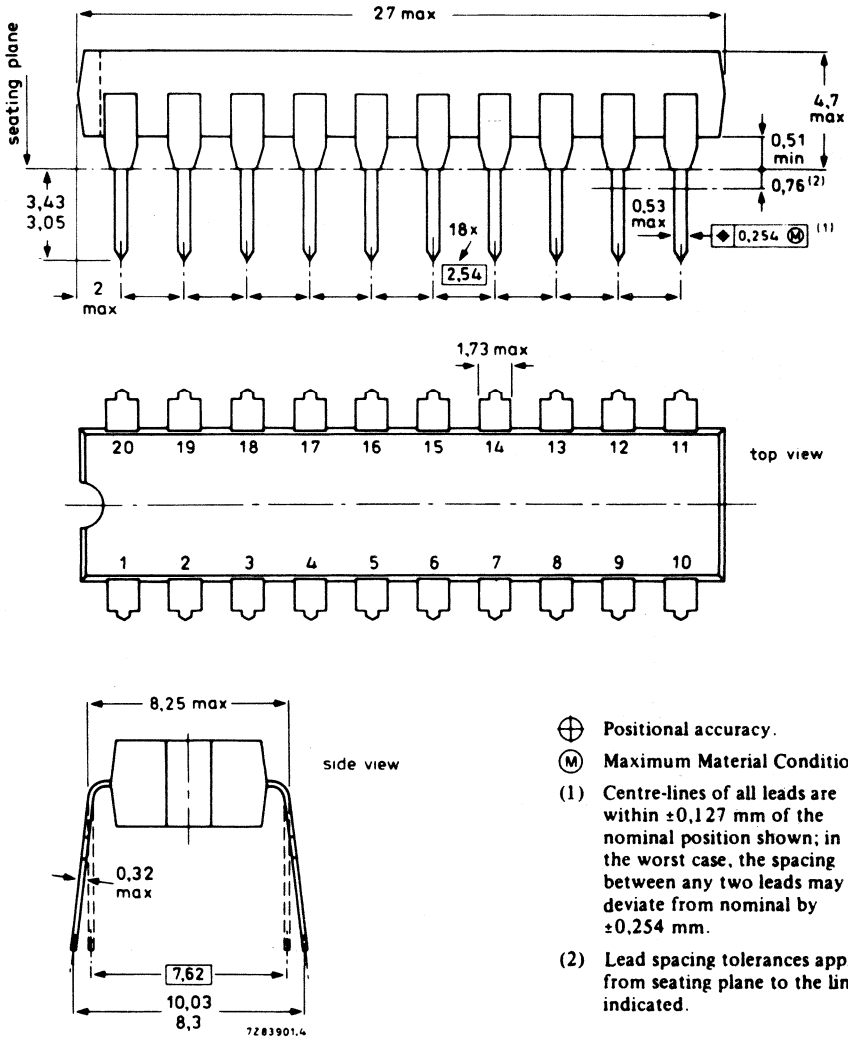
Dimensions in mm

24-LEAD MINI-PACK; PLASTIC (SO24; SOT137A)



Dimensions in mm

20-LEAD DUAL IN-LINE; PLASTIC (SOT146)



⊕ Positional accuracy.

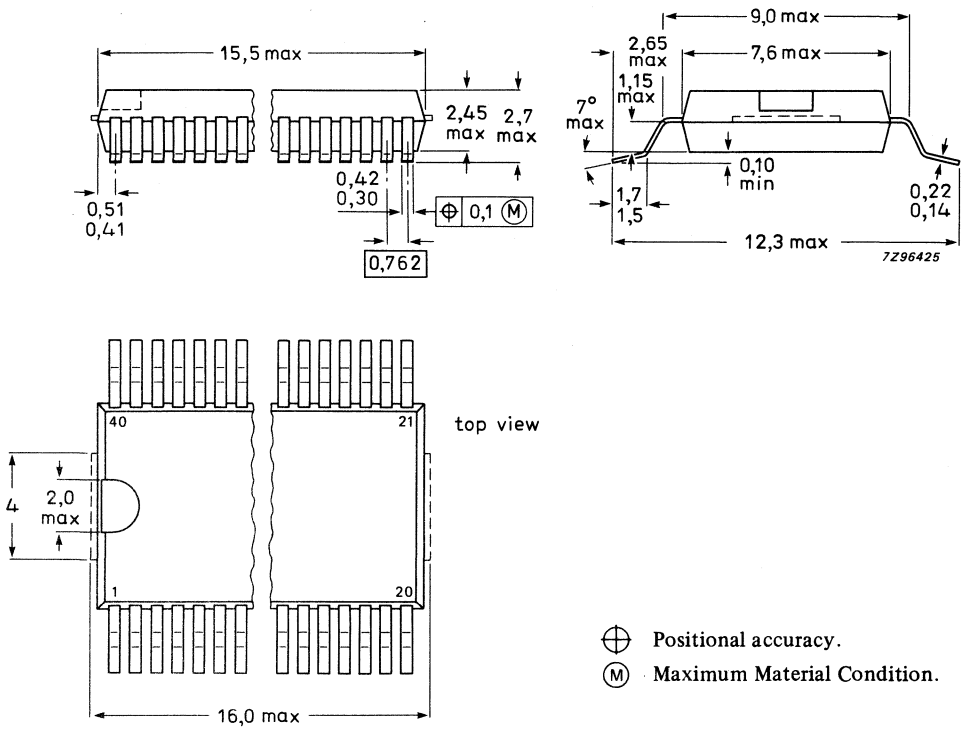
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

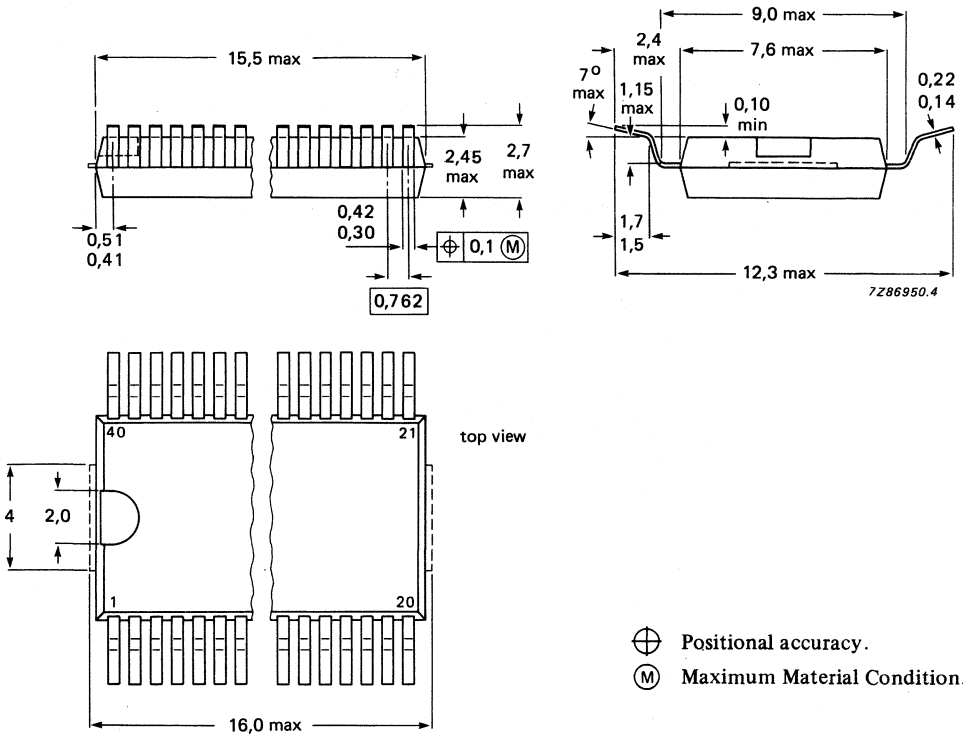
Dimensions in mm

40-LEAD MINI-PACK; PLASTIC (VSO40; SOT158A)



Dimensions in mm

40-LEAD MINI-PACK; PLASTIC (OPPOSITE BENT LEADS) (VSO40; SOT158B)

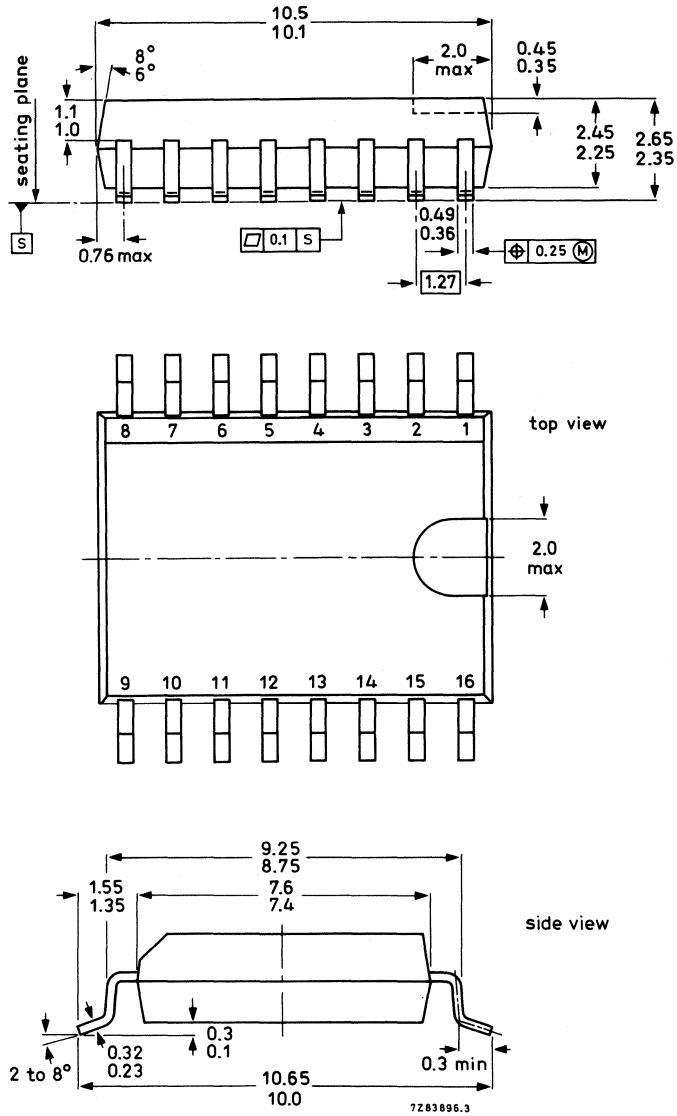


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

16-LEAD MINI-PACK; PLASTIC (SO16L; SOT162A)

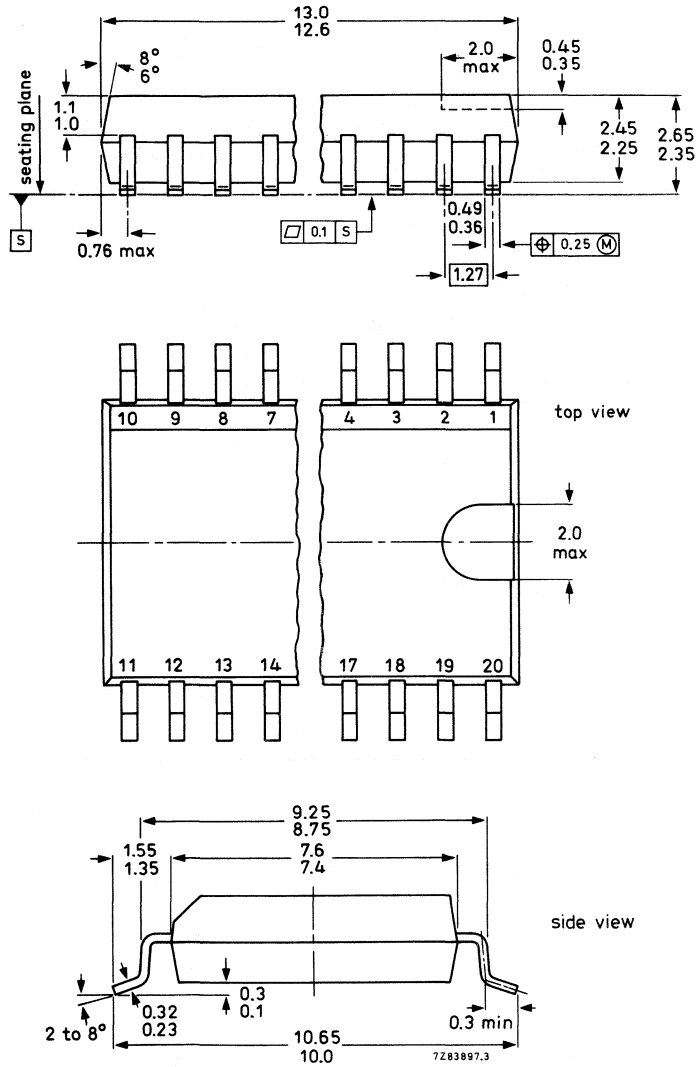


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

20-LEAD MINI-PACK; PLASTIC (SO20; SOT163A)

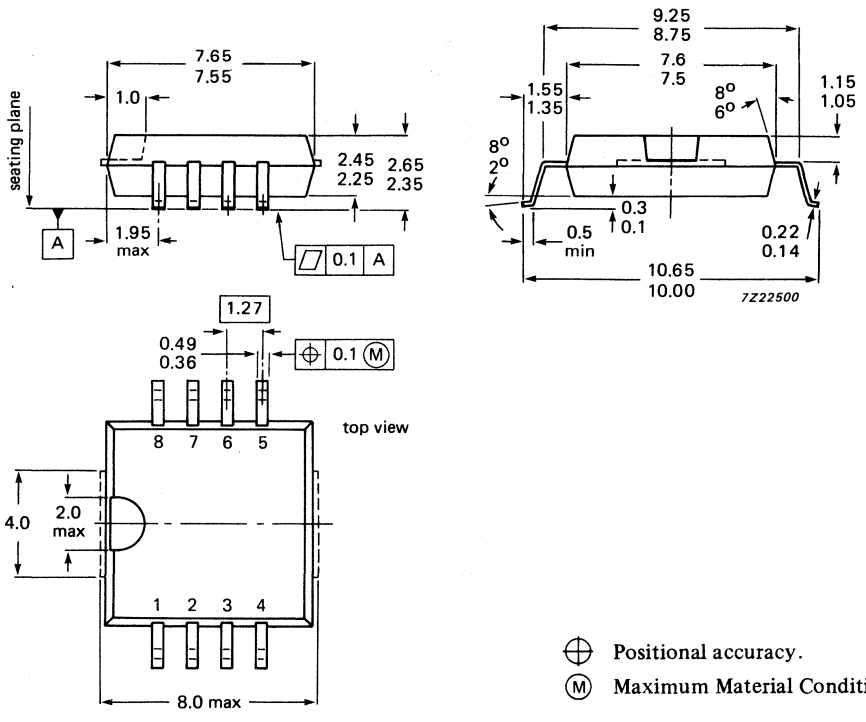


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO8L; SOT176C)

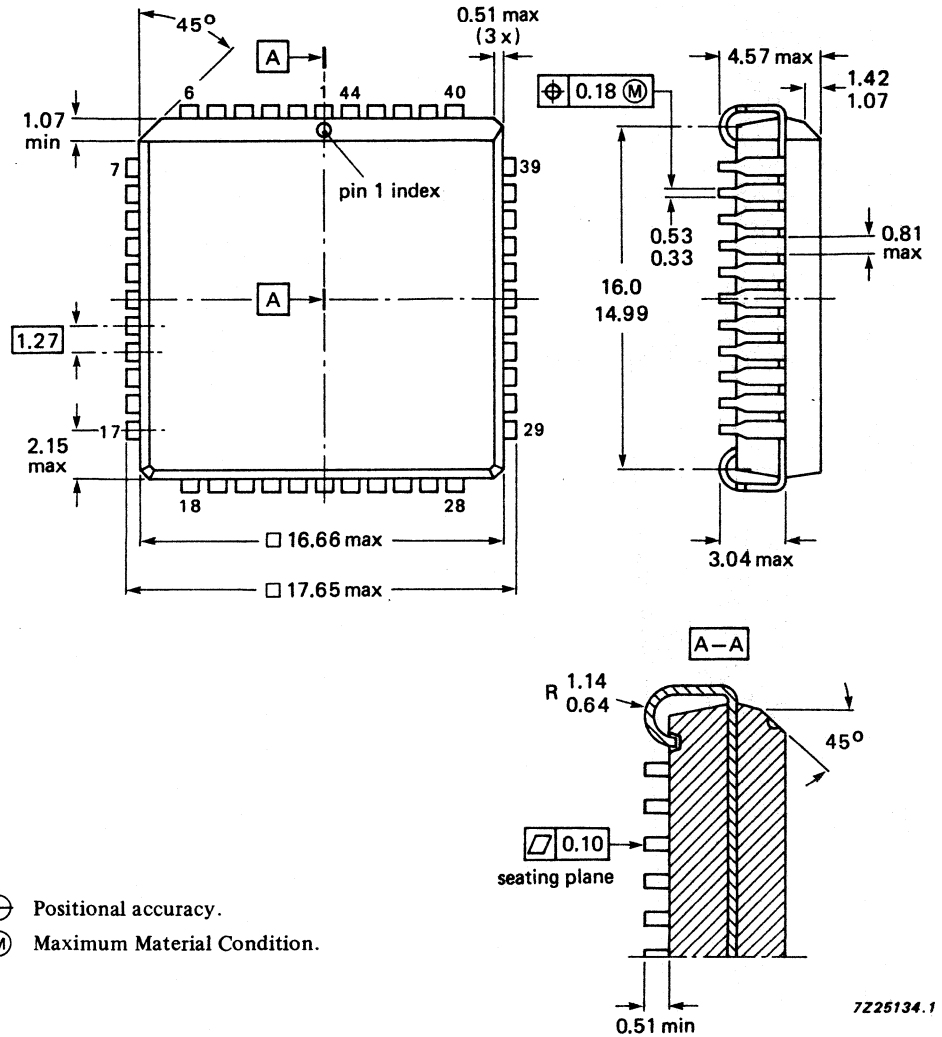


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

44-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); 'POCKET' VERSION (SOT187AA)

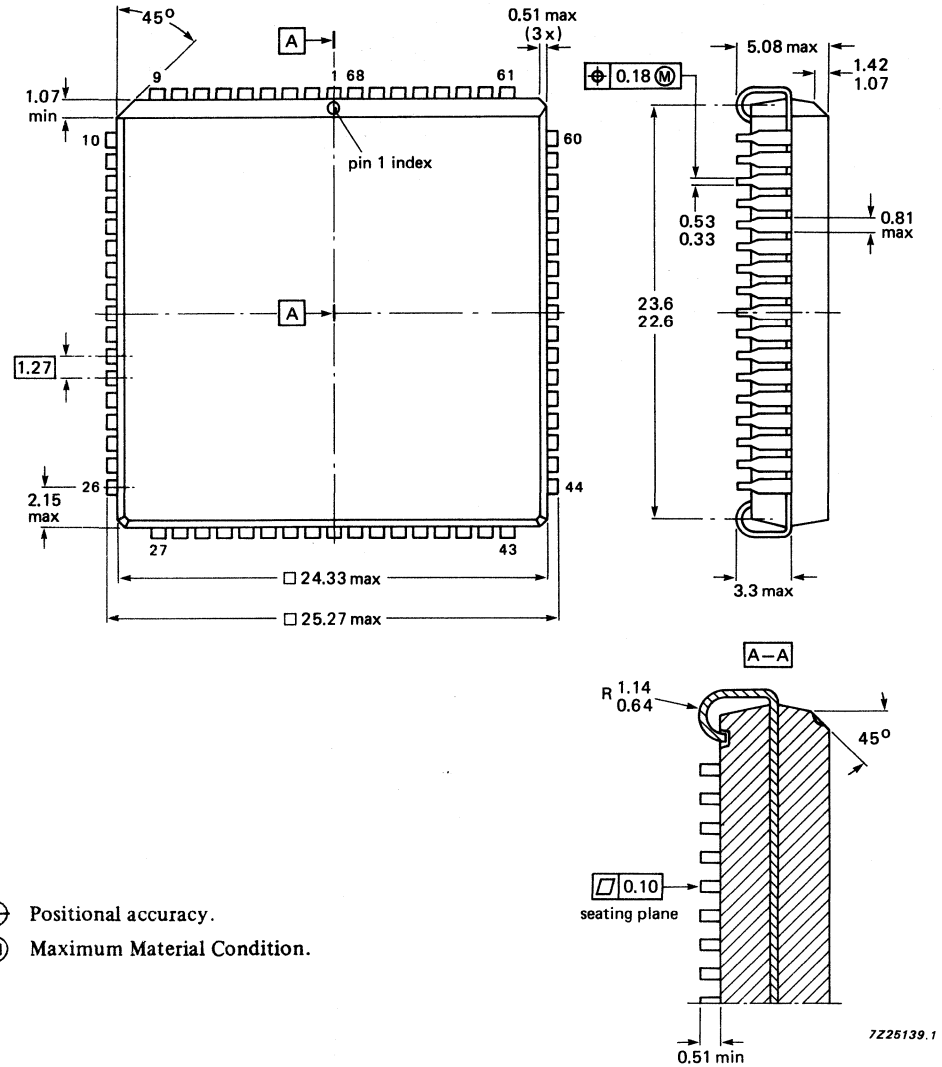


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

68-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); 'POCKET' VERSION (SOT188AA)

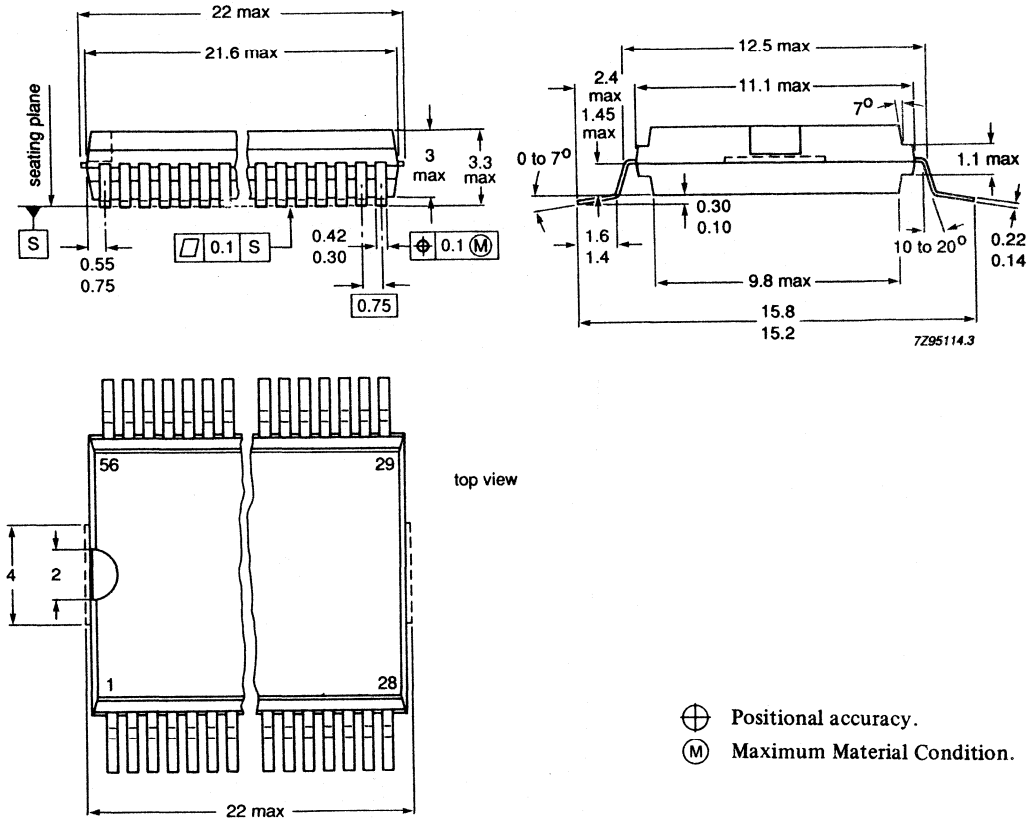


⊕ Positional accuracy.

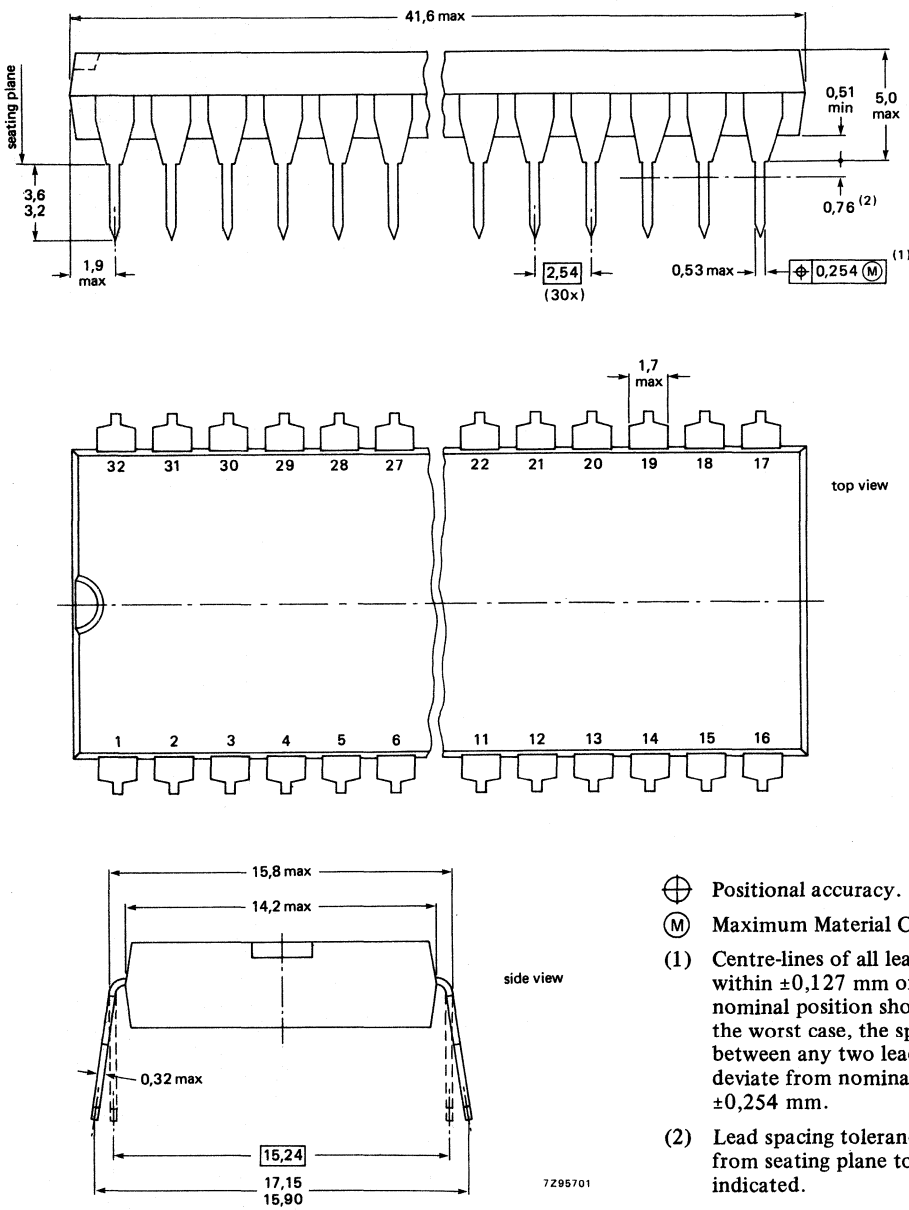
Ⓜ Maximum Material Condition.

Dimensions in mm

56-LEAD MINI-PACK; PLASTIC (VSO56; SOT190)



32-LEAD DUAL IN-LINE; PLASTIC (SOT201)



⊕ Positional accuracy.

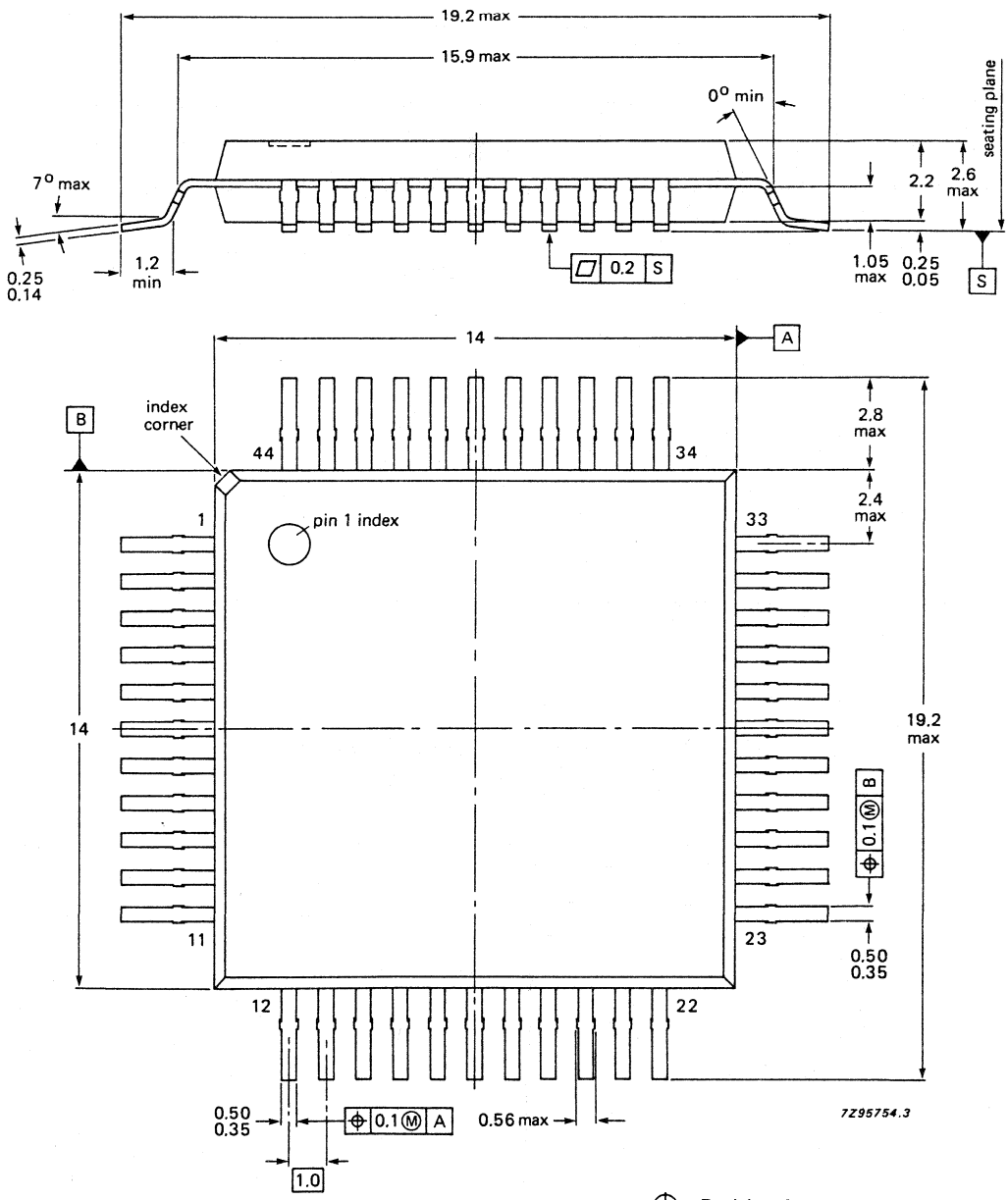
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

44-LEAD QUAD FLAT-PACK; PLASTIC (SOT205A)

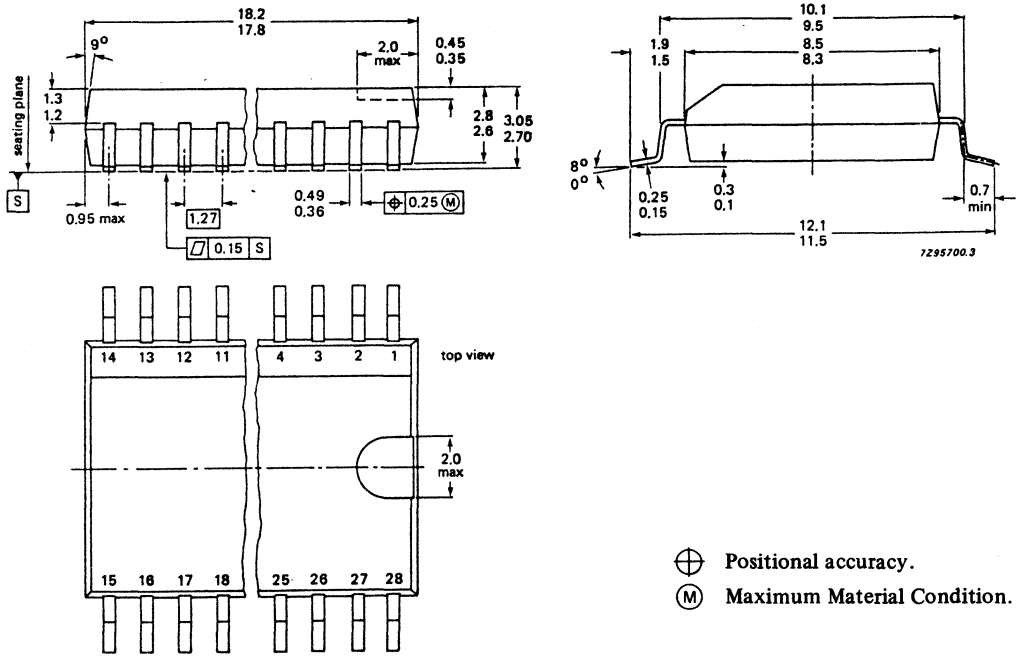


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

28-LEAD MINI-PACK; PLASTIC (SO28XL; SOT213)

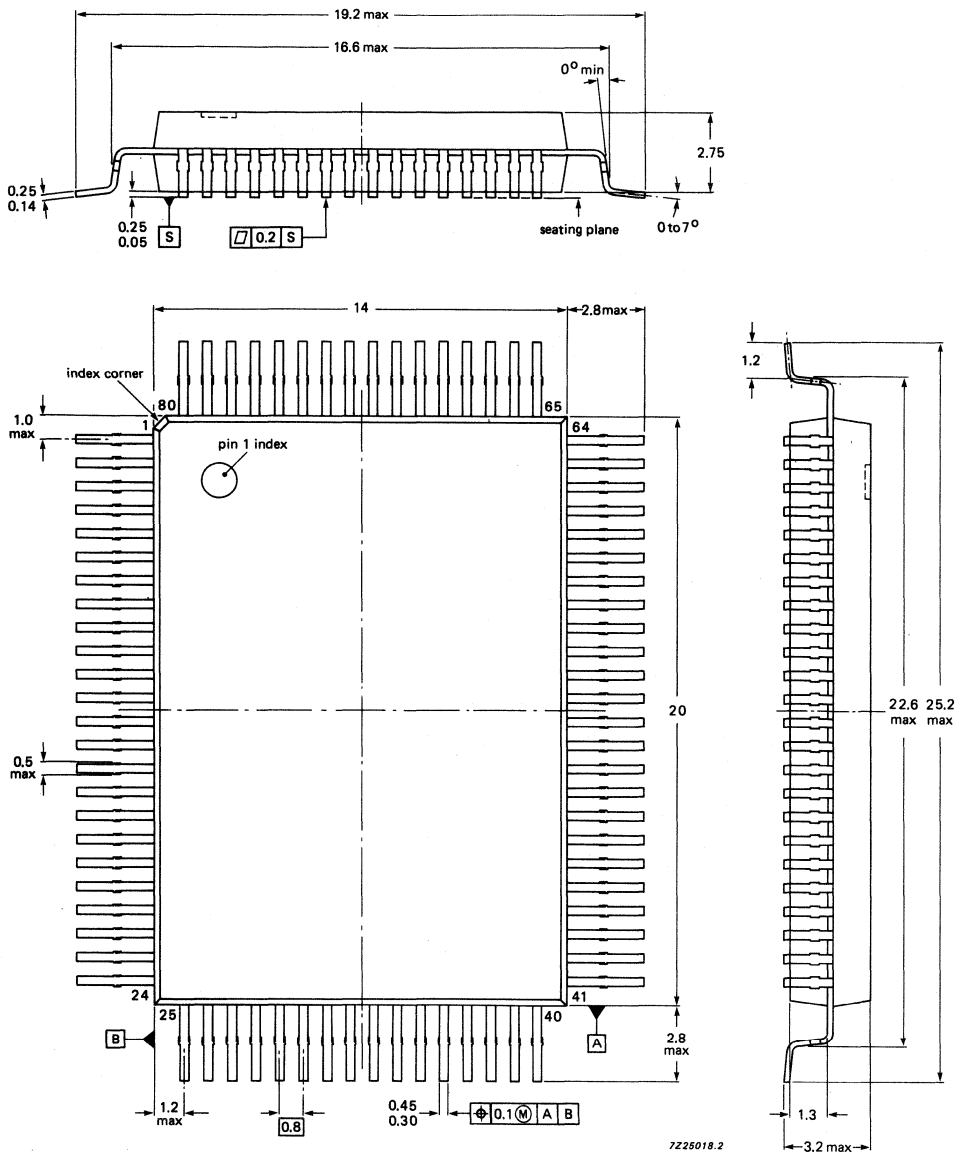


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

80-LEAD QUAD FLAT-PACK; PLASTIC (SOT219)

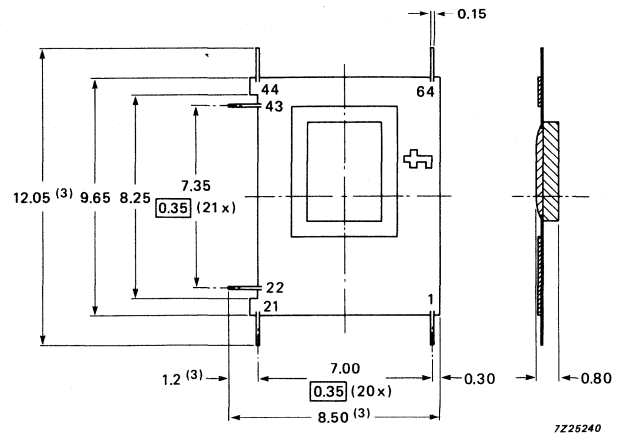


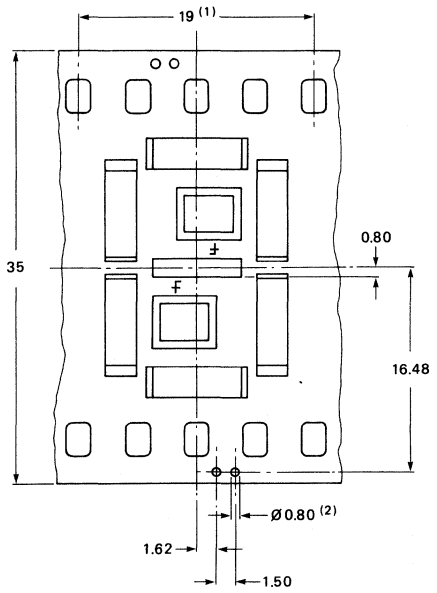
⊕ Positional accuracy.

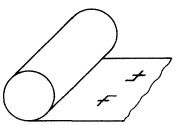
Ⓜ Maximum Material Condition.

Dimensions in mm

64-LEAD TAPE-AUTOMATED-BONDING (TAB) MODULE (SOT267A,C,D)







7Z25241

(1) 1 pattern = 4 perforation pitch intervals (contains two modules)
(2) Circuit-test holes
(3) Fixed by the user

Dimensions in mm

SOLDERING

Plastic mini-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave) in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been preheated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS (BY HAND)

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

SOLDERING

Tab modules

FLUXING

Use a flux that does not have to be removed, or a water-soluble flux.

SOLDERING

The reflow soldering method using a pulse-heated tool is usually suitable. Limit the soldering operation to 3 s at 250 °C at the leads.

CLEANING

Avoid cleaning if possible. If cleaning is necessary, use cold or hot water. A detergent may be added to the water. Finally rinse with de-ionized water.

Do **not** use ultrasonic cleaning methods as these may damage the inner or outer leads.

Do **not** use solvents.

DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of seven series of handbooks:

INTEGRATED CIRCUITS

DISCRETE SEMICONDUCTORS

DISPLAY COMPONENTS

PASSIVE COMPONENTS*

PROFESSIONAL COMPONENTS**

MAGNETIC PRODUCTS*

LIQUID CRYSTAL DISPLAYS

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* Will replace the Components and materials (green) series of handbooks.
** Will replace the Electron tubes (blue) series of handbooks.

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* Not yet issued with the new code in this series of handbooks.
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ADS86
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